Data Book

AU6391

USB2.0 to ATA/ATAPI Bridge Controller

Technical Reference Manual

Product Specification

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Product specification	This data book contains final product specifications.

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1.0 Introduction

1.1 Description

The AU6391 is a single chip controller designed for bridgingg USB 2.0 to ATA/ATAPI bus interface. It is used as the primary controller of building an external USB 2.0 hard disk or CD/DVD drives.

To maximize the data throughput and achieve the best compatibility, AU6391 is equipped with Alcor's proprietary automatic speed negotiation (ASN) algorithm. The ASN algorithm allows AU6391 to select optimized operating mode that device can best support a reliable data transfer from PIO mode 0~4 and Ultra DMA mode 2/4. The silicon would work with the default device driver from Windows ME, Windows 2000, Windows XP and Mac OS X, however, vendor device driver provided by Alcor Micro would enable the built device working under Windows 98, Windows 2000 (SP1/SP2) and Mac OS 9.

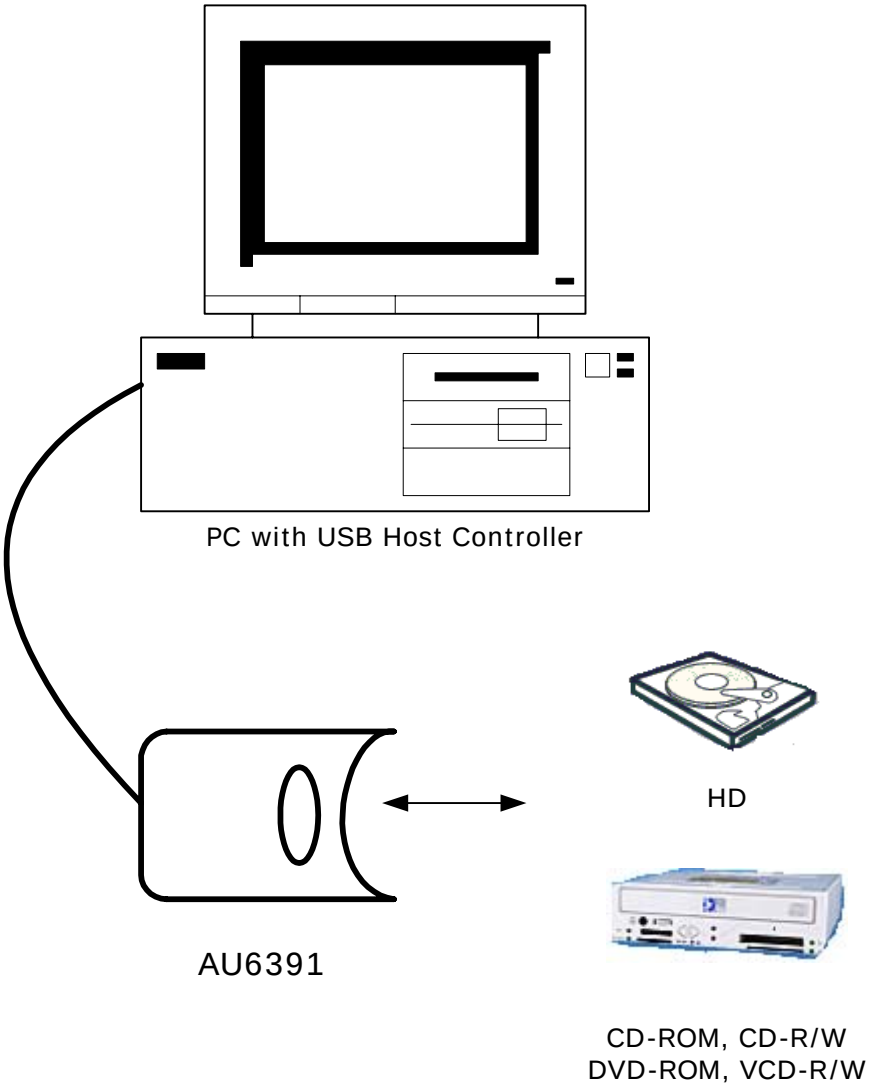
1.2 Features

- Supports USB 2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Supports ATA/ATAPI-6 specification Revision 1.0
  - PIO mode 0~4
  - UDMA mode 2/4
- Supports ATA/ATAPI device configured in master or slave mode
- Supports 48-bit addressing for large capacity hard drive
- Hardware DMA engine integrated inside for performance enhancement
- Works with default device driver from Windows ME/2000/XP and Mac OS X.
- One spared LED pin for disk access indication
- Built-in voltage regulator
- 48-pin LQFP package

2.0 Application Block Diagram

The following picture is an application diagram of a typical removable USB2.0 ATA/ATAPI device. With such kinds of devices, users can exchange recorded digital content between ATA/ATAPI device and PC (Notebook) via USB.

2.1 Block Diagram



3.0 Pin Assignment

There are two different form factor packages available to choose from. The following figure shows signal names for each pin and the table in the page after describes each pin in details.

Figure 3.1 GBL bonding Pin Assignment Diagram

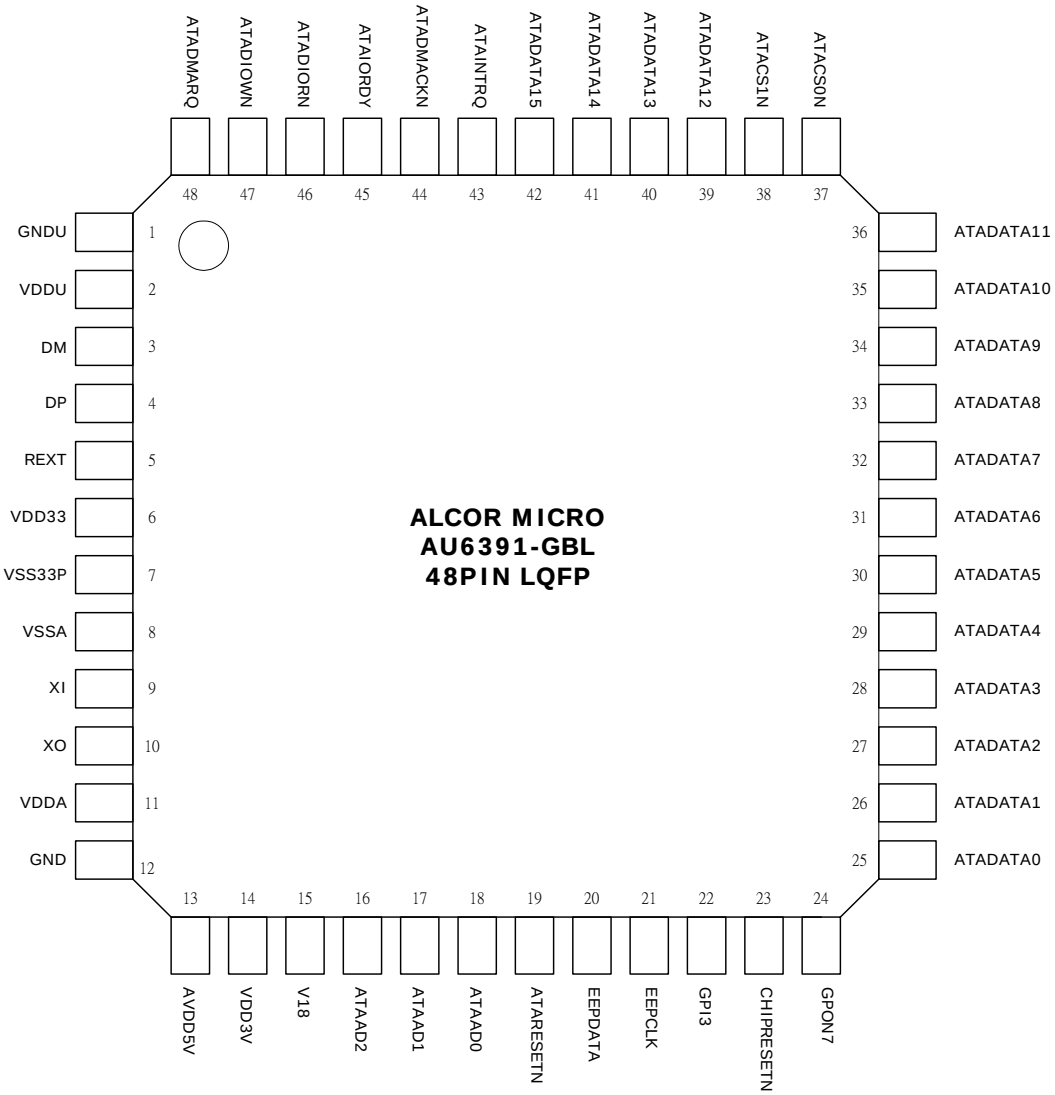


Table 3.1 GBL bonding Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GNDU	PWR	GND for UTMI Power
2	VDDU	PWR	Power for UTMI core
3	DM	I/O	USB DM
4	DP	I/O	USB DP
5	REXT	I	Connect pull-low resistor for impedance match
6	VDD33	PWR	UTMI power 3.3V
7	VSS33P	PWR	UTMI power GND
8	VSSA	PWR	Analog GND
9	XI	I	12 MHz crystal input.
10	XO	O	12 MHz crystal output.
11	VDDA	PWR	Analog 1.8V power
12	GND		GND for IO pad
13	AVDD5V	I	5V power supply input
14	VDD3V	O	3.3V Power Out
15	V18	PWR	1.8 V output for core power
16	ATAAD2	O	ATA Address bus 2
17	ATAAD1	O	ATA Address bus 1
18	ATAAD0	O	ATA Address bus 0
19	ATARESETN	O	ATA Reset
20	EEPDATA	B	EEPDATA
21	EEPCLK	B	EEPCLK
22	GPI3	I	GPI for customized software triggle
23	CHIPRESETN	I	Reset (low active to reset the whole chip), must be pull up with RC.
24	GPON7	O	LED indicator

Pin #	Pin Name	I/O	Description
25	ATADATA0	I/O	ATA Data Bus 0
26	ATADATA1	I/O	ATA Data Bus 1
27	ATADATA2	I/O	ATA Data Bus 2
28	ATADATA3	I/O	ATA Data Bus 3
29	ATADATA4	I/O	ATA Data Bus 4
30	ATADATA5	I/O	ATA Data Bus 5
31	ATADATA6	I/O	ATA Data Bus 6
32	ATADATA7	I/O	ATA Data Bus 7
33	ATADATA8	I/O	ATA Data Bus 8
34	ATADATA9	I/O	ATA Data Bus 9
35	ATADATA10	I/O	ATA Data Bus 10
36	ATADATA11	I/O	ATA Data Bus 11
37	ATACS0N	O	ATA Chip Select0
38	ATACS1N	O	ATA Chip Select1
39	ATADATA12	I/O	ATA Data Bus 12
40	ATADATA13	I/O	ATA Data Bus 13
41	ATADATA14	I/O	ATA Data Bus 14
42	ATADATA15	I/O	ATA Data Bus 15
43	ATAINTRQ	I	ATA Interput request
44	ATADMACKN	O	ATA Control Signal DMACKN
45	ATAIORDY	I	ATA Control Signal IORDY
46	ATADIORN	O	ATA Control Signal DIORN
47	ATADIOWN	O	ATA Control Signal DIOWN
48	ATADMARQ	I	ATA Control Signal DMARQ

The following figure shows signal names of each pin of the 48-pin package and the table in the page after describes each pin in details.

Figure 3.1 GEL bonding Pin Assignment Diagram

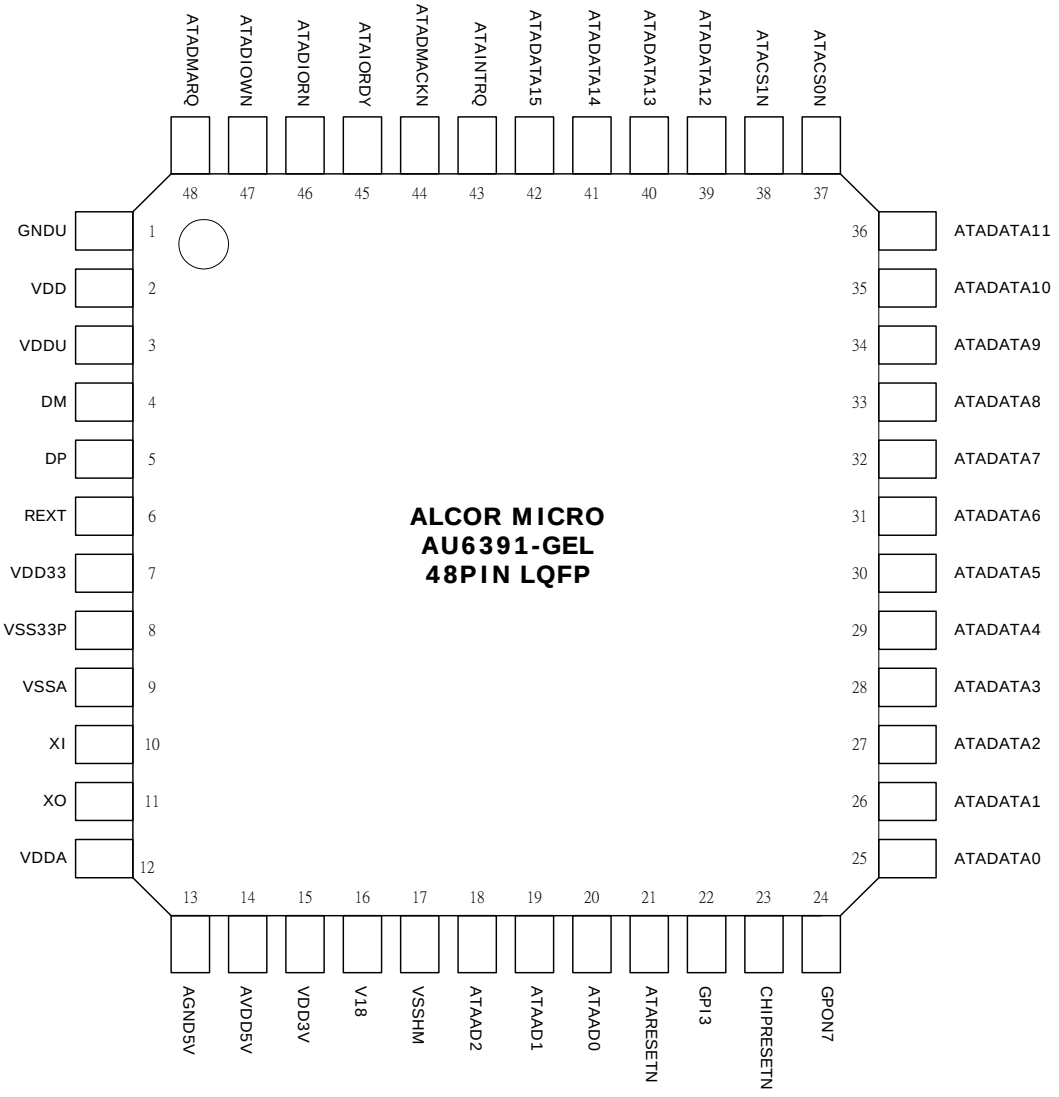


Table 3.1 GEL bonding Pin Descriptions

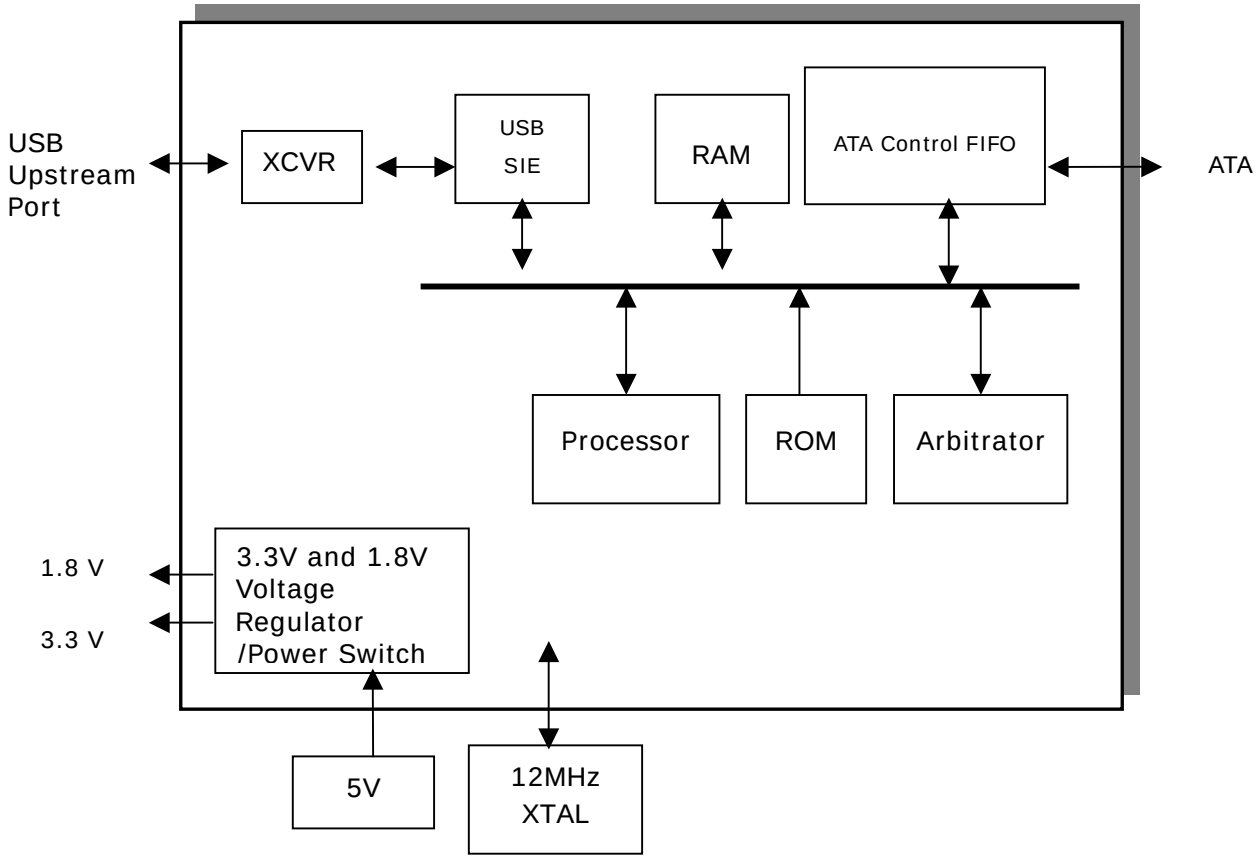
Pin #	Pin Name	I/O	Description
1	GNDU	GND	Ground
2	VDD	PWR	1.8V
3	VDDU	PWR	Power for UTMI core
4	DM	I/O	USB DM
5	DP	I/O	USB DP
6	REXT	I	Connect pull-low resistor for impedance match
7	VDD33	PWR	3.3V
8	VSS33P	PWR	UTMI power GND
9	VSSA	PWR	Analog GND
10	XI	I	12 MHz crystal input.
11	XO	O	12 MHz crystal output.
12	VDDA	PWR	1.8V
13	AGND5V	GND	Ground
14	AVDD5V	I	5V Power Source
15	VDD3V	O	3.3 V Power Out
16	V18	PWR	1.8 V output for core power
17	VSSHM	GND	Ground
18	ATAAD2	O	ATA Address bus [2]
19	ATAAD1	O	ATA Address bus [1]
20	ATAAD0	O	ATA Address bus [0]
21	ATARESETN	O	ATA Reset
22	GPI3	I	General Purpose Input.
23	CHIPRESETN	I	Reset (low active to reset the whole chip), must be pull up with RC.
24	GPON7	O	General Purpose Output.
25	ATADATA0	I/O	ATA Data Bus [0]

Pin #	Pin Name	I/O	Description
26	ATADATA1	I/O	ATA Data Bus [1]
27	ATADATA2	I/O	ATA Data Bus [2]
28	ATADATA3	I/O	ATA Data Bus [3]
29	ATADATA4	I/O	ATA Data Bus [4]
30	ATADATA5	I/O	ATA Data Bus [5]
31	ATADATA6	I/O	ATA Data Bus [6]
32	ATADATA7	I/O	ATA Data Bus [7]
33	ATADATA8	I/O	ATA Data Bus [8]
34	ATADATA9	I/O	ATA Data Bus [9]
35	ATADATA10	I/O	ATA Data Bus [10]
36	ATADATA11	I/O	ATA Data Bus [11]
37	ATACS0N	O	ATA Chip Select0
38	ATACS1N	O	ATA Chip Select1
39	ATADATA12	I/O	ATA Data Bus [12]
40	ATADATA13	I/O	ATA Data Bus [13]
41	ATADATA14	I/O	ATA Data Bus [14]
42	ATADATA15	I/O	ATA Data Bus [15]
43	ATAINTRQ	I	ATA Interput request
44	ATADMACKN	O	ATA Control Signal DMACKN
45	ATAIORDY	I	ATA Control Signal IORDY
46	ATADIORN	O	ATA Control Signal DIORN
47	ATADIOWN	O	ATA Control Signal DIOWN
48	ATADMARQ	I	ATA Control Signal DMARQ

4.0 System Architecture and Reference Design

4.1 AU6391 Block Diagram

Figure 4.1 AU6391 Block Diagram



5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDHM}	Power Supply	-0.3 to V_{DDHM} +0.3	V
V_{IN}	Input signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output signal Voltage	-0.3 to V_{DDHM} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
A_{VDD5V}	Power Supply	4.75	5.0	5.25	V
V_{DDHM}	Power Supply	3.0	3.3	3.6	V
V_{DD} V_{18}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	^{O}C

5.3 Leakage Current and Capacitance

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	no pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDHM}	Power supply	3.3V I/O	3.0	3.0	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{DDHM} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD33	Analog supply voltage		3.0	3.3	3.6	V
VDD V18	Digital supply voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA
$I_{CC(susp)}$	Suspend supply current	In suspend mode, current with 1.5kΩ pull-up resistor on pin RPU disconnected			120	µA

Table 5.6 Static characteristic : Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VDDH*-0.2			V

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						

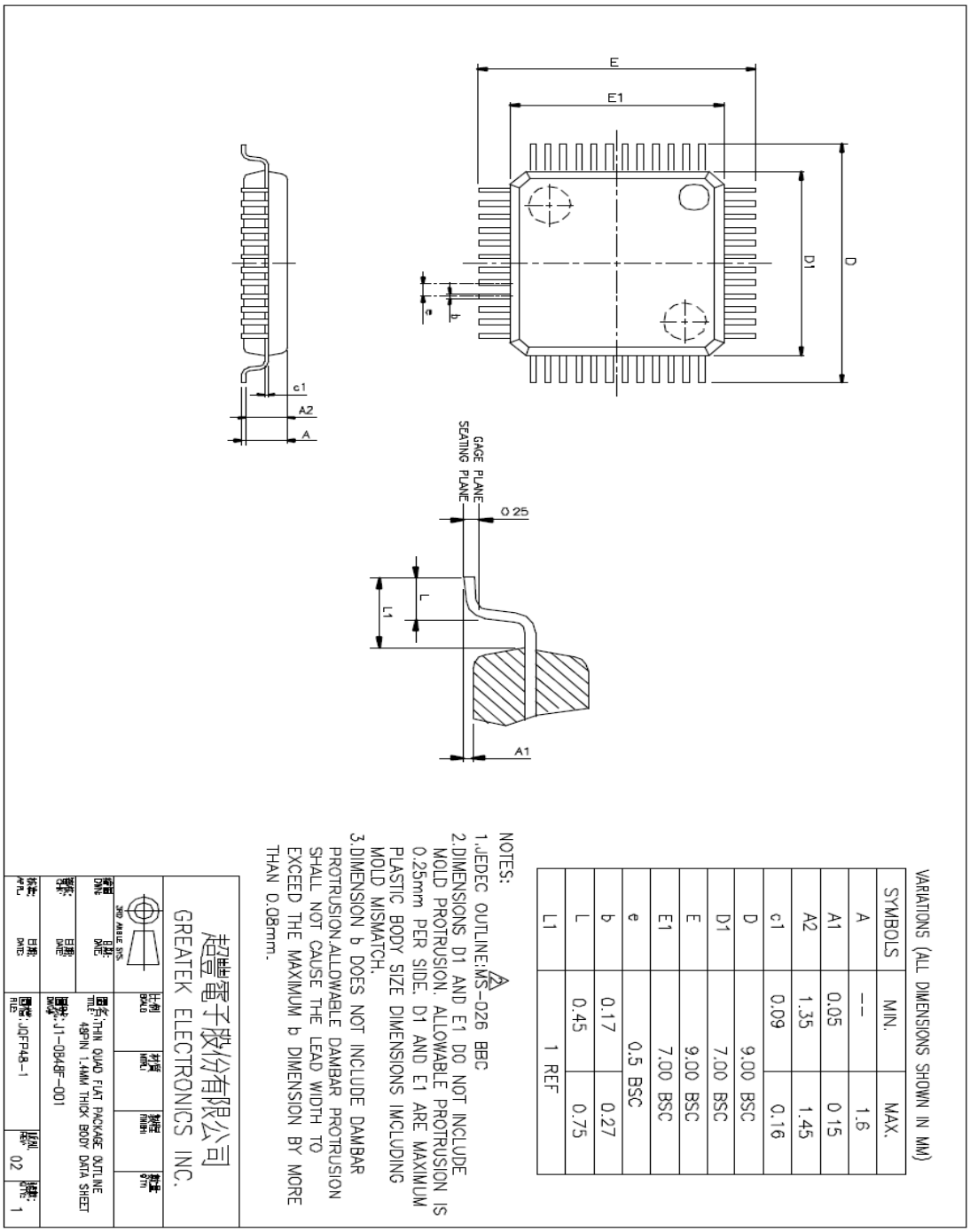
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns
t_{LF}	Fall time	CL=200pF-600pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

6.0 Mechanical Information

Figure 6.1 Mechanical Information Diagram



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

超豐電子股份有限公司
GREATEK ELECTRONICS INC.

TITLE:	48PIN THIN QUAD FLAT PACKAGE OUTLINE 1.4MM THICK BODY DATA SHEET
DWG #:	J1-0848F-001
REV:	02
SHEET:	1

7.0 Abbreviations

This chapter lists and defines terms and abbreviations used throughout this specification.

SIE Serial Interface Engine
ATA Advanced Technology Attachment
UTMI USB Transceiver Macrocell Interface

【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.