Semicustom

CMOS

Embedded array

CE81 Series

■ **DESCRIPTION**

The CE81 series 0.18 μm CMOS embedded array is a line of highly integrated CMOS ASICs featuring high speed and low power consumption.

This series incorporates up to 34 million gates which have a gate delay time of 12 ps, resulting in both integration and speed about three times higher than conventional products.

In addition, CE81 series can operate at a power-supply voltage of down to 1.1 V, substantially reducing power consumption.

■ **FEATURES**

- Technology : 0.18 μm silicon-gate CMOS, 3- to 5-layer wiring
- Supply voltage : + 1.8 V ± 0.15 V (normal) to + 1.1 V ± 0.1 V
- Junction temperature range : −40 to +125 °C
- Gate delay time : t_{pd} = 12 ps (1.8 V, inverter, F/O = 1)
- Gate power consumption : P_d = 8 nW/MHz/BC (1.1 V, 2-NAND, F/O = 1)
- High-load driving capability : I_{OL} = 2/4/8/12 mA mixable
- Output buffer cells with noise reduction circuits
- Inputs with on-chip input pull-up/pull-down resistors (33 kΩ typical) and bidirectional buffer cells
- Buffer cells dedicated to crystal oscillator
- Special interface : P-CML, LVDS, PCI, AGP, USB, SDRAM-I/F, SSTL, and others (including those under development)
- IP macros : CPU, DSP, PCI, IEEE1394, USB, IrDA, PLL, ADC, DAC, and others (including those under development)
- Capable of incorporating compiled cells (RAM/ROM/multiplier, and others)
- Configurable internal bus circuits
- Advanced hardware/software co-design environment
- Short-term development using a timing driven layout tool
- Support for static timing sign-off
  Dramatically reducing the time for generating test vectors for timing verification and the simulation time

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- Hierarchical design environment for supporting large-scale circuits
- Simulation (before layout) considering the input slew rate and detailed RC delay calculation (after layout) , supporting development with minimized timing trouble after trial manufacture
- Support for memory (RAM/ROM) SCAN
- Support for memory (RAM) BIST
- Support for boundary SCAN
- Support for path delay test
- A variety of package options
   (TQFP, HQFP, EBGA, FBGA, TAB-BGA, LQFP)

■ MACRO LIBRARY (Including macros being prepared)

1. Logic cells (about 800 types)

• Adder	• Decoder
• AND-OR Inverter	• Non-SCAN Flip Flop
• Clock Buffer	• Inverter
• Latch	• Buffer
• NAND	• OR-AND Inverter
• AND	• OR
• NOR	• Selector
• SCAN Flip Flop	• BUS Driver
• ENOR	• EOR
• AND-OR	• Others

2. IP macros

|	
CPU/DSP	FR, SPARClite, standard CPU (under preparation) Communications DSP, DSP for AV
Interface macro	PCI, IEEE1394, USB, IrDA, etc.
Multimedia processing macros	JPEG, MPEG, etc.
Mixed signal macros	ADC, DAC, OPAMP, etc.
Compiled macros	RAM, ROM, multiplier, adder, multiplier-accumulator, etc.
PLL	Analog PLL, digital PLL

3. Special I/O interface macros

• T-LVTTL	• SSTL	• HSTL	• P-CML
• LVDS	• PCI	• AGP	• USB
• IEEE1394			

■ CHIP STRUCTURE

The chip layout of the CE81 series consists of two major areas : chip peripheral area and basic cell area.

The chip peripheral area contains the input/output buffer cells for interfacing with external devices and the associated bonding pads. The basic cell area contains some of input/output buffer cells, the unit cells and the compiled cells.

• Chip configuration

Bonding pad

I/O buffer cell

Basic cell area
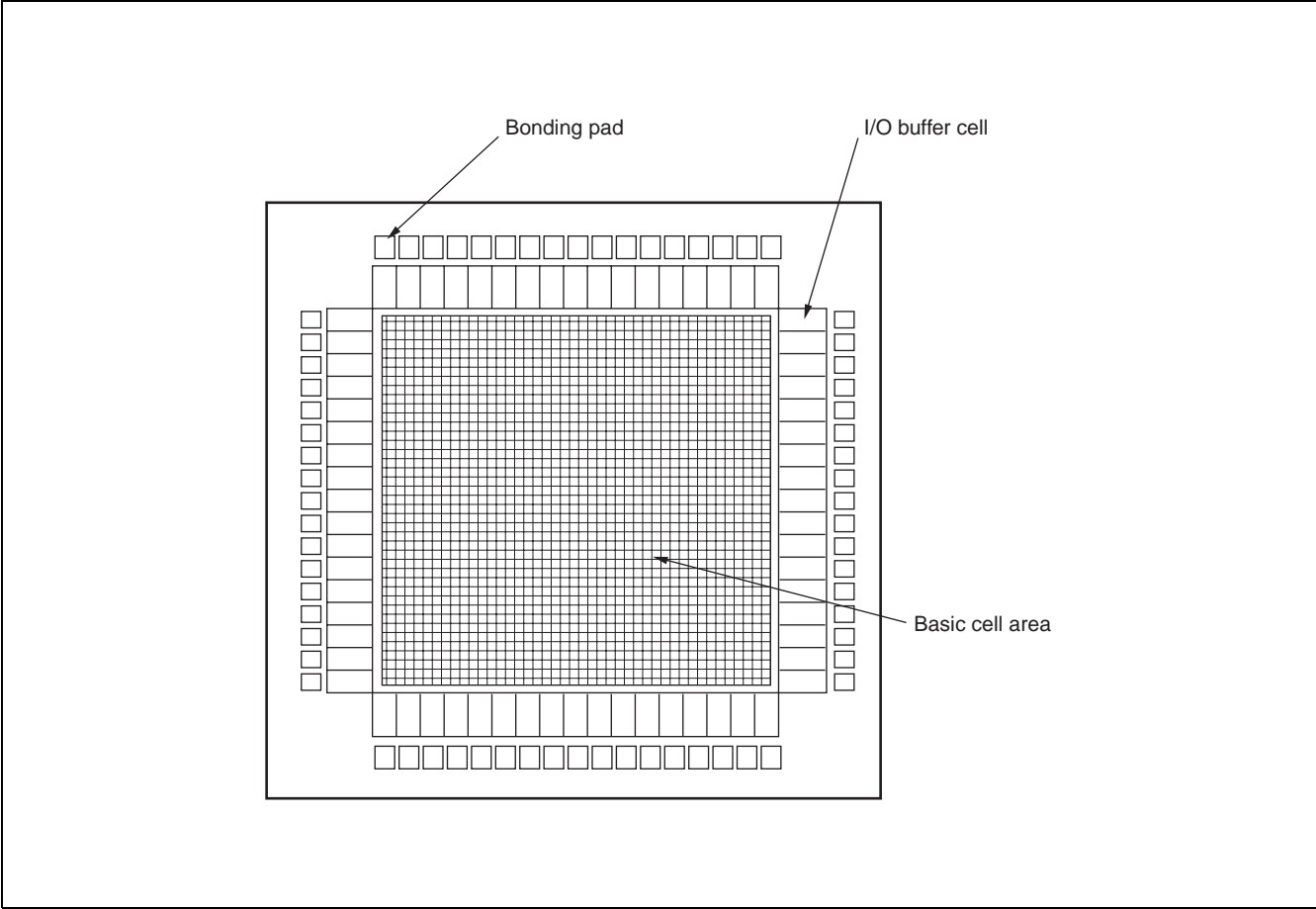
■ COMPILED CELLS

Compiled cells are macro cells which are automatically generated with the bit/word configuration specified. The CE81 series has the following types of compiled cells (Note that each macro is different in word/bit range depending on the column type) .

1. Clock synchronous single-port RAM (1 address : 1 RW)

• High density/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	Bit
16	64 to 72 K	64 to 4 K	1 to 18	Bit

• High speed type

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 144 K	64 to 2 K	4 to 72	Bit

• Large scale partial write type

Column type	Memory capacity	Word range	Bit range	Unit
16	24.5 K to 1179 K	4 to 16 K	6 to 72	Bit

2. Clock synchronous dual-port RAM (2 addresses : 1 RW, 1 R)

• High density/Partial write type

Column type	Memory capacity	Word range	Bit range	Unit
4	16 to 72 K	16 to 1 K	1 to 72	Bit
16	64 to 72 K	64 to 4 K	1 to 18	Bit

3. Clock synchronous register file (3 addresses : 1 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64	1 to 72	Bit

4. Clock synchronous register file (4 addresses : 2 W, 2 R)

Column type	Memory capacity	Word range	Bit range	Unit
1	4608	4 to 64 K	1 to 72	Bit

5. Clock synchronous ROM (1 addresses : 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
16	256 to 512 K	128 to 4 K	2 to 128	Bit

6. Clock synchronous delay line memory (2 addresses : 1 W, 1 R)

Column type	Memory capacity	Word range	Bit range	Unit
8	256 to 32 K	32 to 1 K	8 to 32	Bit
16	384 to 32 K	64 to 2 K	6 to 16	Bit
32	512 to 32 K	128 to 4 K	4 to 8	Bit

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply voltage*1	V_{DD}	−0.5	+2.5 *2	V
			+4.0 *3	
Input voltage*1	V_I	−0.5	V_{DD}+0.5 (≤ 2.5 V) *2	V
			V_{DD}+0.5 (≤ 4.0 V) *3	
Output voltage*1	V_O	−0.5	V_{DD}+0.5 (≤ 2.5 V) *2	V
			V_{DD}+0.5 (≤ 4.0 V) *3	
Storage temperature	Tst	−55	+125	°C
Junction temperature	T_j	−40	+125	°C
Output current *4	I_O	—	±4	mA
Input signal transmitting rate	R_I	—	Clock Input *5 : 200 Normal Input : 100	Mbps *6
Output signal transmitting rate	R_O	—	100	Mbps *6
Output load capacitance	C_O	—	3000/R_O	pF
Continuous time of indefinite input signal	tz	—	10	ms
Supply pin current	I_D	—	*7	mA

*1 : The parameter is based on V_{SS} = 0 V.

*2 : Internal gate part in case of signal power supply or dual power supply

*3 : I/O part in case 3.3 V I/F or 2.5 V I/F is used by dual power supply

*4 : DC current which continues more than 10 ms, or average DC current

*5 : In case of using I/O cell for clock input

*6 : bps = bit per second

*7 : Supply pin current for one V_{DD}/GND pin

Frame	Source type	Maximum current [mA]		Number of layer
		Standard source	Additional source	
YS/S, YI/I	V_{DDE}, V_{DDI}, V_{DD}, V_{SS}	68	68	4, 5
	V_{DDE}	39	39	3
	V_{DDI}, V_{DD}, V_{SS}	68	68	
A	V_{DDE}, V_{DDI}, V_{DD}, V_{SS}	34	34	—
B	V_{DDE}, V_{DDI}, V_{DD}, V_{SS}	43	30	—

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• **Single power supply** ($V_{DD} = +1.8\ V \pm 0.15\ V$)

($V_{SS} = 0\ V$)

Parameter	Symbol	Value			Unit
		Min	**Typ**	**Max**	
Supply voltage (1.8 V supply voltage)	V_{DD}	1.65	1.8	1.95	V
"H" level input voltage (1.8 V CMOS)	V_{IH}	$V_{DD} \times 0.65$	—	$V_{DD} + 0.3$	V
"L" level input voltage (1.8 V CMOS)	V_{IL}	–0.3	—	$V_{DD} \times 0.35$	V
Junction temperature	T_j	–40	—	+125	°C

• **Dual power supply** ($V_{DDE} = +3.3\ V \pm 0.3\ V$, $V_{DDI} = +1.8\ V \pm 0.15\ V$)

($V_{SS} = 0\ V$)

Parameter		Symbol	Value			Unit
			Min	**Typ**	**Max**	
Supply voltage	1.8 V supply voltage	V_{DDI}	1.65	1.8	1.95	V
	3.3 V supply voltage	V_{DDE}	3.0	3.3	3.6	
"H" level input voltage	1.8 V CMOS	V_{IH}	$V_{DD} \times 0.65$	—	$V_{DDI} + 0.3$	V
	3.3 V CMOS		2.0	—	$V_{DDE} + 0.3$	
"L" level input voltage	1.8 V CMOS	V_{IL}	–0.3	—	$V_{DD} \times 0.35$	V
	3.3 V CMOS		–0.3	—	+0.8	
Junction temperature		T_j	–40	—	+125	°C

• **Dual power supply** ($V_{DDE} = +3.3\ V \pm 0.3\ V$, $V_{DDI} = +1.5\ V \pm 0.1\ V$ / $+1.1\ V \pm 0.1\ V$)

($V_{SS} = 0\ V$)

Parameter		Symbol	Value			Unit
			Min	**Typ**	**Max**	
Supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	1.0	1.1	1.2	V
			1.4	1.5	1.6	V
"H" level input voltage	3.3 V CMOS	V_{IH}	2.0	—	$V_{DDE} + 0.3$	V
"L" level input voltage	3.3 V CMOS	V_{IL}	–0.3	—	+0.8	V
Junction temperature		T_j	–40	—	+125	°C

• **Dual power supply** (**V$_{DDE}$ = + 2.5 V ± 0.2 V, V$_{DDI}$ = + 1.8 V ± 0.15 V**)

(V$_{SS}$ = 0 V)

Parameter		Symbol	Value			Unit
			Min	**Typ**	**Max**	
Supply voltage		V$_{DDE}$	2.3	2.5	2.7	V
		V$_{DDI}$	1.65	1.8	1.95	V
"H" level input voltage	1.8 V CMOS	V$_{IH}$	V$_{DDI}$ × 0.65	—	V$_{DDI}$ + 0.3	V
	2.5 V CMOS		1.7	—	V$_{DDE}$ + 0.3	V
"L" level input voltage	1.8 V CMOS	V$_{IL}$	–0.3	—	V$_{DDI}$ × 0.35	V
	2.5 V CMOS		–0.3	—	+0.7	V
Junction temperature		T$_j$	–40	—	+125	°C

• **Dual power supply** (**V$_{DDE}$ = + 2.5 V ± 0.2 V, V$_{DDI}$ = + 1.5 V ± 0.1 V / + 1.1 V ± 0.1 V**)

(V$_{SS}$ = 0 V)

Parameter		Symbol	Value			Unit
			Min	**Typ**	**Max**	
Supply voltage		V$_{DDE}$	2.3	2.5	2.7	V
		V$_{DDI}$	1.0	1.1	1.2	V
			1.4	1.5	1.6	V
"H" level input voltage	2.5 V CMOS	V$_{IH}$	1.7	—	V$_{DDE}$ + 0.3	V
"L" level input voltage	2.5 V CMOS	V$_{IL}$	–0.3	—	+0.7	V
Junction temperature		T$_j$	–40	—	+125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

• **Static supply current (single power supply/Dual power supply)**

A frame

Frame	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE
CATLG value [mA]	0.5	0.7	1	1.4	2	2.6	3.3	4	4.6	5.3	6.6

S frame

Frame	SA	SB	SC	SD	SE	SF	SG
CATLG value [mA]	3.7	4.4	5	5.8	7.1	9.2	10.9

I frame

Frame	I1	I2	I3	I4	I5	I6	I7	I8	I9	IA
CATLG value [mA]	0.3	0.4	0.6	0.7	0.8	1.2	1.5	2	2.8	3.4

Note : When the memory is in a standby mode and analog macro is in a power-down mode. At both cases, conditions are $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, and $T_j = +25\ °C$. The above values may not be guaranteed when the input buffer with a pull-up/pull-down resister or a crystal oscillator buffer is used.
The above values may not be guaranteed when a High-speed cell library is used.

• **Single power supply** : V_{DD} = **1.8 V**

(V_{DD} = 1.8 V ± 0.15 V, V_{SS} = 0 V, T_j = −40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply current	I_{DDS}	—	—	—	*	mA
"H" level output voltage	V_{OH}	$I_{OH} = -100\ \mu A$	$V_{DD} - 0.2$	—	V_{DD}	V
"L" level output voltage	V_{OL}	$I_{OL} = 100\ \mu A$	0	—	0.2	V
"H" level output V-I characteristics	—	$V_{DD} = 1.8\ V \pm 0.15\ V$	—	—	—	—
"L" level output V-I characteristics	—	$V_{DD} = 1.8\ V \pm 0.15\ V$	—	—	—	—
Input leakage current	I_L	—	—	—	±5	μA
Pull-up/pull-down resistance	R_P	Pull-up $V_{IL} = 0$ Pull-down $V_{IH} = V_{DD}$	—	18	—	kΩ

* : Refer to the table on the previous page "Static supply current (single power supply/Dual power supply) ".

- **Dual power supply** : V_{DDE} = **3.3 V, V_{DDI}** = **1.8 V** / **1.5 V** / **1.1 V**
  (V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.8 V ± 0.15 V / 1.5 V ± 0.1 V / 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = −40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply current	I_{DDS}	—	—	—	*1	mA
"H" level output voltage	V_{OH4}	3.3 V output I_{OH} = −100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V output I_{OH} = −100 µA	V_{DDI} − 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL4}	3.3 V output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V output I_{OL} = 100 µA	0	—	0.2	V
"H" level output V-I characteristics	—	3.3 V V_{DDE} = 3.3 V±0.3 V	*2			—
		1.8 V V_{DDI} = 1.8 V±0.15 V	—			—
"L" level output V-I characteristics	I_{OL}	3.3 V V_{DDE} = 3.3 V±0.3 V	*2			—
		1.8 V V_{DDE} = 1.8 V±0.15 V	—			—
Input leakage current	I_L	—	—	—	±5	µA
Pull-up/pull-down resistance	R_P	1.8 V Pull up V_{IL} = 0 Pull down V_{IH} = V_{DDI}	—	18	—	kΩ
		3.3 V Pull up V_{IL} = 0 Pull down V_{IH} = V_{DDE}	10	33	80	

*1 : Refer to the table on the previous page "Static supply current (single power supply/Dual power supply) ".

*2 : Refer to the "• V-I Characteristics" Fig. 1, Fig. 2.

- **Dual power supply** : V_{DDE} = **2.5 V**, V_{DDI} = **1.8 V** / **1.5 V** / **1.1 V**
  (V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.8 V ± 0.15 V / 1.5 V ± 0.1 V / 1.1 V ± 0.1 V, V_{SS} = 0 V, T_j = −40 °C to +125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Supply current	I_{DDS}	—	—	—	*	mA
"H" level output voltage	V_{OH3}	2.5 V output I_{OH} = −100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
	V_{OH2}	1.8 V output I_{OH} = −100 µA	V_{DDI} − 0.2	—	V_{DDI}	V
"L" level output voltage	V_{OL3}	2.5 V output I_{OL} = 100 µA	0	—	0.2	V
	V_{OL2}	1.8 V output I_{OL} = 100 µA	0	—	0.2	V
"H" level output V-I characteristics	I_{OH}	2.5 V V_{DDE} = 2.5 V±0.2 V		—		—
		1.8 V V_{DDI} = 1.8 V±0.15 V		—		—
"L" level output V-I characteristics	I_{OL}	2.5 V V_{DDE} = 2.5 V±0.2 V		—		—
		1.8 V V_{DDI} = 1.8 V±0.15 V		—		—
Input leakage current	I_L	—	—	—	±5	µA
Pull-up/pull-down resistance	R_P	1.8 V Pull up V_{IL} = 0 Pull down V_{IH} = V_{DDI}	—	18	—	kΩ
		2.5 V Pull up V_{IL} = 0 Pull down V_{IH} = V_{DDE}	—	25	—	

* : Refer to the table on the previous page "Static supply current (single power supply/Dual power supply) ".

- **V-I Characteristics**

Min : Process = Slow, $T_j = +125\ °C$, $V_{DD} = 3.6\ V$
Typ : Process = Typical, $T_j = +25\ °C$, $V_{DD} = 3.3\ V$
Max : Process = Fast, $T_j = -40\ °C$, $V_{DD} = 3.0\ V$
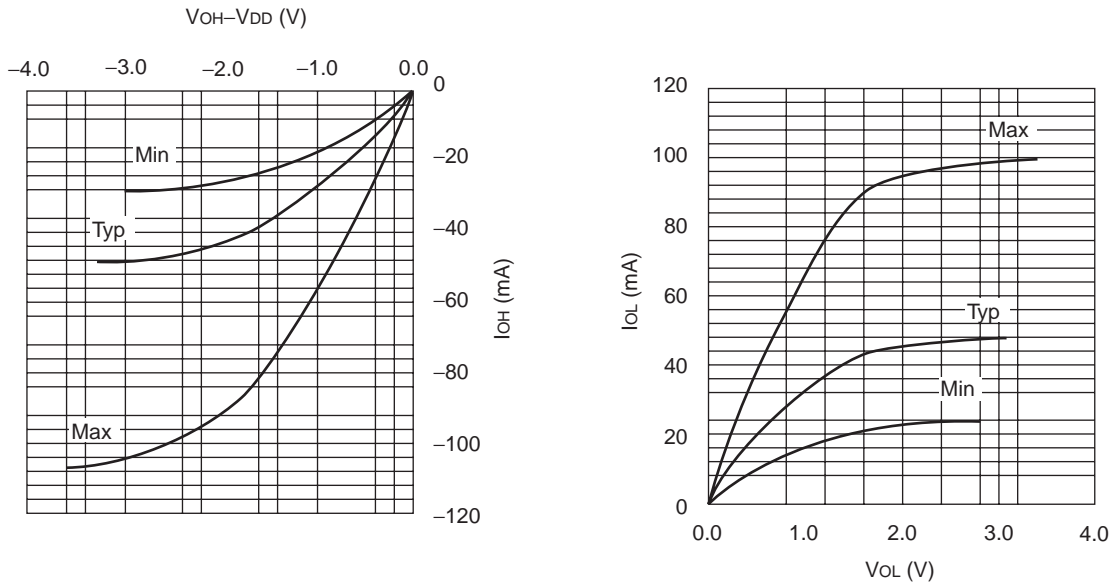
Fig.1 V-I characteristics (3.3 V normal I/O L, M type)

Min : Process = Slow, $T_j = +125\ °C$, $V_{DD} = 3.6\ V$
Typ : Process = Typical, $T_j = +25\ °C$, $V_{DD} = 3.3\ V$
Max : Process = Fast, $T_j = -40\ °C$, $V_{DD} = 3.0\ V$
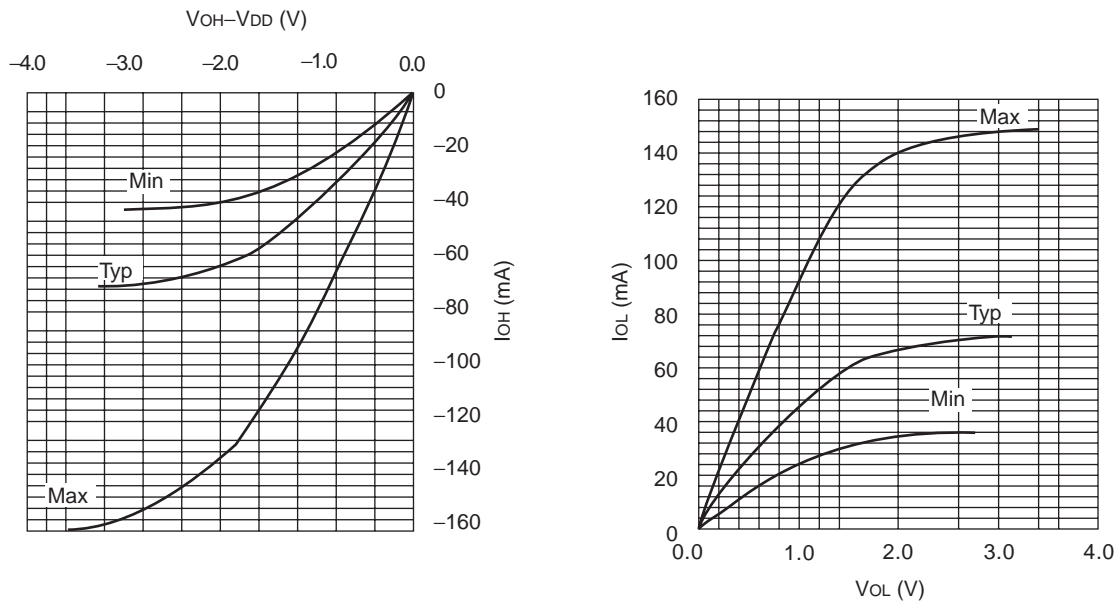
Fig.2 V-I characteristics (3.3 V normal I/O H, V type)

2. AC Characteristics

$(V_{DD} = 1.8\ V \pm 0.15\ V,\ V_{SS} = 0\ V,\ T_j = -40\ °C\ to\ +125\ °C)$

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Delay time	t_{pd}[*1]	typ[*2] × tmin[*3]	typ[*2] × ttyp[*3]	typ[*2] × tmax[*3]	ns

*1 : Delay time = propagation delay time, Enable time, Disable time

*2 : "typ" is calculated based on the cell specification.

*3 : Measurement conditions.

Measurement condition	tmin	ttyp	tmax
$V_{DD} = 2.5\ V \pm 0.2\ V,\ V_{SS} = 0\ V,\ T_j = -40\ °C\ to\ +125\ °C$	0.60	1.00	1.64
$V_{DD} = 1.8\ V \pm 0.15\ V,\ V_{SS} = 0\ V,\ T_j = -40\ °C\ to\ +125\ °C$	0.84	1.57	2.84
$V_{DD} = 1.5\ V \pm 0.1\ V,\ V_{SS} = 0\ V,\ T_j = -40\ °C\ to\ +125\ °C$	1.14	2.22	4.09

Note : $t_{pd\ max}$ is calculated according to the maximum junction temperature (T_j) .

■ INPUT/OUTPUT PIN CAPACITANCE

$(f = 1\ MHz,\ V_{DD} = V_I = 0\ V,\ Ta = +25\ °C)$

Parameter	Symbol	Value	Unit
Input pin	C_{IN}	Max 16	pF
Output pin	C_{OUT}	Max 16	pF
I/O pin	$C_{I/O}$	Max 16	pF

Note : Capacitance varies according to the package and the location of the pin.

■ DESIGN METHOD

Linking a floor plan tool and a logic synthesis tool enables automatic circuit optimization using floor plan information. In addition, also available are CDDM (Clock Driven Design Method) clock tree synthesis tools using floor plan information. Using floor plan information at a pre-layout stage prevents major problems with setup and hold timings which can occur after layout. Using a hierarchical layout method to support larger-scale circuit design considerably shortens the overall design cycle time.

■ PACKAGES

The table below lists the package types available and the reference number of gates used.

Consult Fujitsu for the combination of each package and the availability.

• Number of gates used and package types

Package & Pin Count		Pin Pitch (mm)	Number of gates used (0 – 20000k)
T A B - B G A	304	0.80	891k
	352	0.80	1254k
	480	1.00	1905k
	560	1.00	2689k
	660	1.00	3609k
	720	1.00	9129k
E B G A	576	1.27	5982k
	660	1.00	12727k
	672	1.27	7952k
H Q F P	208	0.50	1098k
	240	0.50	2085k
	256	0.40	3764k
	304	0.50	4712k
	304	0.50	15158k
T Q F P	100	0.50	514k
	120	0.40	514k
L Q F P	144	0.50	722k
	176	0.50	963k
	208	0.50	1098k
F B G A	112	0.80	514k
	176	0.80	722k
	192	0.80	1098k
	240	0.50	2697k
	272	0.80	1550k
	288	0.75	2697k

Note : The packages that can be used depend on the circuit configuration. For details, contact Fujitsu.

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