1.36-W Mono Fully Differential Audio Power Amplifier

DESCRIPTION

The EUA6204 is a mono fully-differential audio amplifier, capable of delivering 1.36W of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a 5V power supply, and 720mW to a 8Ω load from a 3.6V power supply.

The EUA6204 is ideal for PDA/smart phone application due to features such as -80-dB supply voltage rejection from 20Ha to 2kHz, improved RF rectification immunity, small 20mm^2 PCB area, and a fast startup with minimal pop.

The EUA6204 is available in a MSOP-8 and in the space-saving 3mm × 3mm DFN package.

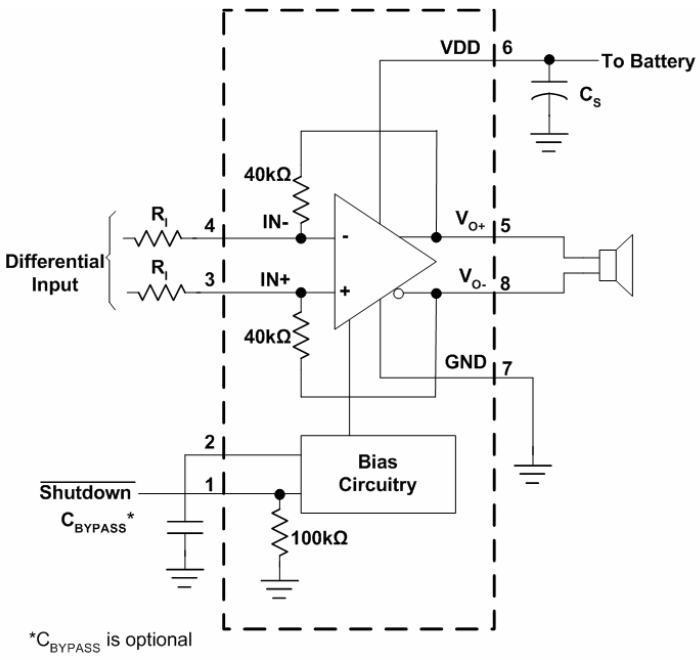
FEATURES

- Supply Voltage 2.5V to 5.5V
- 1.36W into 8Ω from a 5-V Supply at THD=1% (typ)
- Low Supply Current: 4mA typ at 5V
- Shutdown Current: 0.01μA typ
- Fast Startup with Minimal Pop
- Only Three External Components
  - Improved PSRR (-80dB) for Direct Battery Operation
  - Full Differential Design Reduces RF Rectification
  - -63dB CMRR Eliminates Two Input Coupling Capacitors
- RoHS Compliant and 100% Lead (Pb)-Free

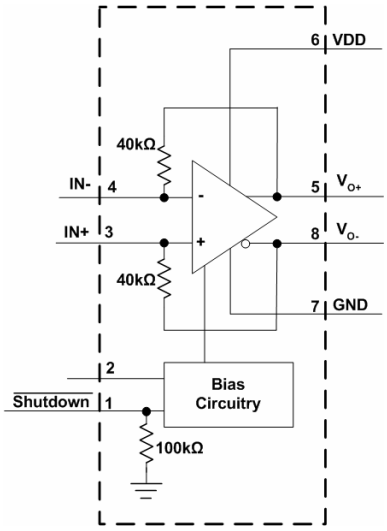
APPLICATIONS

- Wireless Handsets
- PDAs
- Portable Devices

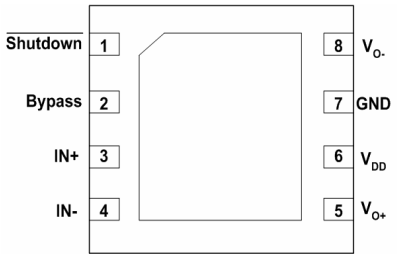
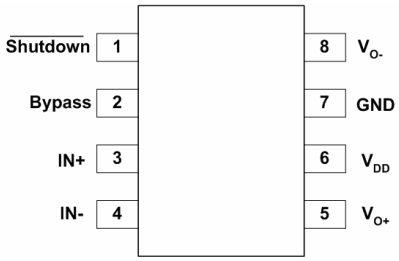
Typical Application Circuit



Block Diagram



Pin Configurations

Package	Pin Configurations
DFN-8	
MSOP-8	

Pin Description

SYMBOL	PIN	DESCRIPTION
$\overline{\text{Shutdown}}$	1	Shutdown terminal
Bypass	2	Mid-supply voltage, adding a bypass capacitor improves PSRR
IN+	3	Positive differential input
IN-	4	Negative differential input
VO+	5	Positive BTL output
VDD	6	Power supply
GND	7	High-current ground
VO-	8	Negative BTL output

Ordering Information

Order Number	Package Type	Marking	Operating Temperature range
EUA6204JIR1	DFN-8	xxxx A6204	-40°C to 85°C
EUA6204MIR1	MSOP-8	xxxx A6204	-40°C to 85°C

EUA6204 □ □ □ □

Lead Free Code
1: Lead Free 0: Lead

Packing
R: Tape & Reel

Operating temperature range
I: Industry Standard

Package Type
J: DFN
M: MSOP

Absolute Maximum Ratings

- Supply voltage, V_{DD} ---------- 6V
- Input voltage, V_I ---------- -0.3 V to V_{DD} +0.3V
- Storage temperature rang, T_{stg} ---------- -65°C to 150°C
- ESD Susceptibility ---------- 2kV
- Junction Temperature ---------- 150°C
- Thermal Resistance

  θ_{JC} (MSOP) ---------- 56°C/W

  θ_{JA} (MSOP) ---------- 160°C/W

  θ_{JA} (DFN) ---------- 50°C/W

Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}	2.5		5.5	V
High-level input voltage, V_{IH}	1.55			V
Low-level input voltage, V_{IL}			0.5	
Operating free-air temperature, T_A	-40		85	°C

Electrical Characteristics, T_A=25°C

Symbol	Parameter	Conditions		EUA6204 Min	EUA6204 Typ	EUA6204 Max.	Unit
V_{OS}	Output offset voltage (measured differentially)	V_I=0V differential, Gain=1V/V, V_{DD}=5.5V		-9	2	9	mV
PSRR	Power supply rejection ratio	V_{DD}=2.5V to 5.5V			-85	-60	dB
V_{IC}	Common mode input range	V_{DD}=2.5V to 5.5V		0.5		V_{DD}-0.8	V
CMRR	Common mode rejection range	V_{DD}=2.5V, V_{IC}=0.5V to 1.7V			-63	-40	dB
		V_{DD}=5.5V, V_{IC}=0.5V to 4.7V			-63	-40	
	Low-output swing	R_L=8Ω, Gain=1V/V, V_{IN+}=V_{DD}, V_{IN-}=0V or V_{IN+}=0V, V_{IN-}=V_{DD}	V_{DD}=5.5V		0.45		V
			V_{DD}=3.6V		0.37		
			V_{DD}=2.5V		0.26	0.4	
	High-output swing	R_L=8Ω, Gain=1V/V, V_{IN+}=V_{DD}, V_{IN-}=0V or V_{IN-}=V_{DD}, V_{IN+}=0V	V_{DD}=5.5V		4.95		V
			V_{DD}=3.6V		3.18		
			V_{DD}=2.5V	2	2.13		
$\lvert I_{IH}\rvert$	High-level input current, $\overline{\text{Shutdown}}$	V_{DD}=5.5V, V_I=5.8V			58	100	µA
$\lvert I_{IL}\rvert$	Low-level input current, $\overline{\text{Shutdown}}$	V_{DD}=5.5V, V_I=-0.3V			3	100	µA
I_Q	Quiescent current	V_{DD}=2.5V to 5.5V, no load			4	8	mA
$I_{(SD)}$	Supply current	V($\overline{\text{Shutdown}}$)≤0.5V, V_{DD}=2.5V to 5.5V, R_L= 8Ω			0.01	1	µA
	Gain	R_L= 8Ω		$\frac{38k\Omega}{RI}$	$\frac{40k\Omega}{RI}$	$\frac{42k\Omega}{RI}$	V/V
	Resistance from shutdown to GND				100		kΩ

Operating Characteristics, T_A=25°C, Gain=1V/V

Symbol	Parameter	Conditions		EUA6204			Unit
				Min	Typ	Max.	
P_O	Output power	THD+N=1%, f=1kHz,R_L=8Ω	V_{DD}=5V		1.36		W
			V_{DD}=3.6V		0.72		
			V_{DD}=2.5V		0.33		
		THD+N=10%, f=1kHz,R_L=8Ω	V_{DD}=5V		1.7		W
			V_{DD}=3.6V		0.85		
			V_{DD}=2.5V		0.4		
THD+N	Total harmonic distortion plus noise	V_{DD}=5V, P_O=1W, R_L=8Ω, f=1kHz			0.15		%
		V_{DD}=3.6V, P_O=0.5W, R_L=8Ω, f=1kHz			0.1		
		V_{DD}=2.5V, P_O=200mW, R_L=8Ω, f=1kHz			0.1		
K_{SVR}	Supply ripple rejection ratio	V_{DD}=3.6V, Inputs ac-grounded with C_i=2µF, $V_{(Ripple)}$=200mVpp	f = 217Hz		-77		dB
			f=20Hz to 20kHz		-60		
SNR	Signal-to-noise ratio	V_{DD}=5V, P_O=1W, R_L=8Ω			100		dB
Vn	Output voltage noise	V_{DD}=3.6V, f=20Hz to 20kHz, Inputs ac-grounded with C_i=2µF	No weighting		25		μV_{RMS}
			A weighting		19		
CMRR	Common mode rejection ratio	V_{DD}=3.6V V_{IC}=1Vpp	f=217Hz		-64		dB
R_F	Feedback resistance			38	40	44	kΩ
	Start-up time from shutdown	V_{DD}=3.6V, C_{BYPASS}=0.1µF			27		ms

Typical Operating Characteristics

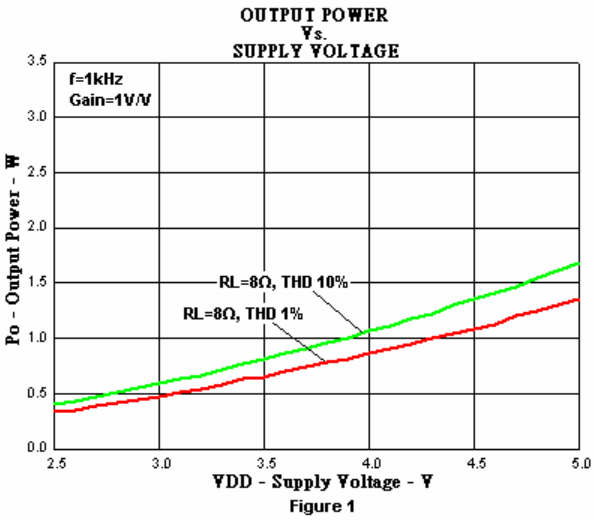


Figure 1

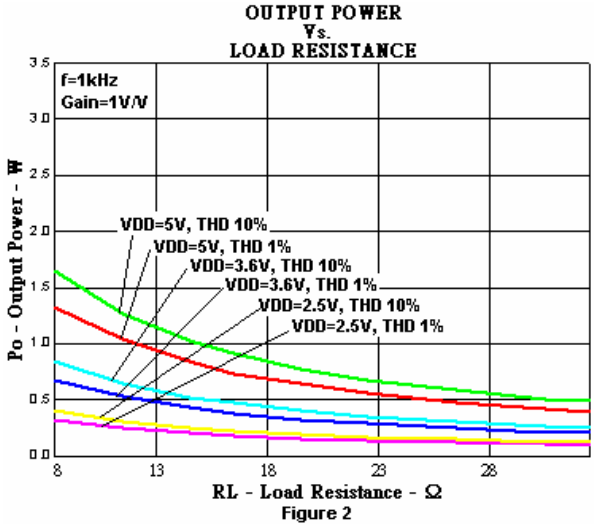


Figure 2

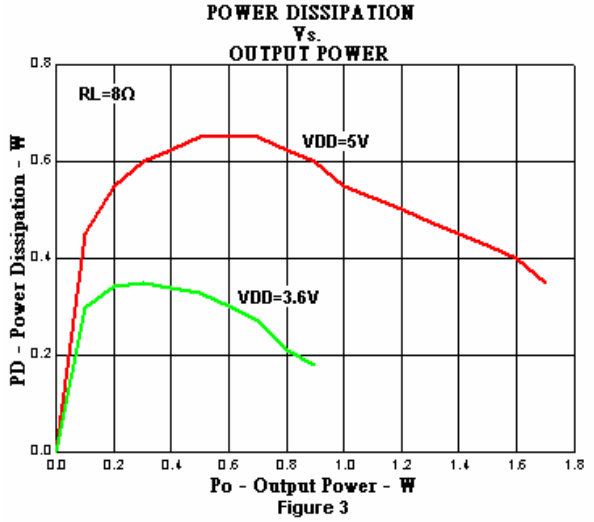


Figure 3

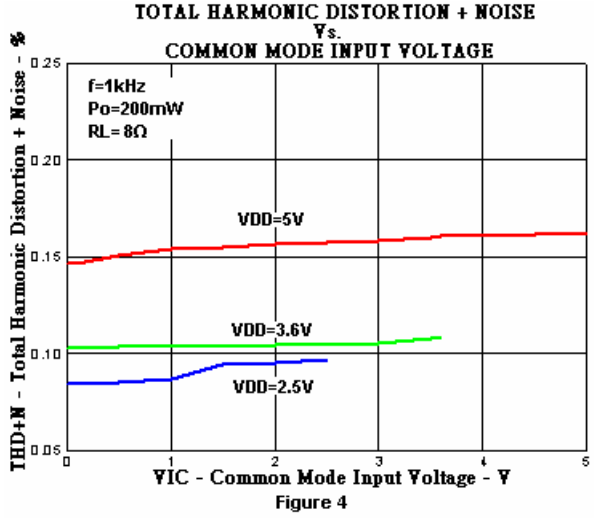


Figure 4

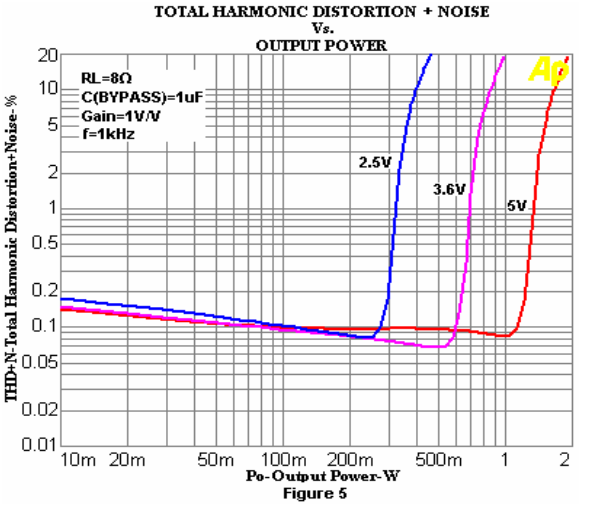


Figure 5

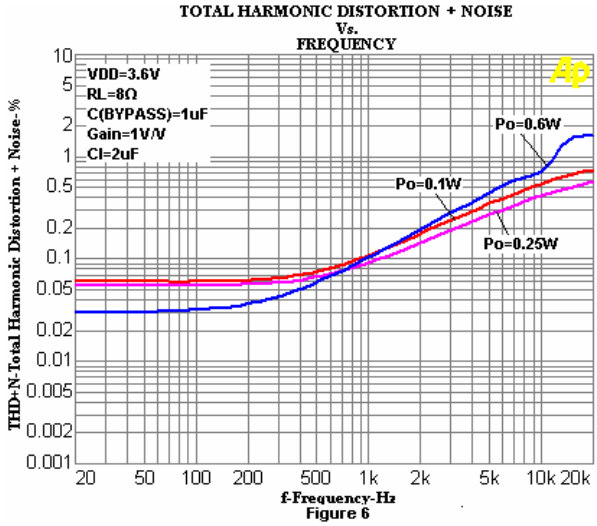


Figure 6

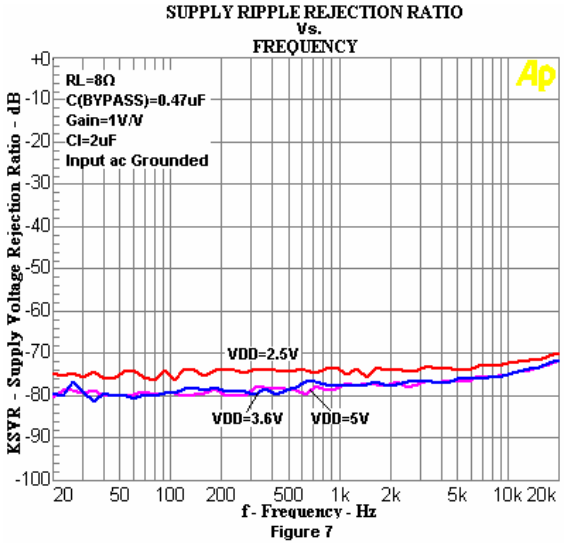


Figure 7

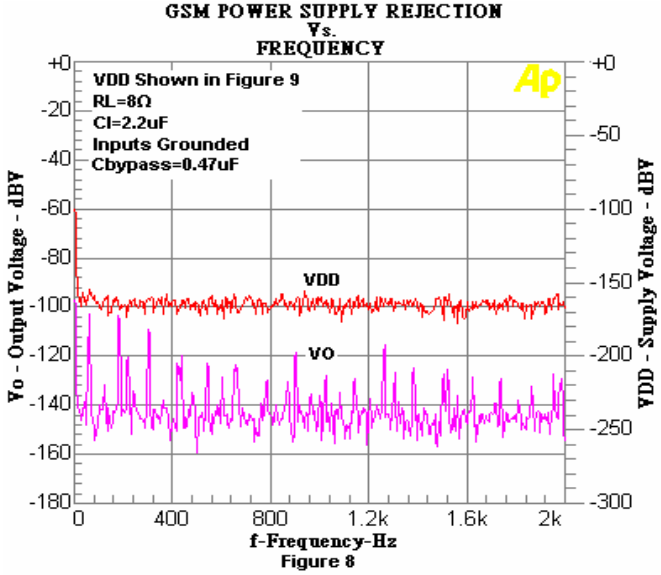


Figure 8

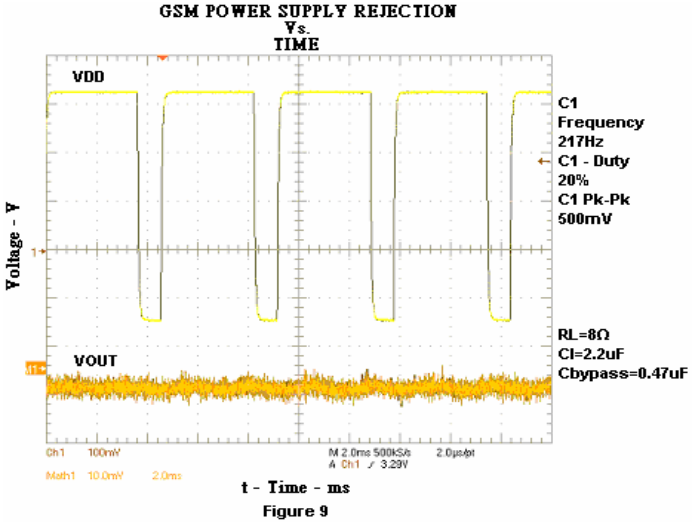


Figure 9

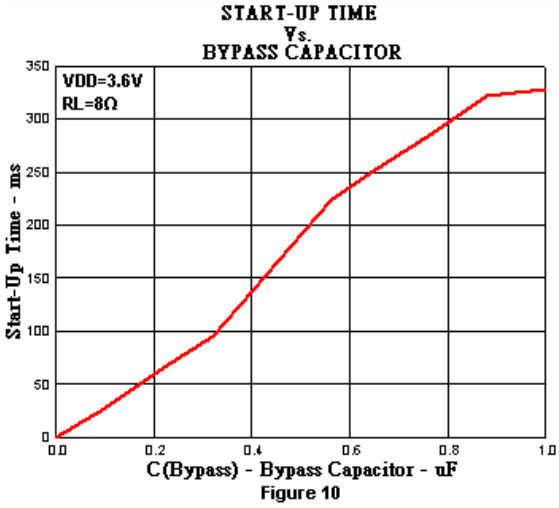


Figure 10

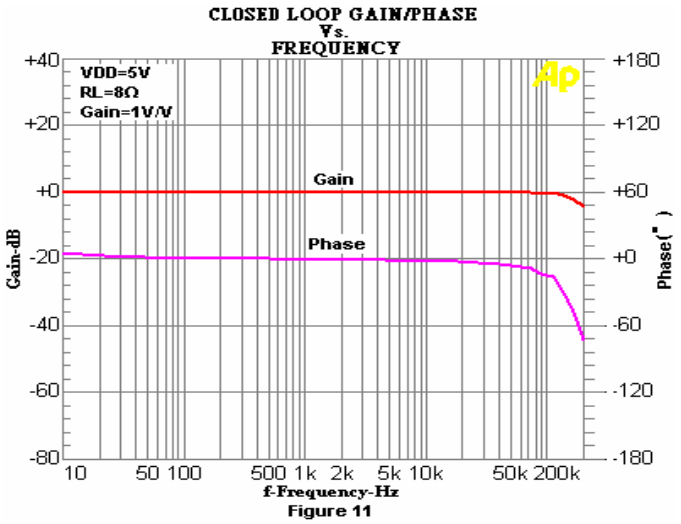


Figure 11

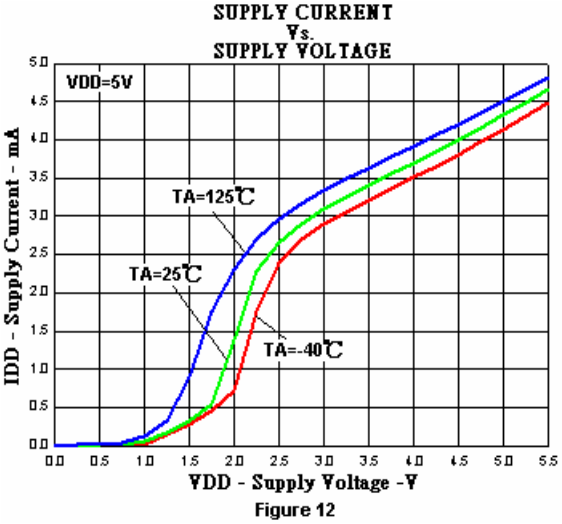
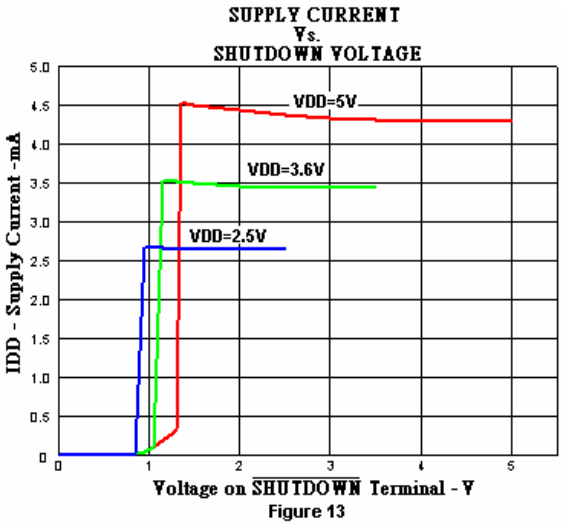


Figure 12


SUPPLY CURRENT
Vs.
SHUTDOWN VOLTAGE
IDD - Supply Current -mA
VDD=5V
VDD=3.6V
VDD=2.5V
Voltage on SHUTDOWN Terminal - V
0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
1
2
3
4
5
Figure 13

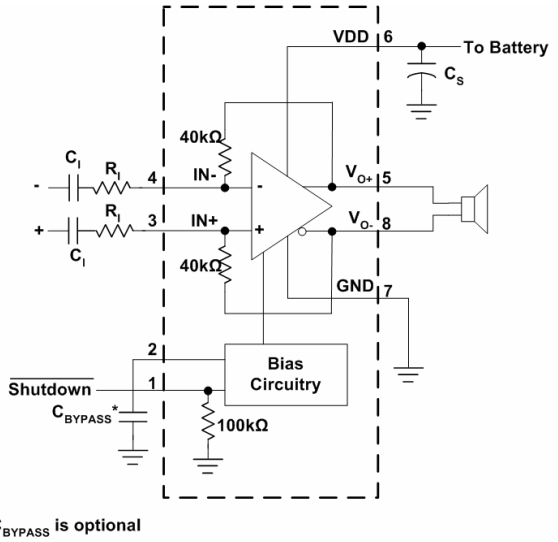
Application Information

Application Schematics

Figure14 through Figure15 show application schematics for differential and single-ended inputs. Typical values are shown in Table1.

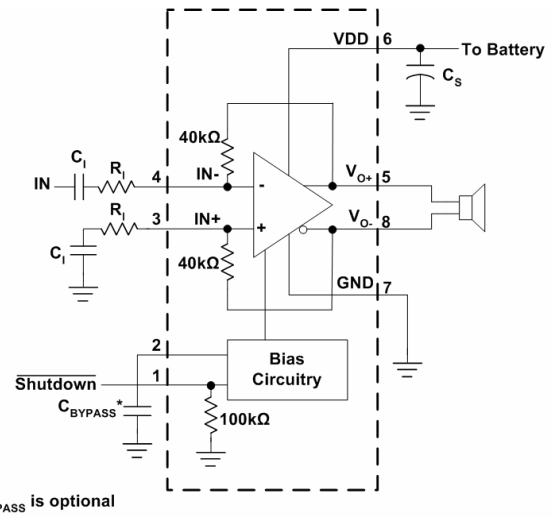
Table1. Typical Component Value

Component	Value
R_I	40kΩ
$C_{(BYPASS)}$	0.22μF
C_S	1μF
C_I	0.22μF



*C_{BYPASS} is optional

Figure14. Differential Input Application Schematic Optimized with Input Capacitors



*C_{BYPASS} is optional

** Due to the fully differential design of this amplifier, the performance is severly degraded if you connect the unused input to BYPASS when using single-ended inputs

Figure15. Single-Ended Input Application Schematic

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the EUA6204 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs of from equation1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \text{ ----------(1)}$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. T_{JMAX} can be determine from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the EUA6204. If T_{JMAX} still exceeds 150°C, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power.

Proper Selection of External Components

Gain-Setting Resistor Selection

The input resistor (R_I) can be selected to set the gain of the amplifier according to equation2.

$$Gain=R_F/R_I \quad (2)$$

The internal feedback resistors (R_F) are trimmed to 40kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

Bypass Capacitor (C_{BYPASS}) and Start-up Time

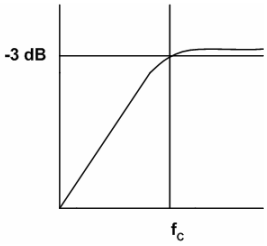
The internal voltage divider at the Bypass pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor to this pin filters any noise into this pin and increases k_{SVR}. $C_{(BYPASS)}$ also determines the rise time of V_{O+} and V_{O-} when the device is taken out of shutdown. The larger the capacitor, the slower the rise time. Show the relationship of $C_{(BYPASS)}$ to start-up time as Figure10.

Input Capacitor (C_I)

The EUA6204 does not require input coupling capacitors if using a differential input source that is biased from 0.5V to V_{DD} -0.8V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation3.

$$f_C = \frac{1}{2\pi R_I C_I} \quad (3)$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit.

Consider the example where R_I is 10kΩ and the specification calls for a flat bass response down to 100Hz. Equation 3 is reconfigured as equation4.

$$C_I = \frac{1}{2\pi R_I f_C} \quad (4)$$

In this example, C_I is 0.16μF, so one would likely choose a value in the range of 0.22μF to 0.47μF.

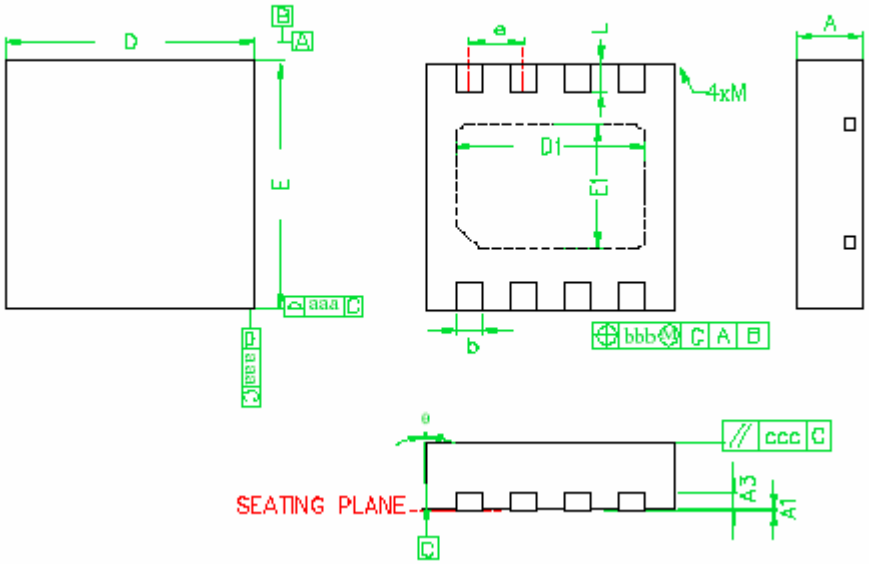
Ceramic capacitors should be used when possible, as they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (C_S)

The EUA6204 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF to 1 μF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

Package Information

DFN-8

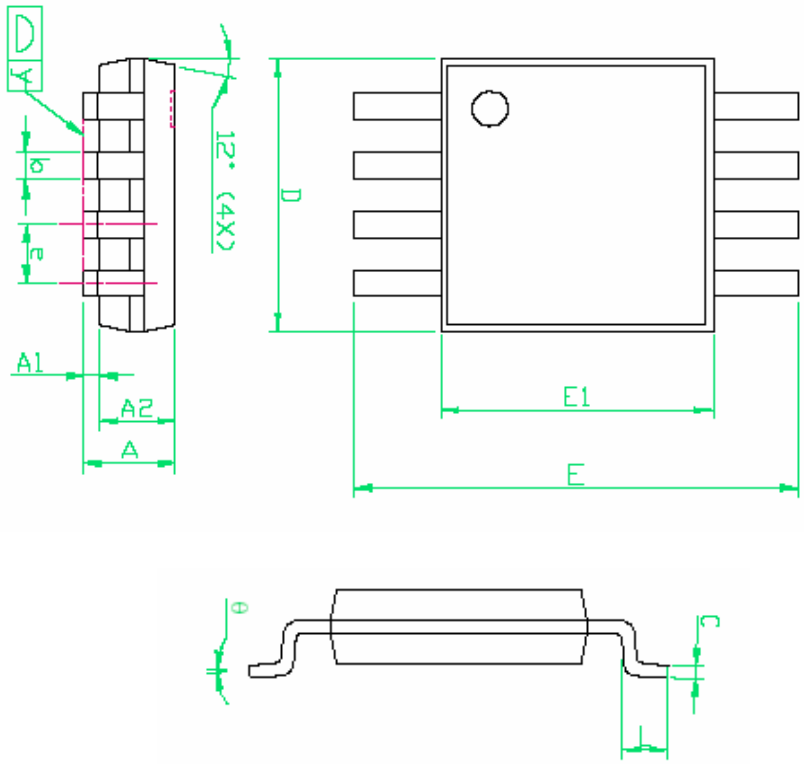


NOTE

1. All dimensions are in millimeters, θ is in degrees
2. M: The maximum allowable corner on the molded plastic body corner
3. Dimension D does not include mold protrusions or gate burrs. Mold protrusions and gate burrs shall not exceed 0.15mm per side
4. Dimension E does not include interterminal mold protrusions or terminal protrusions. Interminal mold protrusions and/or terminal protrusions shall not exceed 0.20mm per side
5. Dimension b applies to plated terminals. Dimension A1 is primarily Y terminal plating, but may or may not include a small protrusion of terminal below the bottom surface of the package
6. Burr shall not exceed 0.060mm
7. JEDEC MO-229

SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.81	0.9	1.00
A1	0	0.015	0.03
A3	------	0.20 REF	------
B	0.25	0.30	0.37
D	2.85	3.00 BSC	3.15
D1	------	2.3 BSC	------
E	2.85	3.00 BSC	3.15
E1	------	1.5 BSC	------
e	------	0.65 BSC	-----
L	0.25	0.35	0.45
aaa	------	0.25	------
bbb	------	0.10	------
ccc	------	0.10	------
M	------	------	0.05
θ	-12	------	0

MSOP-8



NOTE

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless otherwise specified
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.81	0.95	1.10	0.032	0.0375	0.043
A1	0.05	0.09	0.15	0.002	0.004	0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.70	4.90	5.10	0.185	0.193	0.201
E1	2.90	3.00	3.10	0.114	0.118	0.122
e	------	0.65	-----	------	0.026	------
L	0.40	0.53	0.66	0.016	0.021	0.026
y	------	------	0.10	------	------	0.004
θ	0	------	6	0	------	6