Genesys Logic, Inc.

GL817E

USB 2.0
MS/ MS PRO/ SD/ MMC
Controller

Datasheet
Revision 1.38
Apr. 19, 2006

Copyright:

Disclaimer:

ALL MATERIALS ARE PROVIDED "AS IS" WITHOUT EXPRESS OR IMPLIED WARRANTY OF ANY KIND. NO LICENSE OR RIGHT IS GRANTED UNDER ANY PATENT OR TRADEMARK OF GENESYS LOGIC INC.. GENESYS LOGIC HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS IN REGARD TO MATERIALS, INCLUDING ALL WARRANTIES, IMPLIED OR EXPRESS, OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY. IN NO EVENT SHALL GENESYS LOGIC BE LIABLE FOR ANY DAMAGES INCLUDING, WITHOUT LIMITATION, DAMAGES RESULTING FROM LOSS OF INFORMATION OR PROFITS. PLEASE BE ADVISED THAT THE MATERIALS MAY CONTAIN ERRORS OR OMMISIONS. GENESYS LOGIC MAY MAKE CHANGES TO THE MATERIALS OR TO THE PRODUCTS DESCRIBED THEREIN AT ANY TIME WITHOUT NOTICE.

Trademarks:

GENESYS LOGIC is a registered trademark of Genesys Logic, Inc.
All trademarks are the properties of their respective owners.

Office:

Genesys Logic, Inc.
12F, No. 205, Sec. 3, Beishin Rd., Shindian City,
Taipei, Taiwan
Tel: (886-2) 8913-1888
Fax: (886-2) 6629-6168

http://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	09/25/2003	First formal release.
1.10	01/19/2004	1. Added LQFP-48 pin diagram, list and description. 2. Removed LQFP-64 pin diagram, list and description. 3. Added Chapter 8 Ordering Information.
1.11	04/14/2004	Updated package dimension.
1.20	04/21/2004	Removed NAND Flash interface
1.30	07/02/2004	1. Added media memory card type in Chapter 1 And 2 2. Updated Table 6.1 - Absolute Maximum Ratings value 3. Updated Table 6.2 - DC Characteristics value 4. Added Chapter 6.3.5 Reset Timing 5. Updated IC Marking in package dimension diagram
1.31	01/18/2005	1. Added USB2.0 certified Test ID in Chapter 2 Features 2. Changed Table 6.1 - Absolute Maximum Ratings 3. Added Table 6.2 - Operating Conditions
1.32	01/21/2005	Added Chapter 6.4.6 93C46 Timing
1.33	02/01/2005	Changed power pin description in Table 3.2
1.34	03/06/2005	Changed pin# 13,14 pin description
1.35	04/06/2005	Update Datasheet to meet GL817E-09 with different pin out
1.36	06/21/2005	Add pin#11 pin description Modify pin#24 description to Power LED
1.38	04/19/2006	Add Reset timing chart

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

The GL817E is a highly compatible, best performance USB 2.0 Flash Card Reader Controller. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), Mini SD™, MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick Pro™ (MS Pro), Memory Stick Pro™ Duo (MS Pro Duo) Memory Stick ROM interface on one chip. The GL817E integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver, the Serial Interface Engine (SIE), and compatible 8-bit micro-controller.

By complies with Universal Serial Bus specification rev. 2.0 and USB Storage Class specification ver.1.0, the GL817E can be supported by Windows XP/ 2000/ Me default driver. Also it is supported in Windows 98/ 98SE, Mac, and Linux operating system. For the power consumption consideration, the GL817E complies with USB power specification for bus-powered devices.

The GL817E is available in 48-pin LQFP (Internal Mask ROM code), and it is the best cost / performance solution for your USB 2.0 high-speed Flash Card Reader application.

CHAPTER 2 FEATURES

- Supports USB 2.0 to Memory Stick ™ (MS) and Memory Stick PRO ™ (MS PRO), Secure Digital ™ (SD) and MultiMediaCard ™ (MMC) interface on one chip.
- Supports all combinations of MS/ MS PRO/ SD/ MMC application design.
- Complies with 480Mbps Universal Serial Bus specification rev. 2.0.vc
- Complies with USB Storage Class specification rev. 1.0. (Bulk only protocol).
- USB 2.0 certified (Test ID=40390390)
- Operating System supported: Windows XP/ 2000/ Me/ 98/ 98SE, Mac OS 9.x/ X, Linux.
- Supports customized storage device icon under Windows 98/ 98SE/ 2000 (SP2, SP3 and SP4) by Genesys Logic own driver.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Integrated MCU compatible 8-bit micro-controller.
- Hardware ECC generation and verification.
- Memory Stick™ (MS) / Memory Stick Duo™ (MS Duo) / High Speed Memory Stick™ (HS MS) / Memory Stick Pro™ (MS Pro) / Memory Stick Pro™ Duo (MS Pro Duo) Memory Stick ROM interface
  - Complies with Memory Stick Standard Memory Stick PRO Format Specifications ver 1.00-01
  - Complies with Memory Stick Format Specifications ver 1.40-00
  - Hardware support 4-bit HS Memory Stick PRO interface
  - Supports INS signal
  - Supports automatic CRC16 generation and verification
  - Supports different clock rate up to 40 MHz
- Secure Digital™ , Mini SD™ and MultiMediaCard™
  - Complies with Secure Digital™ / MultiMediaCard™ interface specification
  - Supports both SD / MMC mode access CLK/CMD/DAT0/DAT1/DAT2/DAT3
  - Command transmit and response receive can be enabled separately
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT3-0
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Data processing in block or byte
  - Supports different clock rate from 375 KHz to 24 MHz
- High efficient hardware engine
  - Automatic data read / write with card by hardware engine.
  - Easier firmware development.
  - Media interface signals output low automatically when suspend.
  - Supports automatic CRC16 generation and verification.
- Supports firmware correct page ECC error capability.
- Supports automatic page copy (source page read + destination page write).
- Complies with USB power specification for bus-powered devices.
- Supports Suspend and Wake-up Resume.
- 3.3 Volt operation.
- Available in 48-pin LQFP package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

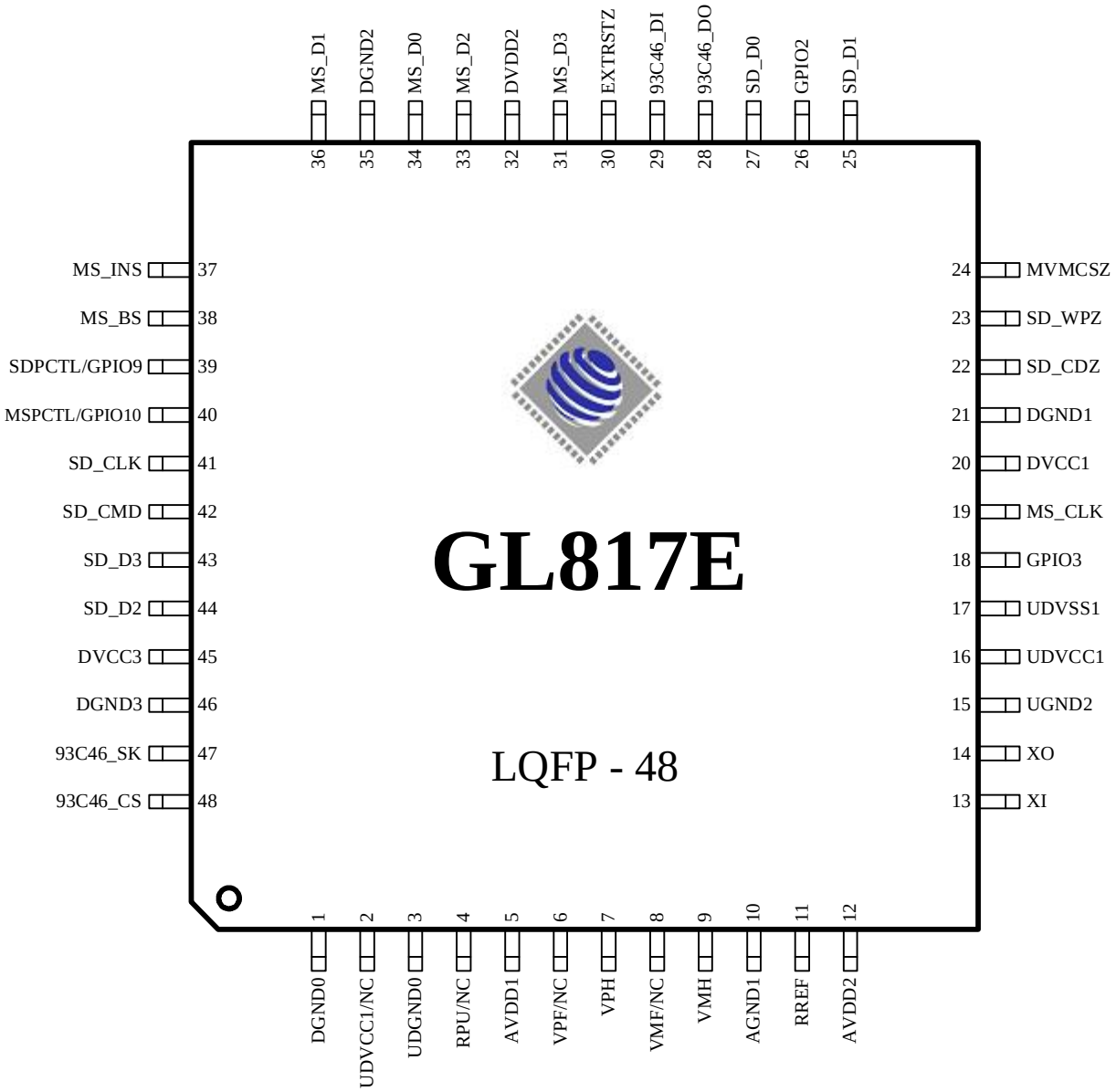


Figure 3.1 - 48 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1 - 48 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DGND0	P	13	XI	I	25	SD_D1	B/SO	37	MS_INS	B/I
2	UDVCC1/ NC	P	14	XO	O	26	GPIO2	B/O	38	MS_BS	O
3	UDGND0	P	15	UGND2	P	27	SD_D0	B/SO	39	SDPCTL/ GPIO9	B/O
4	RPU/ NC	A	16	UDVCC1	P	28	93C46_DO	B/I	40	MSPCTL/ GPIO10	B/O
5	AVDD1	P	17	UDVSS1	P	29	93C46_DI	B/O	41	SD_CLK	O
6	VPF/ NC	A	18	GPIO3	B/O	30	EXTRSTZ	I	42	SD_CMD	B/SO
7	VPH	A	19	MS_CLK	O	31	MS_D3	B/SO	43	SD_D3	B
8	VMF/ NC	A	20	DVCC1	P	32	DVDD2	P	44	SD_D2	B
9	VMH	A	21	DGND1	P	33	MS_D2	B/SO	45	DVCC3	P
10	AGND1	P	22	SD_CDZ	B/I	34	MS_D0	B/SO	46	DGND3	P
11	RREF	A	23	SD_WPZ	B/I	35	DGND2	P	47	93C46_SK	B/O
12	AVDD2	P	24	NVMCSZ	O	36	MS_D1	B/SO	48	93C46_CS	B/O

3.3 Pin Descriptions

Table 3.2 - 48 Pin Descriptions

Pin Name	Pin#	Type	Description
DGND0~3	1,21,35,46	P	Digital GND #0~3
UDVCC1	2	P	GL817E-07: UTMI Digital VDD #1. GL817E-08/GL817E-09: NC: No connection.
UDVCC1	16	P	UTMI Digital VDD #1
UGND0	3	P	UTMI GND #0
RPU/ NC	4	A	GL817E-07: USB resistor pulls up when GL817E-07 mounted. GL817E-08 ~ High: NC: No connection.
AVDD1	5,12	P	Analog VDD #1
VPF	6	A	GL817E-07: FS D+

			GL817E-08/GL817E-09: NC: No connection.
VPH	7	A	HS D+
VMF	8	A	GL817E-07: FS D- GL817E-08/GL817E-09: NC: No connection.
VMH	9	A	HS D-
AGND1	10	P	Analog GND #1
RREF	11	A	Reference resistor
XI	13	I	12MHz Crystal This pin can be connected to one terminal of the crystal or can be connected to an external 12MHz clock when a crystal is not used.
XO	14	O	12MHz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL/CLK. It may not be used to drive any external circuitry other than the crystal circuit.
UGND2	15	P	UTMI GND
UDVSS1	17	P	UTMI Digital GND
GPIO2~3,9,10	26,18,39,40	B/O (odpu)	GPIO2~3,9,10
MS_CLK	19	O	Memory Stick SCLK
DVCC1,3	20,45	P	Digital VDD #1,3
SD_CDZ	22	B/I (pu)	SD CD#
SD_WPZ	23	B/I (pu)	SD Write Protect Detect
NVMCSZ	24	O (pu)	Power LED
SD_D0~3	27,25,44,43	B/SO (pu)	SD DAT0~3
93C46_DO	28	B/I	93C46 Data out
93C46_DI	29	B/O	93C46 Data in
EXTRSTZ	30	I (pu)	External reset Internal pull-up : 65K ohm (+/- 50%)
MS_D0~3	34,36,33,31	B/SO (pu)	MS DAT3~0
DVDD2	32	P	Digital VDD #2
MS_INS	37	B/I (pu)	Memory Stick INS
MS_BS	38	O	Memory Stick BS
SD_PCTL	39	B/O	SD power control
MS_PCTL	40	B/O	MS power control

SD_CLK	41	O	SD/MMC CLK
SD_CMD	42	B/SO (pu)	SD/MMC CMD
93C46_SK	47	B/O	93C46 Clock
93C46_CS	48	B/O	93C46 CS

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

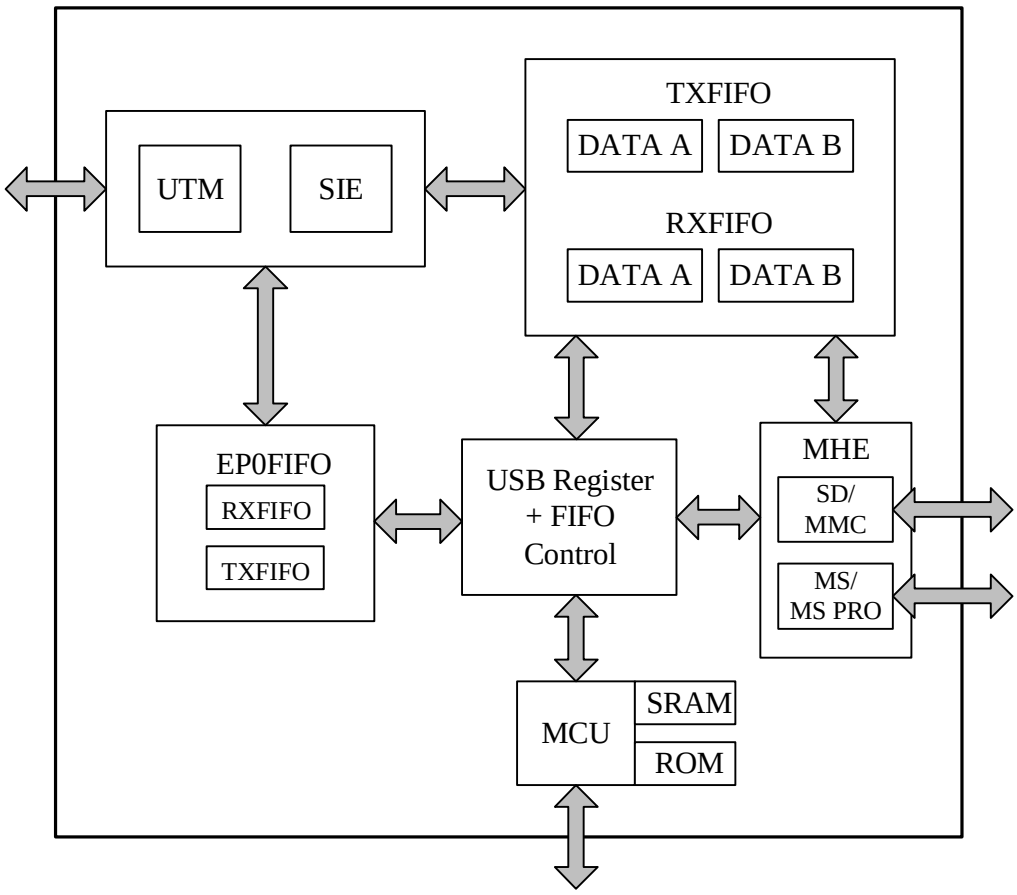


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0 FIFO

Endpoint 0 FIFO: The Control FIFO. It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

5.4 Bulk FIFO

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

5.4.1 TXFIFO

- To ensure the continuous data transmission, TXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and two 16 bytes corresponding redundant areas. All can be directly accessed by MCU.
- Normally SIE popes data, SME pushes data for DATA A/B FIFOs, and redundant area is pushed by SME and popped by MCU.
- Supports MCU single byte access for SmartMedia ECC error correction.
- Supports transmit mode SIE won't transmit data filled in TXFIFO before MCU complete the data integrity checking.

5.4.2 RXFIFO

- To ensure the continuous data transmission, RXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and 16 bytes single redundant area. All can be directly accessed by MCU.
- Normally SME popes data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by MCU and popped by SME.

5.5 MHE (Media Interface)

- SD/MMC Engine.
- MS/MS PRO Engine.

5.6 USB Registers / FIFO Control

It is a register space to store status information and to control the functions of GL817E by MCU.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.25%

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	Input High Voltage		2.6	-	5	V
V_{IL}	Input Low Voltage		0.0	-	0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
I_{OH}	Output Current High		-	8.3	-	mA
I_{OL}	Output Current Low		-	7.8	-	mA
C_{IN}	Input Pin Capacitance		-	-	2.0	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	280	µA
I_{CC}	Supply current	Connect to USB with MCU operating	-	-	85	mA

6.4 AC Characteristics

6.4.1 UTMI Transceiver

The GL817E is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.4.2 Secure Digital / MultiMediaCard

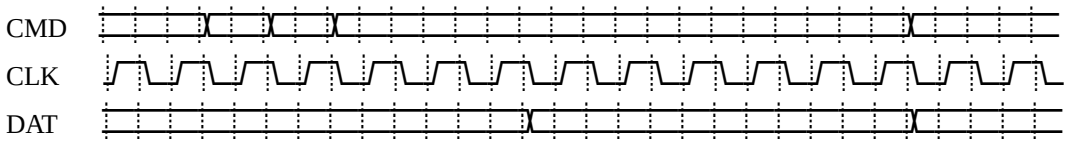


Figure 6.2 - Timing Diagram of SD / MMC Interface

Parameter	Description	Mode	Typ	Unit	Remark
Fck	CLK frequency	0	375K	Hz	
		1	6M		
		2	15M		
		3	24M		

6.4. 3 Memory Stick

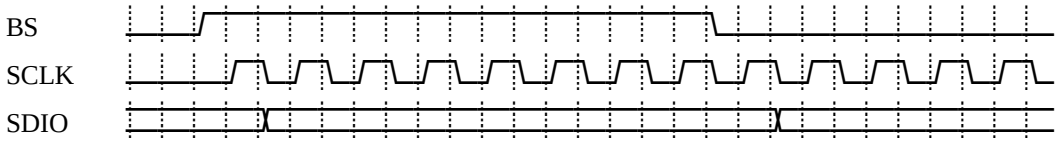


Figure 6.3 - Timing Diagram of MemoryStick

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	24M		

6.4. 4 Memory Stick Pro

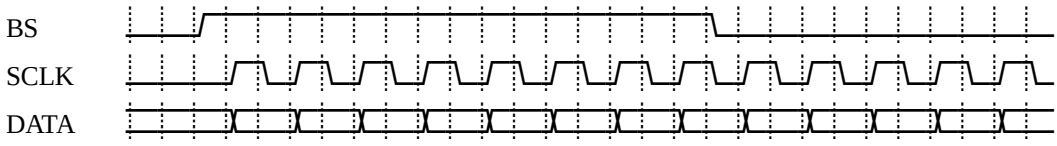


Figure 6.4 - Timing Diagram of MemoryStick Pro

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	30M	Hz	
		1	40M		

6.4.5 Reset Timing

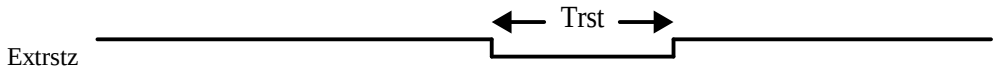


Figure 6.5 - Timing Diagram of Reset width

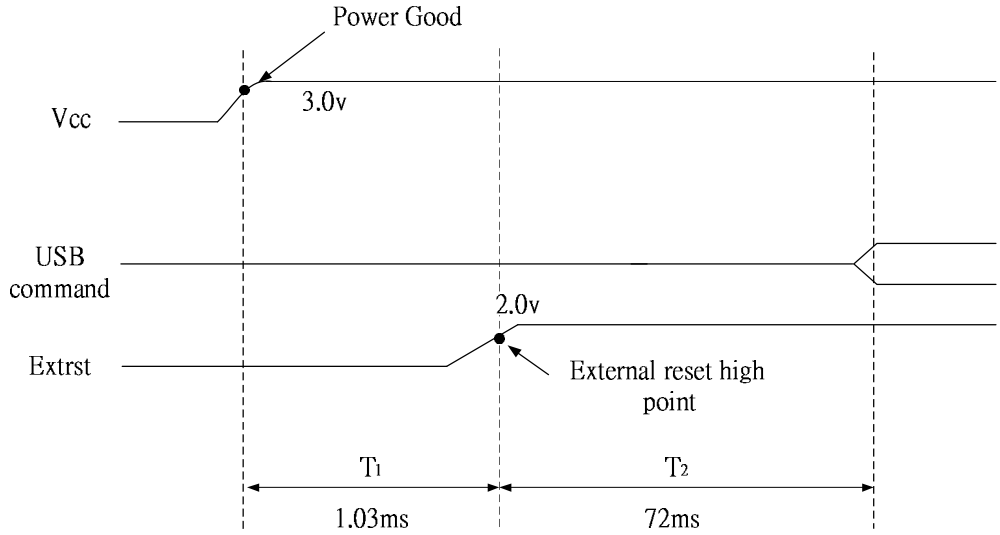


Figure 6.6- Timing Diagram of Power Good to USB command receive ready

Parameter	Description	Min	Typ	Max	Unit
Trst	Chip reset sense timing width	2	-	-	us
T1	External reset valid from power up to high	1.03	-	-	ms
T2	Reset Deassertion to respond USB command ready	72	-	-	ms

6.4.6 93C46 Timing

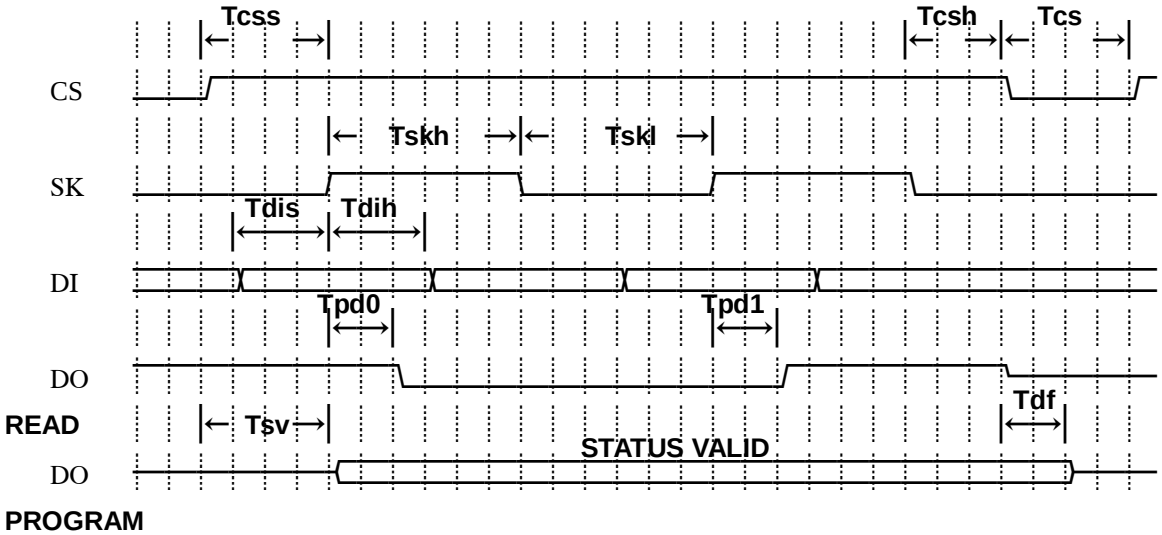
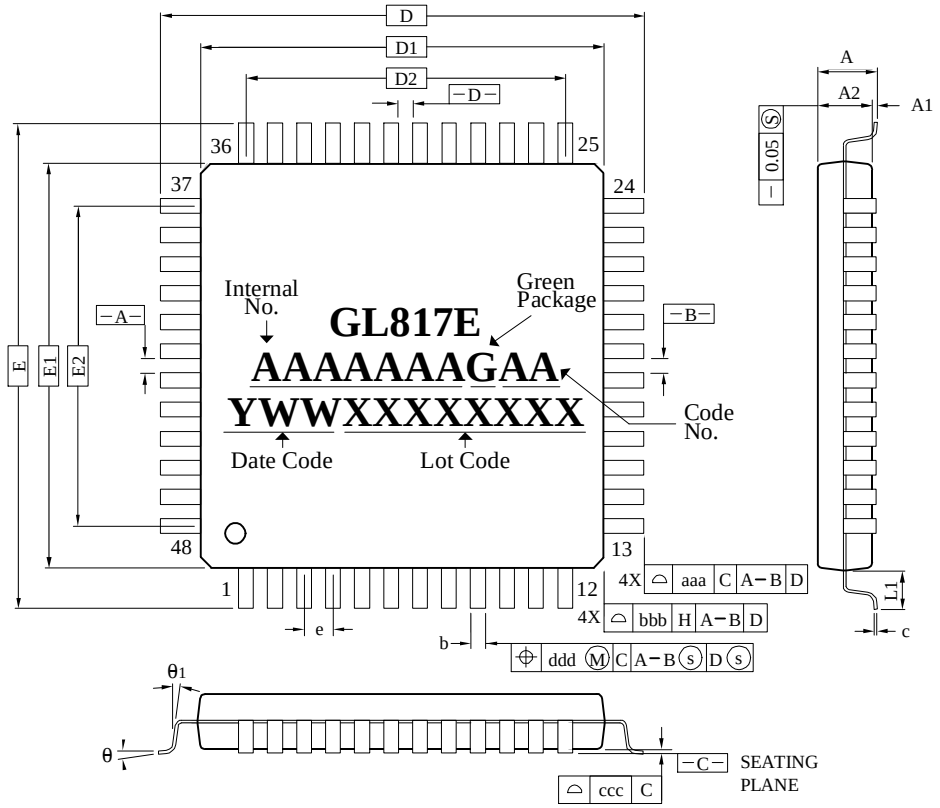
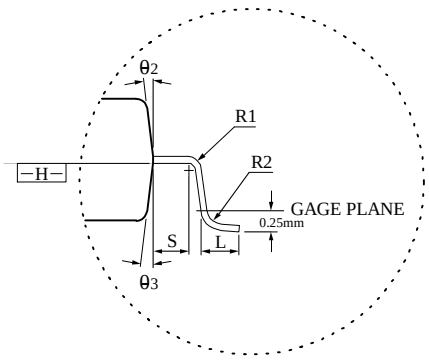


Figure 6.6 - Timing Diagram of 93C46

Parameter	Description	Min	Typ	Max	Unit
Tskh	SK High Time	250	-	-	ns
Tskl	SK Low Time	250	-	-	
Tcs	Minimum CS Low Time	250	-	-	
Tcss	CS Setup Time	50	-	-	
Tdis	DI Setup Time	100	-	-	
Tcsh	CS Hold Time	0	-	-	
Tdih	DI Hold Time	100	-	-	
Tpd1	Output Delay to “1”	-	-	250	
Tpd0	Output Delay to “0”	-	-	250	
Tsv	CS to Status Valid	-	-	250	
Tdf	CS to DO in High Impedance	-	-	100	

CHAPTER 7 PACKAGE DIMENSION





NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Figure 7.1 - GL817E 48 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL817E	48-pin LQFP	

