LOW SKEW, 1-TO-4 DIFFERENTIAL-TO-LVDS FANOUT BUFFER

ICS889832

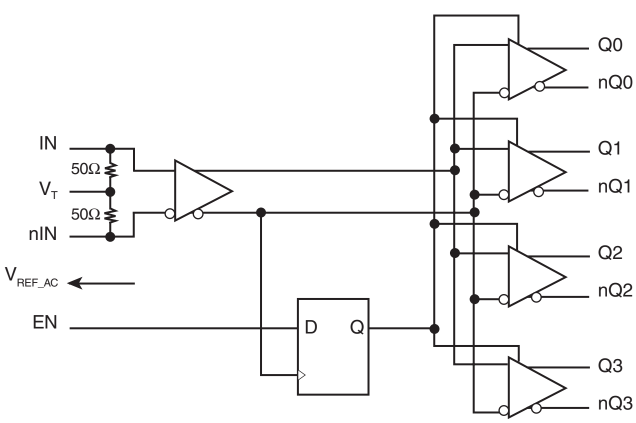
GENERAL DESCRIPTION

The ICS889832 is a high speed 1-to-4 Differential-to-LVDS Fanout Buffer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS889832 is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and V_{REF_AC} pin allow other differential signal families such as LVPECL, LVDS, and SSTL to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS889832 is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

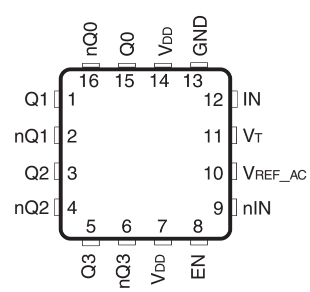
FEATURES

- Four differential LVDS outputs
- IN, nIN pair can accept the following differential input levels: LVPECL, LVDS, SSTL
- 50Ω internal input termination to V_T
- Output frequency: >2GHz
- Output skew: 25ps (maximum)
- Part-to-part skew: 200ps (maximum)
- Additive phase jitter, RMS: <0.2ps (typical)
- Propagation delay: 510ps (maximum)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS889832
16-Lead VFQFN
3mm x 3mm x 0.95 package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q1, nQ1	Output		Differential output pair. LVDS interface levels.
3, 4	Q2, nQ2	Output		Differential output pair. LVDS interface levels.
5, 6	Q3, nQ3	Output		Differential output pair. LVDS interface levels.
7, 14	V_{DD}	Power		Positive supply pins.
8	EN	Input	Pullup	Synchronizing clock enable. When LOW, Q outputs will go LOW and nQ outputs will go HIGH on the next LOW transition at IN inputs. Input threshold is V_{DD}/2V. Includes a 37kΩ pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN. LVTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential clock input. 50Ω internal input termination to V_T.
10	V_{REF_AC}	Output		Reference voltage for AC-coupled applications.
11	V_T	Input		Termination input.
12	IN	Input		Non-inverting differential clock input. 50Ω internal input termination to V_T.
13	GND	Power		Power supply ground.
15, 16	Q0, nQ0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

Table 3A. Control Input Function Table

Input	Outputs	
EN	Q0:Q3	nQ0:nQ3
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

After EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.*

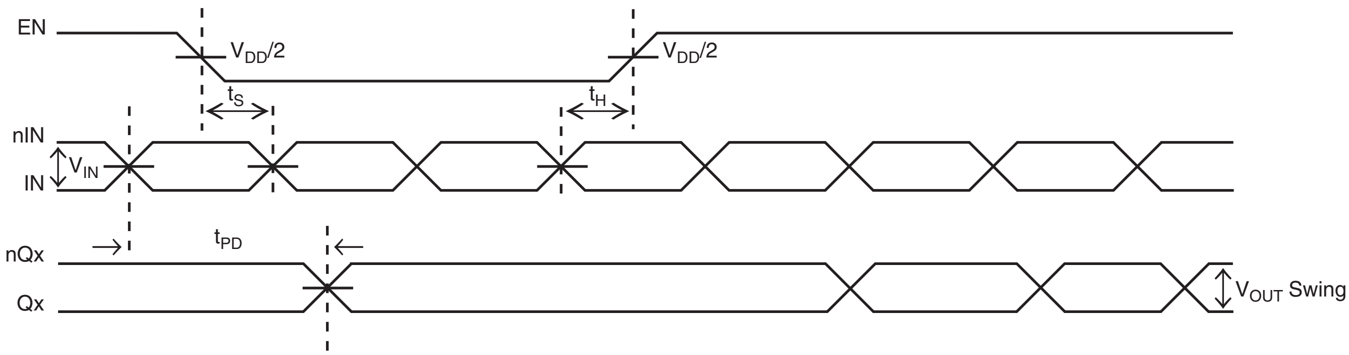


Figure 1. EN Timing Diagram

Table 3B. Truth Table

Inputs			Outputs	
IN	nIN	EN	Q0:Q3	nQ0:nQ3
0	1	1	0	1
1	0	1	1	0
X	X	0	0 (NOTE1)	1 (NOTE1)

NOTE 1: On next negative transition of the input signal (IN).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Input Current, IN, nIN	±50mA
V_T Current, I_{VT}	±100mA
Input Sink/Source, I_{REF_AC}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	51.5°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				120	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			0		0.7	V
I_{IH}	Input High Current	EN	V_{DD} = V_{IN} = 2.625V			5	µA
I_{IL}	Input Low Current	EN	V_{DD} = 2.625V, V_{IN} = 0V	-150			µA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	(IN, nIN)	IN-to-VT	40	50	60	Ω
V_{IH}	Input High Voltage	(IN, nIN)		1.2		V_{DD}	V
V_{IL}	Input Low Voltage	(IN, nIN)		0		V_{IH} - 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{REF_AC}	Reference Voltage			V_{DD} - 1.42	V_{DD} - 1.37	V_{DD} - 1.32	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		3.4	V
I_{IN}	Input Current; NOTE 1	(IN, nIN)				35	mA

NOTE 1: Guaranteed by design.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		0.3	0.4	0.5	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1	1.25	1.5	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

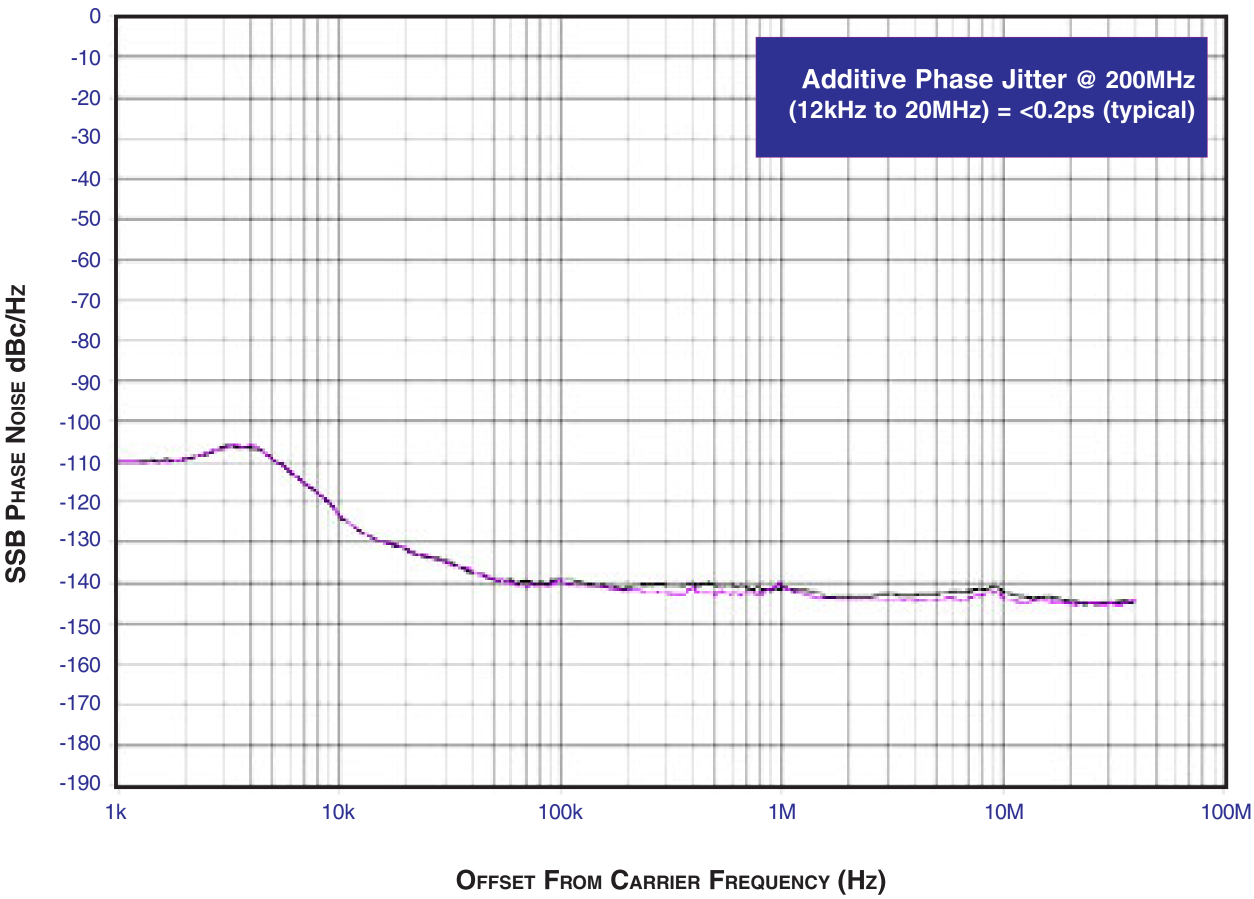
TABLE 5. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%; TA = -40°C TO 85°C

Symbol	Parameter		Condition	Minimum	Typical	Maximum	Units
f_{MAX}	Maximum Output Frequency				>2		GHz
t_{PD}	Propagation Delay; (Differential); NOTE 1			275	390	510	ps
*t*sk(o)	Output Skew; NOTE 2, 4					25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					200	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section		Integration Range: 12kHz - 20MHz		<0.2		ps
t_R/t_F	Output Rise/Fall Time		20% to 80%	70	150	235	ps
t_S	Clock Enable Setup Time	EN to IN, nIN		300			ps
t_H	Clock Enable Hold Time	EN to IN, nIN		300			ps

All parameters are measured at ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

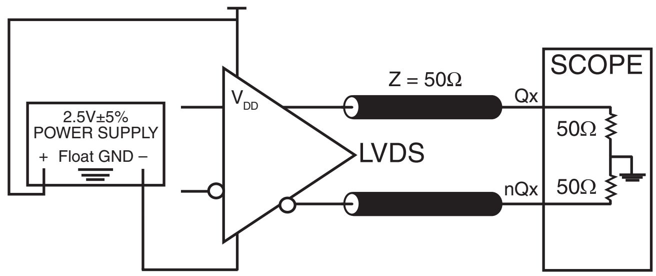
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

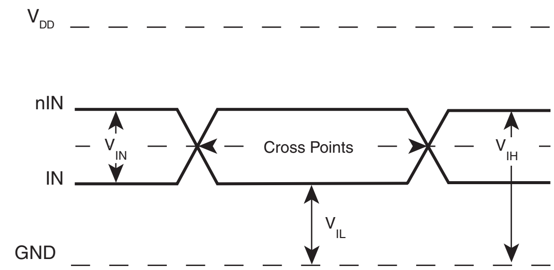


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

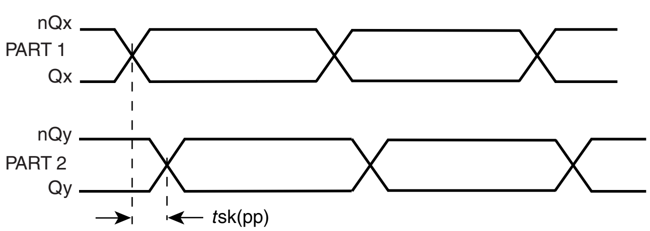
Parameter Measurement Information



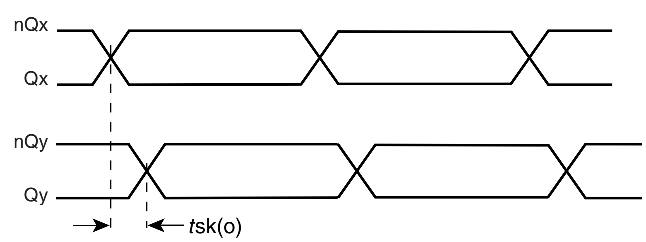
Output Load AC Test Circuit



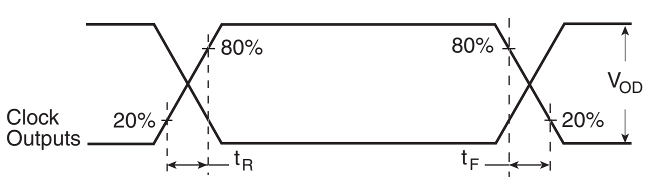
Differential Input Level



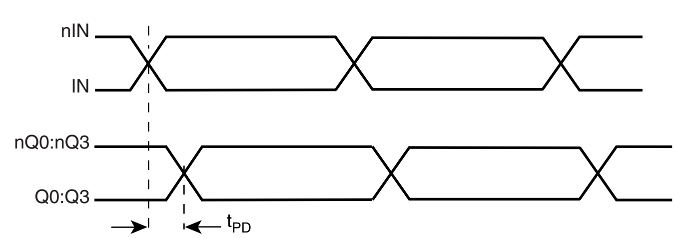
Part-to-Part Skew



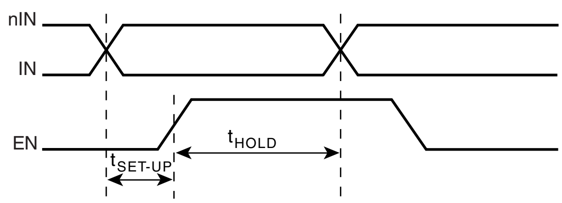
Output Skew



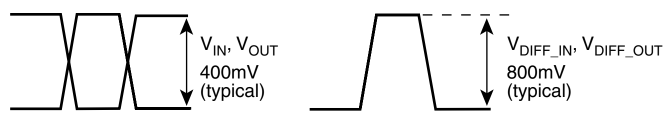
Output Rise/Fall Time



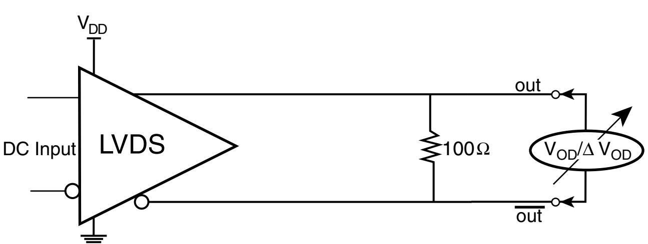
Propagation Delay



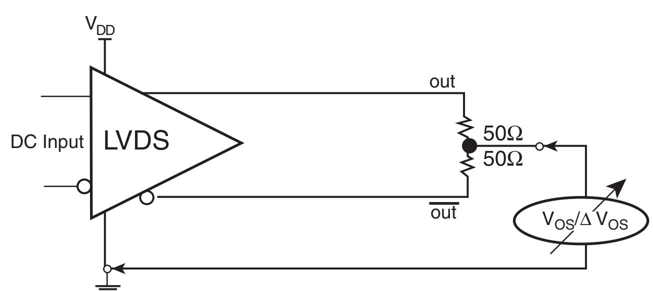
SETUP & HOLD TIME



SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

Application Information

LVPECL Input with Built-In 50Ω Terminations Interface

The IN /nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 1A to 1f* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

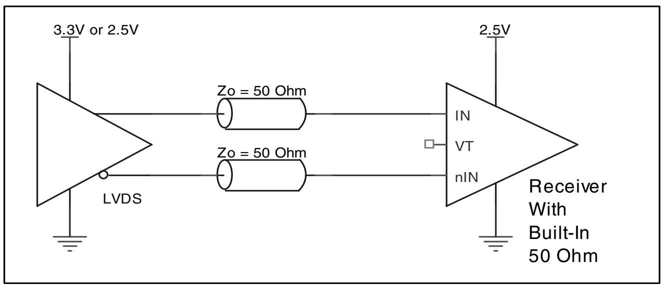


Figure 1A. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVDS Driver

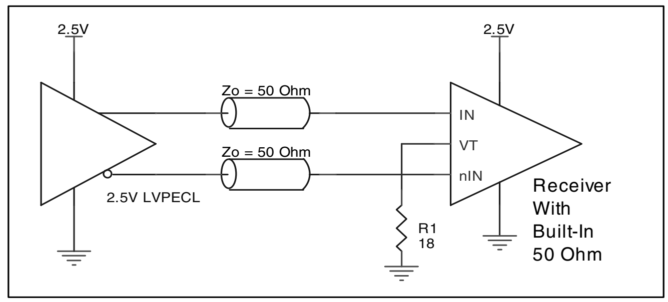


Figure 1B. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an LVPECL Driver

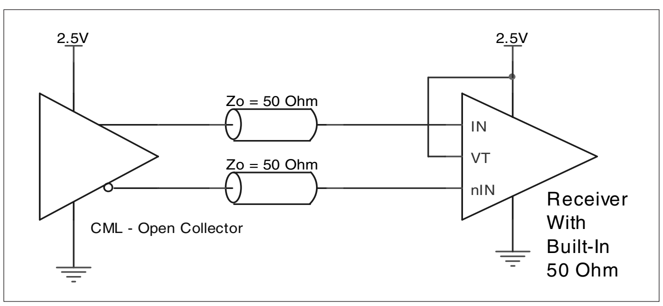


Figure 1C. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by an Open Collector CML Driver

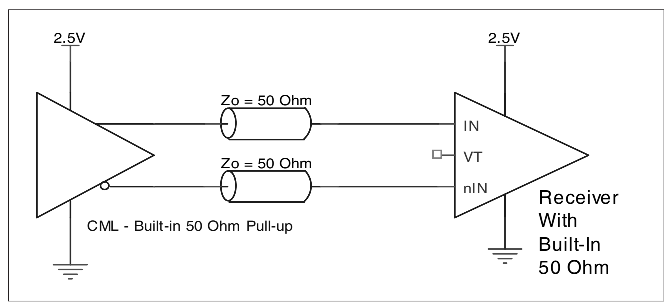


Figure 1D. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a CML Driver with Built-In 50Ω Pullup

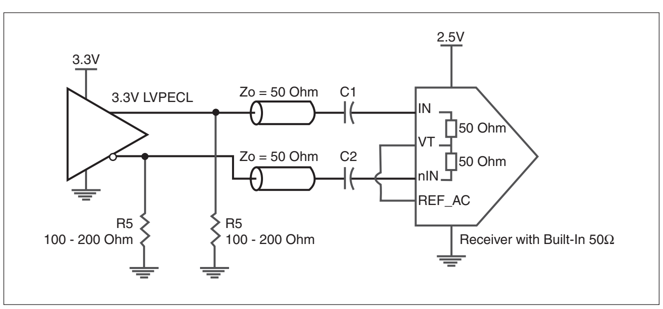


Figure 1E. HiPerClockS IN/nIN Input with Built-in 50Ω

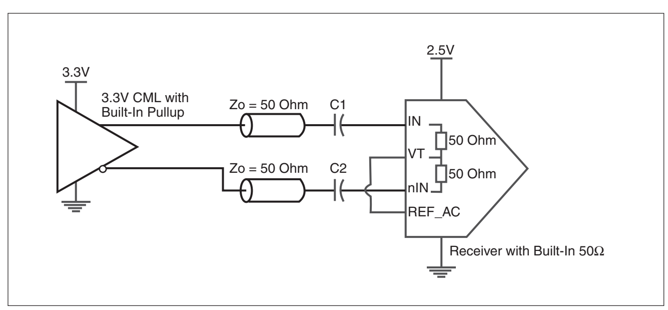


Figure 1F. HiPerClockS IN/nIN Input with Built-in 50Ω Driven by a 3.3V CML Driver with Built-In Pullup

Recommendations for Unused Output Pins

Outputs:

LVDS Output
All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

2.5V LVDS Driver Termination

Figure 2 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused outputs.

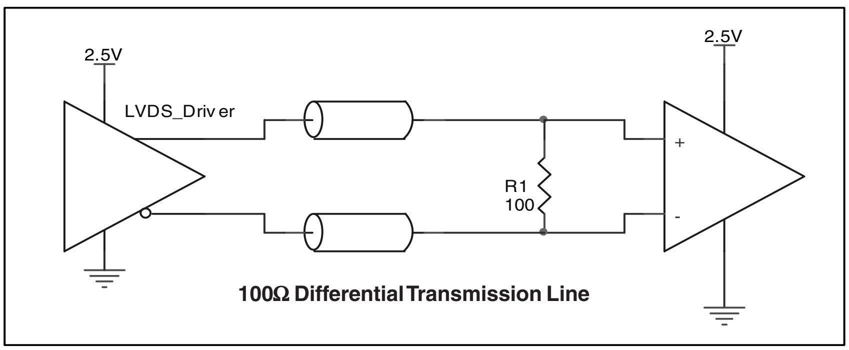


Figure 2. Typical LVDS Driver Termination

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS889832. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS889832 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

- $Power\_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 2.625V * 120mA = **315mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow of and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.315W * 51.5°C/W = 101.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead VFQFN

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)	
	0
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

Transistor Count

The transistor count for ICS889832 is: 206

Pin compatible with SY89832U

Package Outline - K Suffix for 16 Lead VFQFN

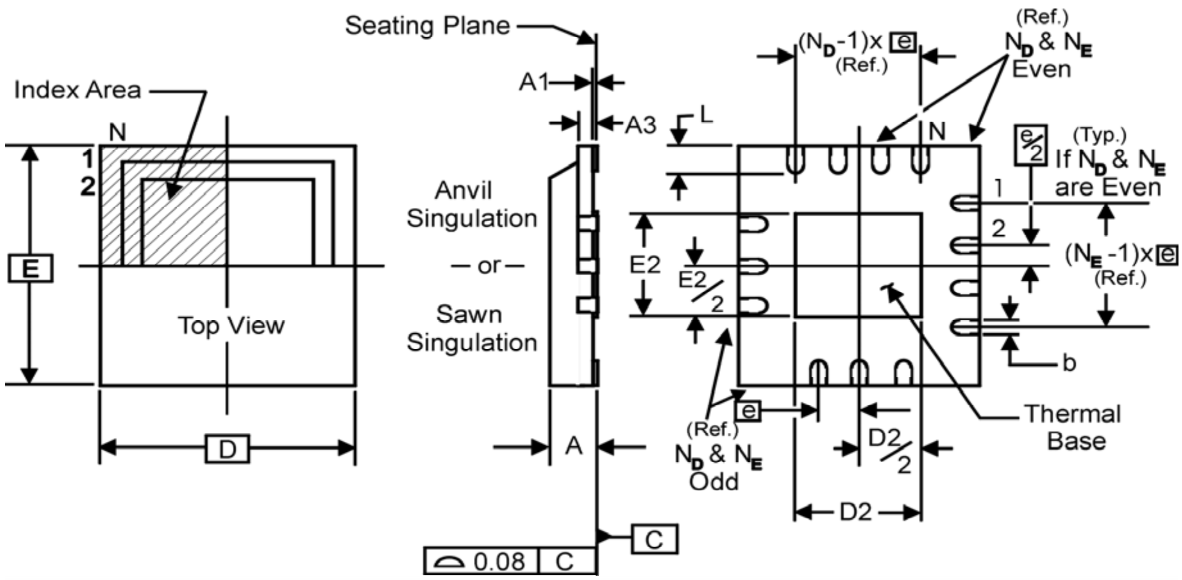


Table 8. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	**MINIMUM**	**MAXIMUM**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	4	
N_E	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS889832AK	832A	16 Lead VFQFN	tube	-40°C to 85°C
ICS889832AKT	832A	16 Lead VFQFN	2500 tape & reel	-40°C to 85°C
ICS889832AK	TBD	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS889832AKT	TBD	16 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

IDT™
www.IDT.com