

18M Network Search (QDR™II Interface Compliant)

Datasheet Brief IDT75K72234

Introduction

With the expanding Internet, all levels of the network must become faster. This requires high-speed packet searches, which are essential for routing, but also necessary for higher-level functions such as Quality of Service (QoS) support and access control. To meet this need, IDT has developed network search engines that accelerate packet processing at OC-192 data rates and beyond.

Device Description

The 18M NSE with Dual LA-1 interface is intended to work with NPUs having a Look Aside Interface. Multiple devices including the 18M Dual LA-1NSE can be connected to the same LA-1 interface. Each 18M Dual LA-1 NSE device may be optionally point-to-point expanded up to eight NSE devices.

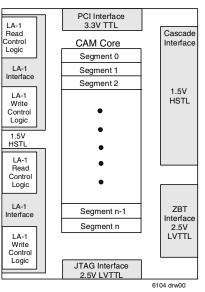
NSE Features

- 256K x 72 (18M) Data and Mask cells
- Full Ternary Content Addressable Memory
- Supports up to 250 Million searches per second
- Dynamic Database Management[™]
 - Configurable Database widths
 - Databases are selectable per NSE command
- Programmable Power Management
 - Only the selected Database consumes power
 - PowerSave logic provides additional power savings
- Lookup (Search) Instructions
- Standard Lookup
- Multi-Hit Lookup
- Multi-Database Lookup
- Re-Issue Multi-Database Lookup
- Simultaneous Multi-Database Lookup
- Maintenance Features
 - Per entry aging support with notification
 - Multi Hit Invalidate
 - Learn per Database
- Search with learn
 - Automatic learning
 - Duplicate learn prevention per database
- Multiple return index formats
- Flexible Associated Data Management
 - 0, 32, 64, or 128 bits of Associated Data per entry
- Instruction Completion Notification
- Multiple contexts per interface
- Pool of 72-bit Global Mask Registers (shared across contexts)
- Parity support for interfaces and CAM core
- 35mm x 35mm thermally efficient 900 BGA Package

External Interfaces

- Two independent LA-1 (QDRII compliant) interfaces
 - Frequency range from 133MHz up to 250 MHz
 - Supports burst of 2 data transfers
 - Echo clocks supported (CQ, \overline{CQ})
 - Dynamic or programmable output impedance control
- PCI2.2 compliant interface
 - Optimized for NSE management
- Cascade Interface
 - 8 NSEs in a Point-to-Point Cascade
 - Up to 4 Multi-Drop cascades to a single LA-1 interface
 - Supports up to 32 devices per LA-1 interface
- NSE attached associated SRAM glueless ZBT® Interface
- IEEE 1149.1-2001 compliant JTAG Interface

Simplified Block Diagram



MAY 2004

©2003 Integrated Device Technology, Inc. All rights reserved. Product specifications subject to change without notice. QDR™ II- Quad Data Rate DSC-6104/03 Trademark of Cypress, IDT, Micron, NEC and Samsung). All brands or products are the trademarks or registered trademarks of their respective owners. ZBT® and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc. LA-1 refers to the approved NPF(www.npforum.org) Look Aside Interface implementation agreement 'Look Aside Interface LA-1.0 (www.npforum.org/techinfo/f2001.114.14a.pdf)