mosaic

SYS32512ZK/LK - 010/012/015

Issue 5.0 June 1999

Description

The SYS32512 is a 512K x 8 SRAM module in a ZIP (ZK) or SIMM (LK & LKXA) packages with access times of 12 and 15ns, with 10ns parts under development. The device is available to commercial and industrial temperature grade.

The LK SIMM package is designed for standard SIMM sockets. The LKXA is designed to fit both angled and standard sockets.

Features

- Access times of 10, 12 and 15ns.
- 5V ± 10%.
- Commercial and Industrial temperature grades
- 72 pin ZIP and SIMM packages.
- Industry standard footprint.
- Power dissipation.
- Operating Power (32 Bit) 4.62W (max)
- Low power standby. (TTL) 1.32W (max)
  (CMOS) 330mW (max)
- Completely Static Operation.

Package Details

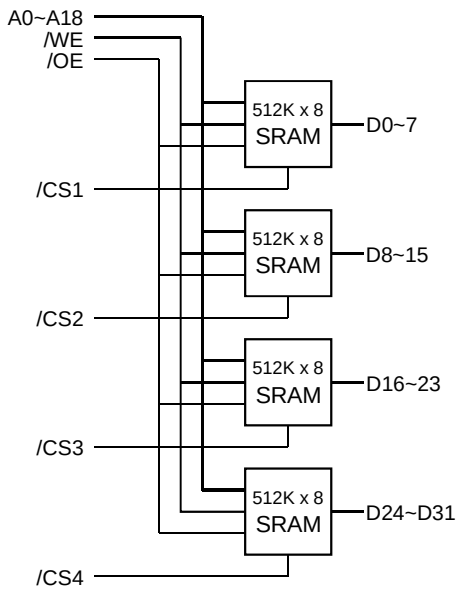
Plastic 72 Pin ZIP (ZK)
Max. Dimensions (mm) - 97.80 x 20.61 x 5.90

Plastic 72 Pin SIMM (LK)

Max. Dimensions (mm) - 108.08 x 15.00 x 5.25

Plastic 72 Pin SIMM (LKXA)
Max. Dimensions (mm) - 108.08 x 20.32 x 4.55

Block Diagram



Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A18
Data Input/Output	D0~D31
Chip Select	/CS1~4
Presence Detect	PD0~3
Write Enable	/WE
Output Enable	/OE
No Connect	NC
Power	V_{CC}
Ground	V_{SS}

Pin Definition - SYS32512 ZK/LK/LKXA

Pin	Signal	Pin	Signal
1	NC	37	/CS4
2	NC	38	/CS3
3	PD2	39	A17
4	PD3	40	A16
5	V_{SS}	41	/OE
6	PD0	42	V_{SS}
7	PD1	43	D24
8	D0	44	D16
9	D8	45	D25
10	D1	46	D17
11	D9	47	D26
12	D2	48	D18
13	D10	49	D27
14	D3	50	D19
15	D11	51	A3
16	V_{CC}	52	A10
17	A0	53	A4
18	A7	54	A11
19	A1	55	A5
20	A8	56	A12
21	A2	57	V_{CC}
22	A9	58	A13
23	D12	59	A6
24	D4	60	D20
25	D13	61	D28
26	D5	62	D21
27	D14	63	D29
28	D6	64	D22
29	D15	65	D30
30	D7	66	D23
31	V_{SS}	67	D31
32	/WE	68	V_{SS}
33	A15	69	A18
34	A14	70	NC
35	/CS2	71	NC
36	/CS1	72	NC

Note
ZK : PD1=GND, PDO=PD2=PD3=OPEN

Absolute Maximum Ratings(1)

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V_{SS}	V_T (2)	-0.3	to	+7.0	V
Power Dissipation	P_T		4.0		W
Storage Temperature	T_{STG}	-55	to	+125	^OC

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

(2) V_T can be -2.0V pulse of less than 2ns.

Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit	
Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Input High Voltage		V_{IH}	2.2	-	V_{CC}+0.3	V	
Input Low Voltage		V_{IL}	-0.3	-	0.8	V	
Operating Temperature	(Commercial)	T_A	0	-	70	^OC	
	(Industrial)	T_{AI}	-40	-	85	^OC	(I Suffix)

DC Electrical Characteristics

(V_{CC}=5V±10%, T_A=0^{O}C to 70^{O}C)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	Address, /OE, /WE	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-8	-	8	µA
Output Leakage Current	Worst Case	I_{LO}	/CS=V_{IH},$V_{I/O}$=GND to V_{CC}	-8	-	8	µA
Average Supply Current	32 Bit	I_{CC1}	Min. Cycle, /CS=V_{IL}, V_{IN} =V_{IH} or V_{IL}, I_{OUT}=OmA	-	-	840	mA
Standby Supply Current	TTL	I_{SB1}	/CS=V_{IH}	-	-	240	mA
	CMOS	I_{SB2}	/CS≥V_{CC}-0.2V, 0.2V ≥V_{IN}≥V_{CC}-0.2V	-	-	60	mA
Output Voltage Low		V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Notes (1) /CS1~4 inputs operate simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

(2) Typical Values are at V_{CC}=5.0V, T_A=25^{O}C and specified loading. /CS above refers to /CS1~4

Capacitance

(V_{CC} = 5.0V, T_A = 25°C)

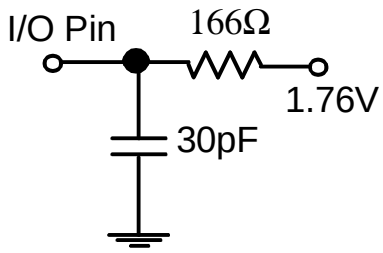
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance, (Address, /OE, /WE)	C_{IN1}	V_{IN}=0V	-	-	32	pF
Input Capacitance, (Other)	C_{IN2}	V_{IN}=0V	-	-	7	pF
Output Capacitance, 8 bit mode (worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	40	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 3ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- V_{CC} = 5V±10%

Output Load



Operation Truth Table

/CS	/OE	/WE	Data Pins	Supply Current	Mode
H	X	X	High Impedence	I_{SB1},I_{SB2}	Standby
L	L	H	Data Out	I_{CC1}	Read
L	H	L	Data In	I_{CC1}	Write
L	L	L	Data In	I_{CC1}	Write
L	H	H	High Impedence	I_{SB1},I_{SB2}	High Z

Notes : H=V_{IH} : L=V_{IL} : X=V_{IH} or V_{IL}

Read Cycle

		10		12		15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Select Access Time	t_{ACS}	-	10	-	12	-	15	ns
Output Enable to Output Valid	t_{OE}	-	5	-	6	-	7	ns
Output Hold From Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	5	0	6	0	7	ns
Output Disable to Output in High Z	t_{OHZ}	0	5	0	6	0	7	ns

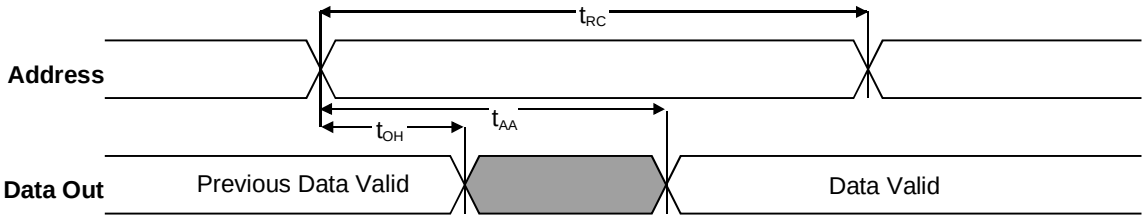
Write Cycle

		10		12		15		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Chip Selection to End of Write	t_{CW}	7	-	8	-	10	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	10	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	7	-	8	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	5	0	6	0	10	ns
Data to Write Time Overlap	t_{DW}	5	-	6	-	7	-	ns
Data Hold time from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	3	-	3	-	3	-	ns

Under Development

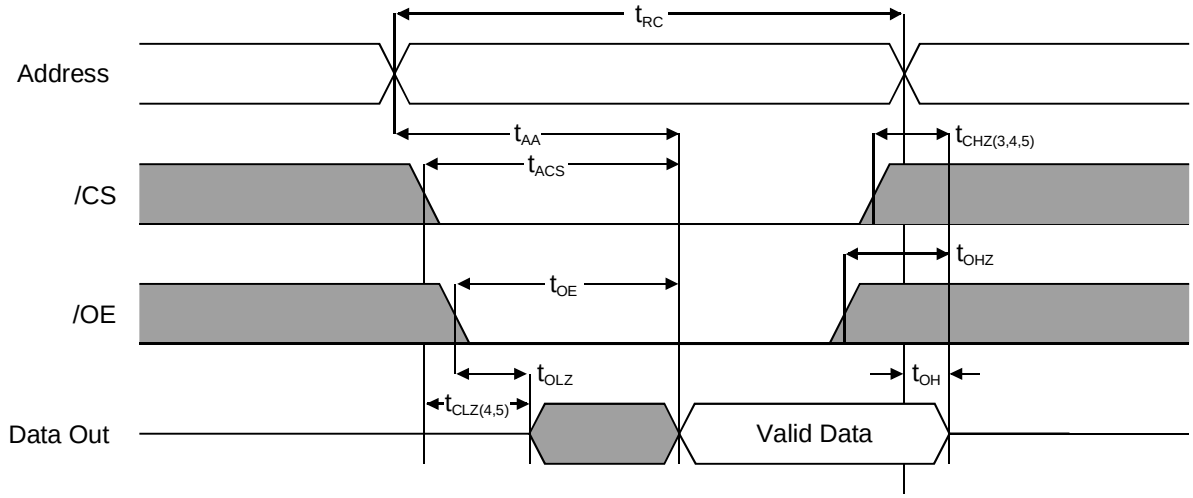
Read Cycle 1

(Address Controlled, /CS=/OE=V_{IL}, /WE=V_{IH})



Read Cycle 2

(/WE = V_{IH})

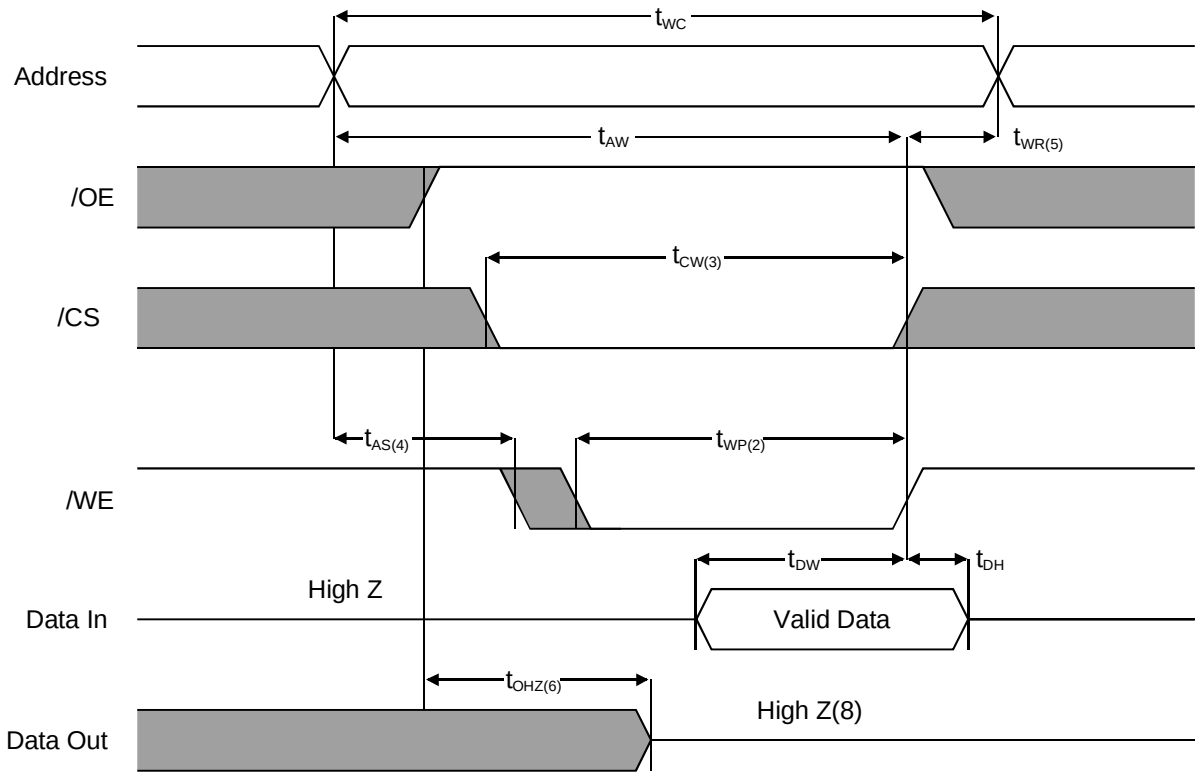


NOTES(READ CYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{CHZ}(Max.) is less than t_{CLZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=V_{IL}.
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
9. /CS=/CS1~4

Write Cycle 1

(/OE = Clock)

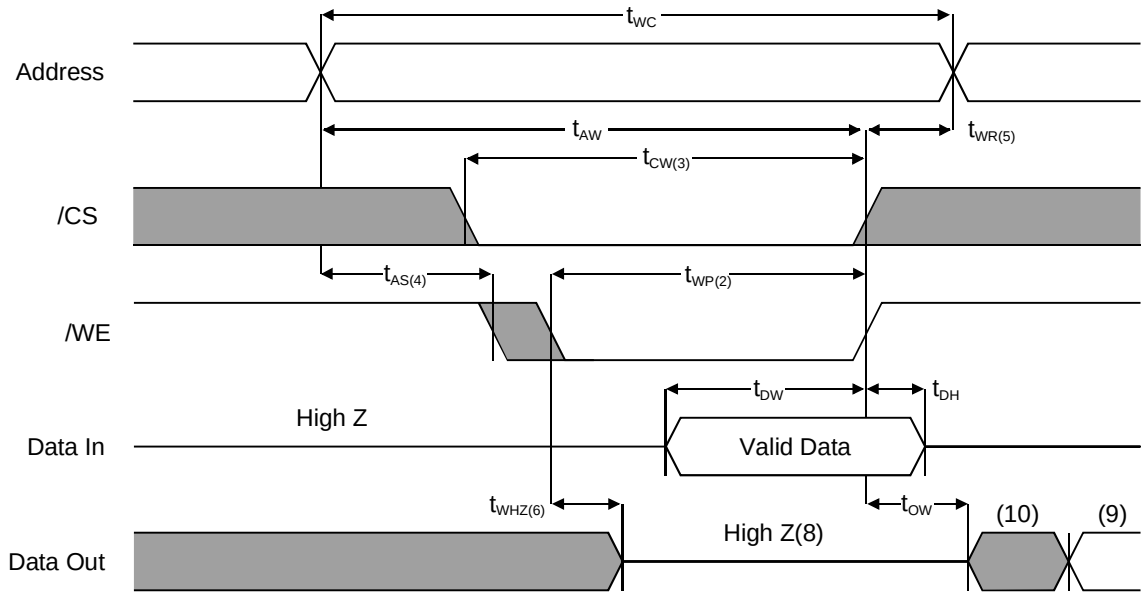


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
11. /CS=/CS1~4

Write Cycle 2

(/OE = Low Fixed)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
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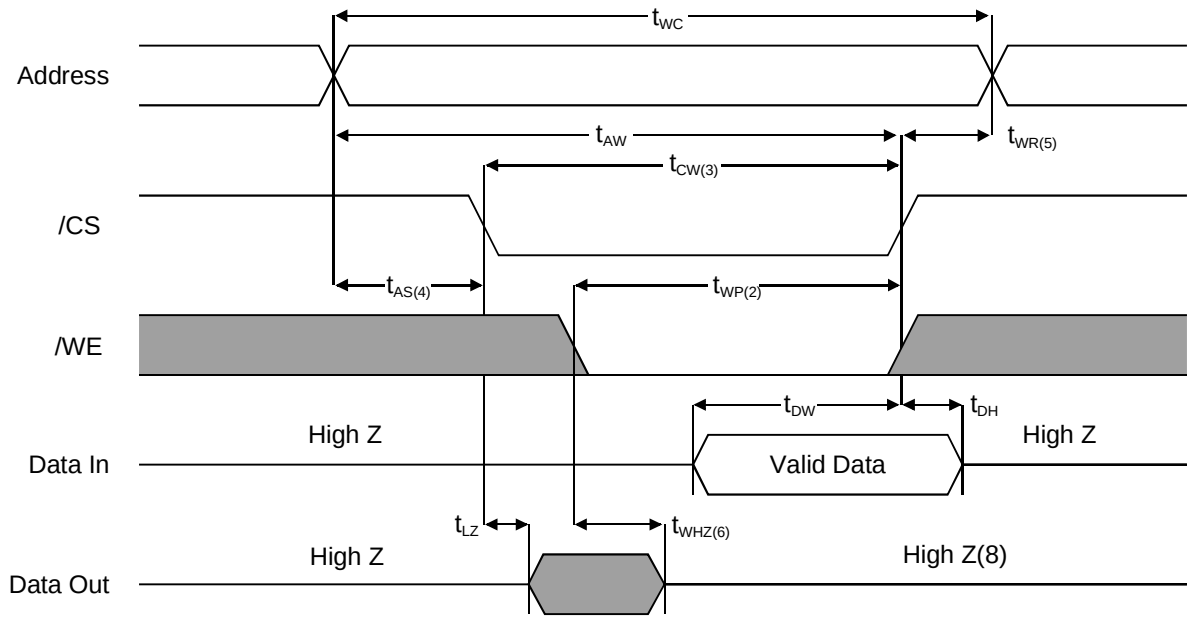
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
11. /CS=/CS1~4

Write Cycle 3

(/CS = Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
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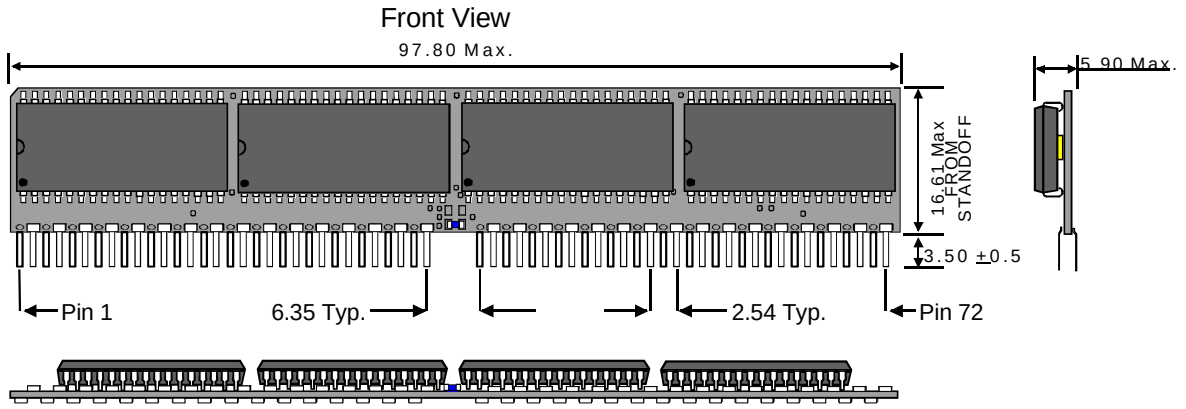
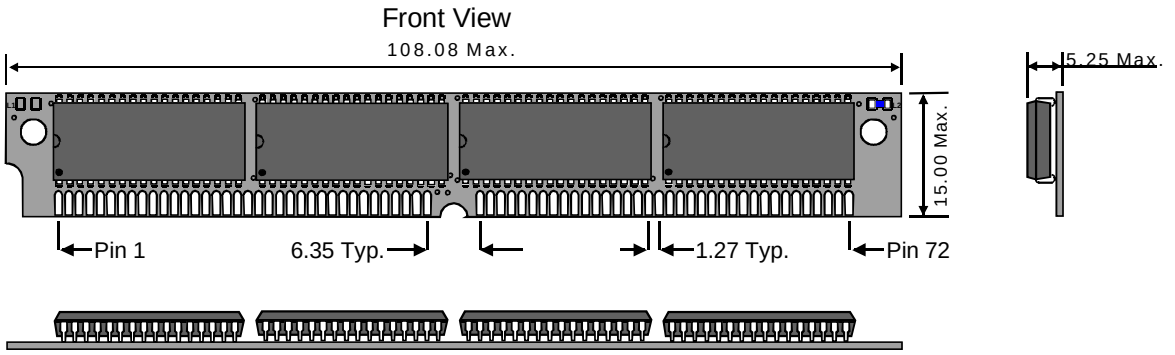
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
11. /CS=/CS1~4

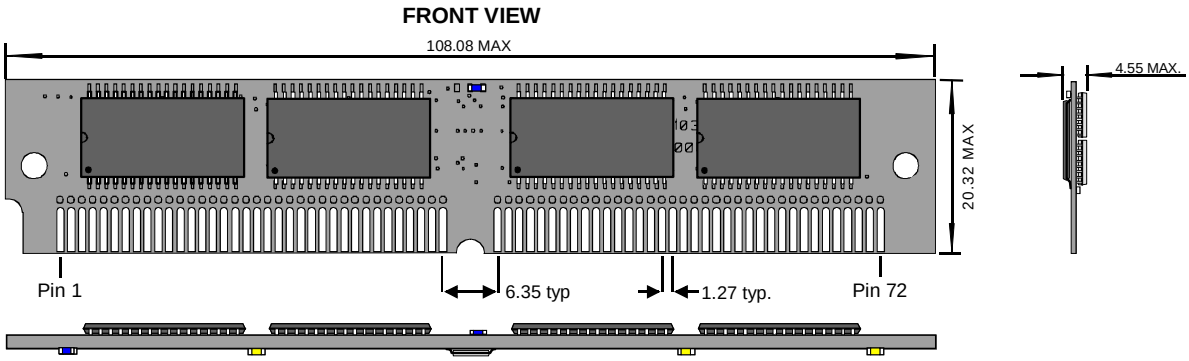
Plastic 72 pin ZIP (ZK)



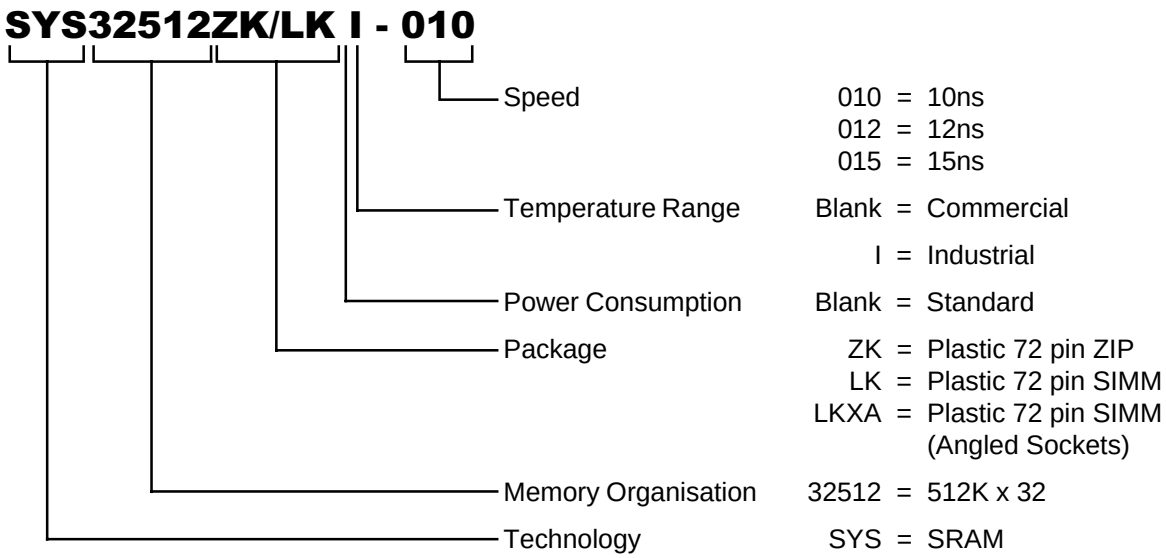
Plastic 72 pin SIMM (LK)



Plastic 72 pin SIMM (LKXA)



Ordering Information



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Our products are subject to a constant process of development. Data may be changed without notice.
Products are not authorised for use as critical components in life support devices without the express written approval of a company director.