AsahiKASEI
ASAHI KASEI EMD

AKD4671-B
Evaluation board Rev.0 for AK4671

GENERAL DESCRIPTION

AKD4671 is an evaluation board for the AK4671, stereo CODEC with built-in Microphone-Amplifier, Receiver-Amplifier and Headphone-Amplifier.
The AKD4671 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The AKD4671-B also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4671 --- Evaluation board for AK4671
(Cable for connecting with printer port of IBM-AT,compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **10pin Header for Digital Audio I/F, PCM I/F (Baseband, Bluetooth)**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

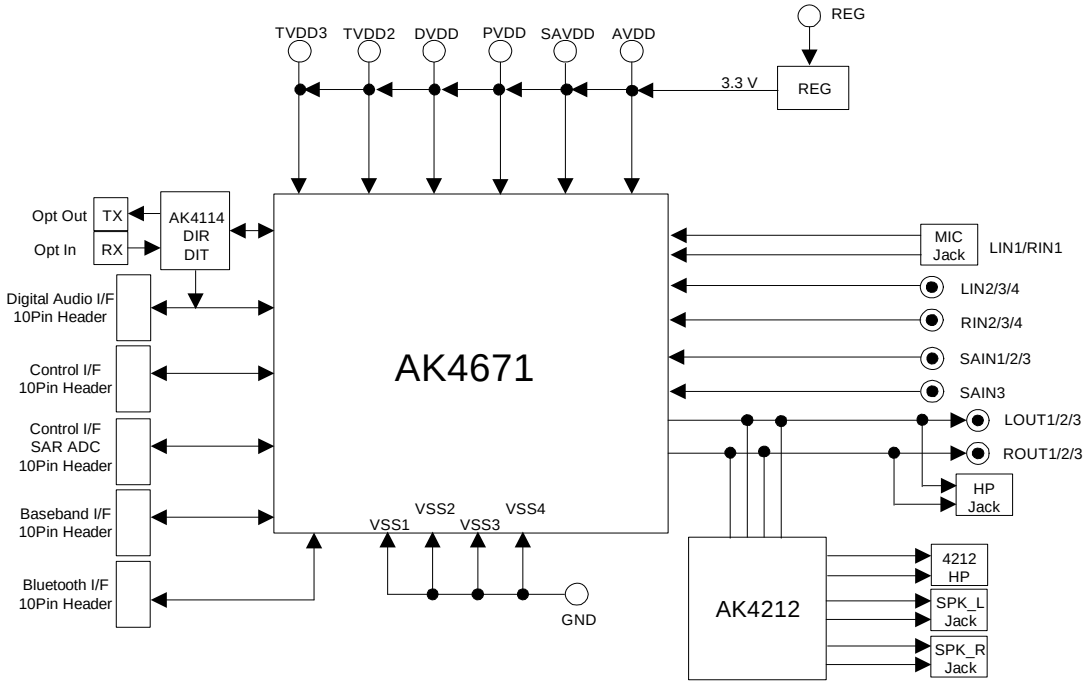


Figure 1. AKD4671-B Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

(1-1) In case of using the regulator.

Set up the jumper pins.

JP	JP18	JP20	JP22	JP24	JP26	JP27	JP29	JP31	JP7
	SVDD SEL	AVDD SEL	SAVDD SEL	PVDD SEL	DVDD SEL	TVDD2 SEL	TVDD3 SEL	VCC SEL	VCC2 SEL
State	Short	Short	Short	Short	Short	Short	Short	Short	Short

Set up the power supply lines.

[REG] (red) = 5.0V : for regulator (3.3V output : AK4671 , Logic)
[D3V] (orange) = 2.7 ~ 3.6V : for AK4114 and logic (typ. 3.3V)
[AGND] (black) = 0V : for analog ground
[DGND] (black) = 0V : for logic ground

(1-2) In case of using the power supply connectors.

Set up the jumper pins.

JP	JP18	JP20	JP22	JP24	JP26	JP27	JP29	JP31	JP7
	SVDD SEL	AVDD SEL	SAVDD SEL	PVDD SEL	DVDD SEL	TVDD2 SEL	TVDD3 SEL	VCC SEL	VCC2 SEL
State	Open	Open	Open	Open	Open	Open	Open	Open	Open

Set up the power supply lines.

[SVDD] (orange) = 3.0 ~ 5.5V : for SVDD of AK4212 (typ. 3.6V)
[AVDD] (orange) = 2.2 ~ 3.6V : for AVDD of AK4671 (typ. 3.3V)
[SAVDD] (orange) = 2.2 ~ 3.6V : for SAVDD of AK4671 (typ. 3.3V)
[PVDD] (orange) = 2.2 ~ 3.6V : for PVDD of AK4671 (typ. 3.3V)
[DVDD] (orange) = 1.6 ~ 3.6V : for DVDD of AK4671 (typ. 3.3V)
[TVDD2] (orange) = 1.6 ~ 3.6V : for TVDD2 of AK4671 (typ. 3.3V)
[TVDD3] (orange) = 1.6 ~ 3.6V : for TVDD3 of AK4671 (typ. 3.3V)
[VCC] (orange) = 1.6 ~ 3.6V : for logic (typ. 3.3V : the voltage same as DVDD)
[VCC2] (orange) = 1.6 ~ 3.6V : for logic (typ. 3.3V : the voltage same as TVDD2 and TVDD3)
[D3V] (orange) = 2.7 ~ 3.6V : for AK4114 and logic (typ. 3.3V)
[AGND] (black) = 0V : for analog ground
[DGND] (black) = 0V : for logic ground

* Each supply line should be distributed from the power supply unit.

2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.

The AK4671 and AK4114 should be reset once bringing SW1 (DIR) and SW2 (PDN) “L” upon power-up.

■ Evaluation mode

1. Audio I/F evaluation mode

In case of AK4671 evaluation using AK4114, it is necessary to correspond to audio interface format for AK4671 and AK4114. About AK4671's audio interface format, refer to datasheet of AK4671. About AK4114's audio interface format, refer to Table 2 on page 19.
The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, please use other mode.
In addition, MCLK of AK4114 supports 256fs and 512fs. When evaluate it in a condition except this, please use other modes

(1) External Slave Mode
(1-1) Evaluation of A/D using DIT of AK4114
(1-2) Evaluation of D/A using DIR of AK4114
(1-3) Evaluation of Loop-back using AK4114 <default>
(1-4) Evaluation of Loop-back that master clock is fed externally, BICK and LRCK are divided with a board
(1-5) All interface signals including master clock are fed externally

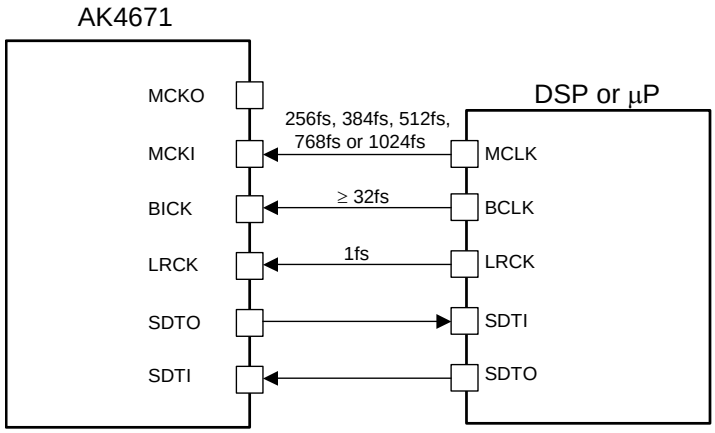
(2) External Master Mode
(2-1) Evaluation of A/D using DIT of AK4114
(2-2) Evaluation of D/A using DIR of AK4114
(2-3) Evaluation of Loop-back using AK4114
(2-4) All interface signals including master clock are fed externally

(3) PLL Slave Mode
(3-1) PLL Reference Clock : MCKI pin
(3-1-1) Evaluation of A/D using DIT of AK4114
(3-1-2) Evaluation of Loop-back using AK4114
(3-1-3) All interface signals including master clock are fed externally
(3-2) PLL Reference Clock : BICK or LRCK pin
(3-2-1) Evaluation of A/D using DIT of AK4114
(3-2-2) Evaluation of D/A using DIR of AK4114
(3-2-3) Evaluation of Loop-back using AK4114
(3-2-4) All interface signals including master clock are fed externally

(4) PLL Master Mode
(4-1) Evaluation of A/D using DIT of AK4114
(4-2) Evaluation of Loop-back
(4-3) All interface signals including master clock are fed externally

(1) External Slave Mode

When PMPLL bit is "0", the AK4671 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 384fs, 512fs, 768fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits.



(1-1) Evaluation of A/D using DIT of AK4114

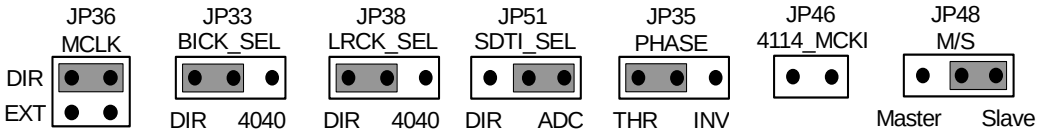
X2 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT4 (DSP).
The jumper pins should be set as the following.

(1-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.

(1-3) Evaluation of Loop-back using AK4114 <default>

X2 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.



(1-4) Evaluation of Loop-back where master clock is fed externally, BICK and LRCK are generated by on-board divider.

J12 (EXT) is used . MCLK is supplied from J12 (EXT). BICK and LRCK are generated by 74HC4040 on AKD4671-B.
Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.

When a termination (51Ω) is unnecessary, please set JP39 (EXT) open.

JP32 (MKFS), JP34 (BCFS), and JP37 (LRCK) should be set according to the frequency of MCLK, BICK and LRCK.
Follows are setting examples in MCLK=256fs , BICK=64fs and LRCK=1fs.
When MCLK=384fs or 768fs, JP32, JP34, and JP37 should be set to "384" side.

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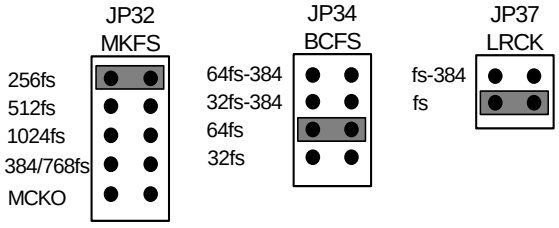
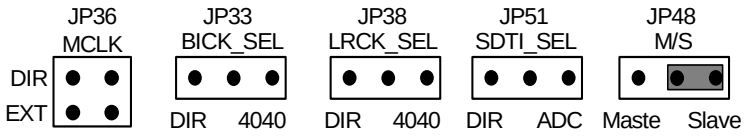


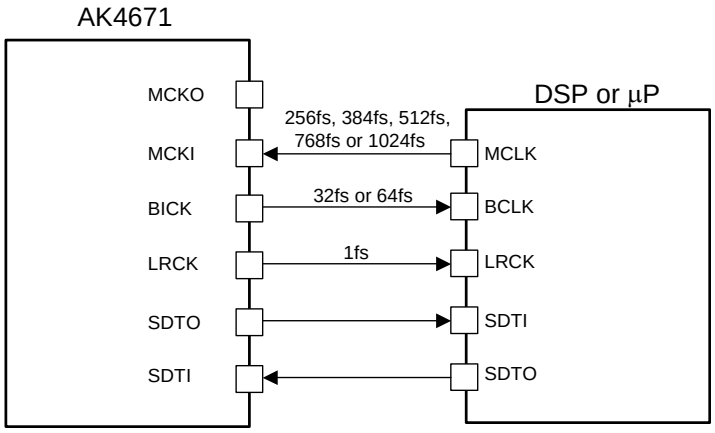
(1-5) All interface signals including master clock are fed externally

PORT4 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as the following.



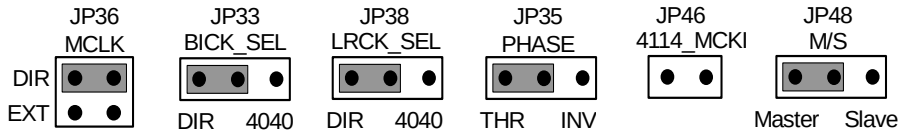
(2) External Master Mode

The AK4671 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input via MCKI pin, without using on-chip PLL circuit. The clock required to operate is MCKI (256fs, 384fs, 512fs, 768fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits.



(2-1) Evaluation of A/D using DIT of AK4114

X2 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT4 (DSP).
In Master Mode, BICK and LRCK of AK4671 should be input to AK4114. Please refer to Table 2 on page 19.
The jumper pins should be set as the following.

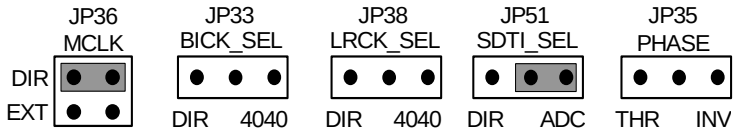


(2-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT4 (DSP).
In Master Mode, BICK and LRCK of AK4671 should be input to AK4114. Please refer to Table 2 on page 19.
The jumper pins should be set as the following.

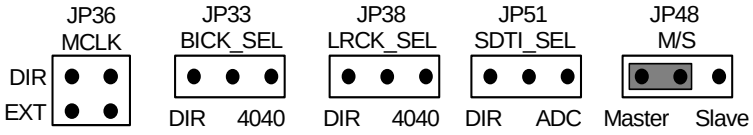
(2-3) Evaluation of Loop-back using AK4114

X'tal (X2) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.



(2-4) All interface signals including master clock are fed externally

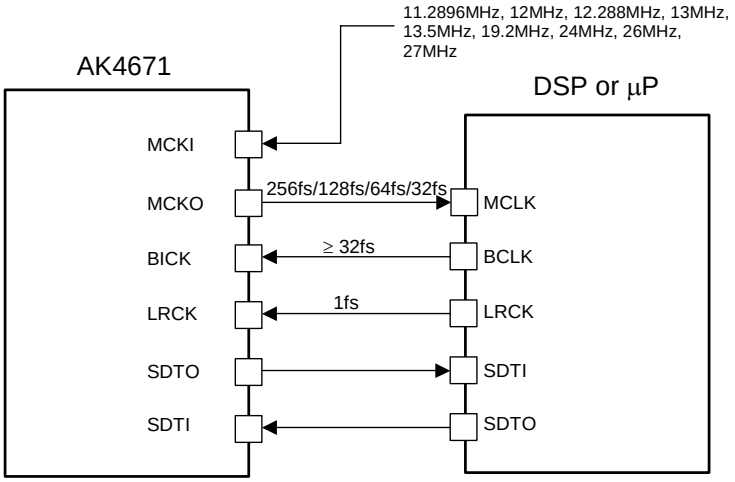
PORT4 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as the following.



(3) PLL Slave Mode

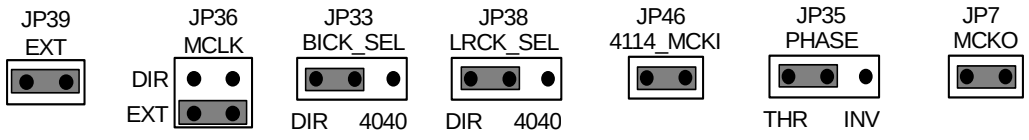
A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock to the AK4671 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits.
BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits and the output is enabled by MCKO bit.
Sampling frequency can be selected by FS3-0 bits.

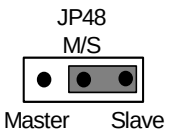
(3-1) PLL Reference Clock : MCKI pin



(3-1-1) Evaluation of A/D using DIT of AK4114

J12 (EXT) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT4 (DSP).
X'tal oscillator should be removed from X2.
The jumper pins should be set as the following.

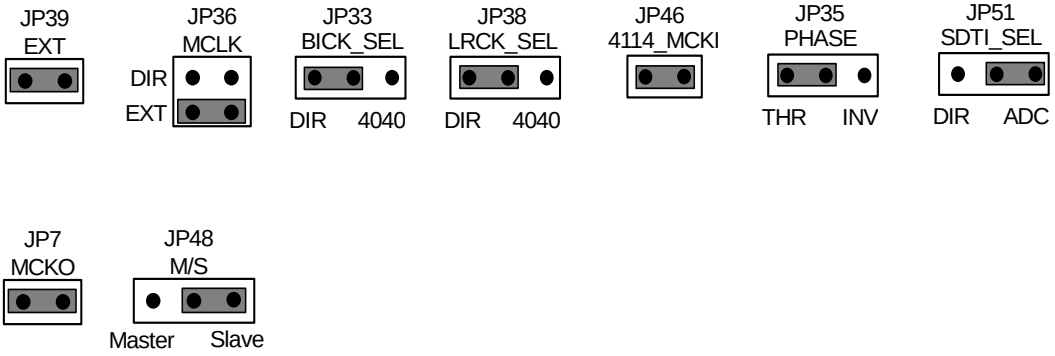




When a termination (51Ω) is unnecessary, please set JP39 (EXT) to open.

(3-1-2) Evaluation of Loop-back using AK4114

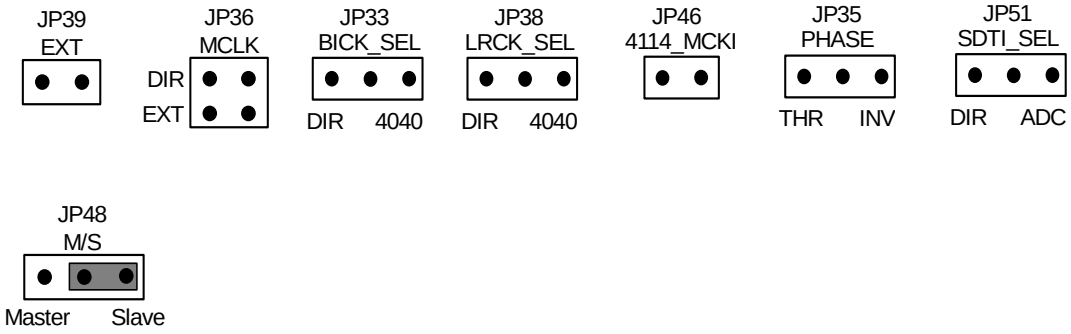
J12 (EXT) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
X'tal oscillator should be removed from X2.
The jumper pins should be set as the following.



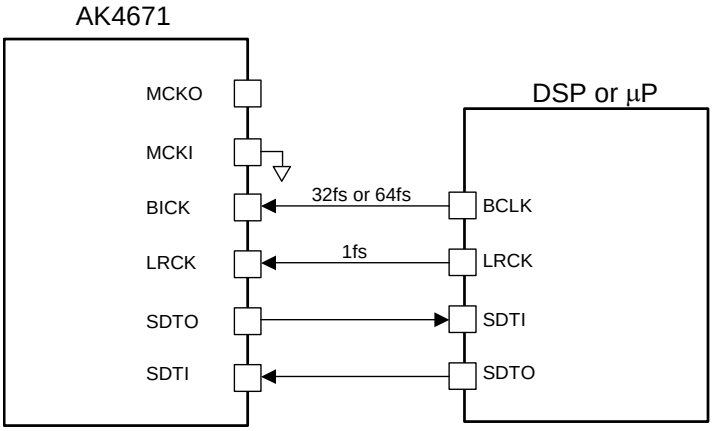
When a termination (51Ω) is unnecessary, please set JP39 (EXT) open.

(3-1-3) All interface signals including master clock are fed externally

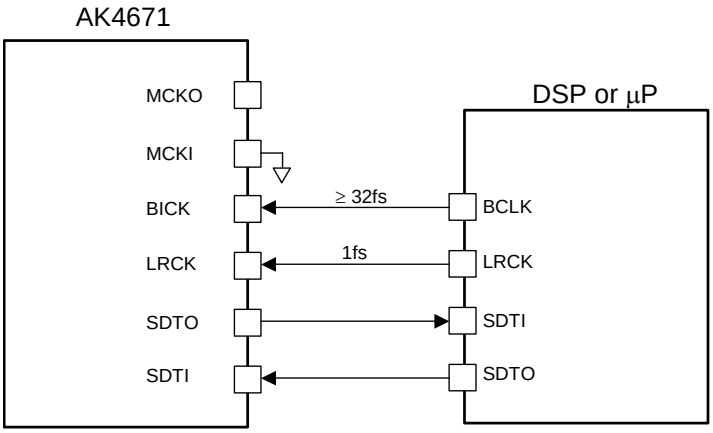
PORT4 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as the following.



(3-2) PLL Reference Clock : BICK or LRCK pin



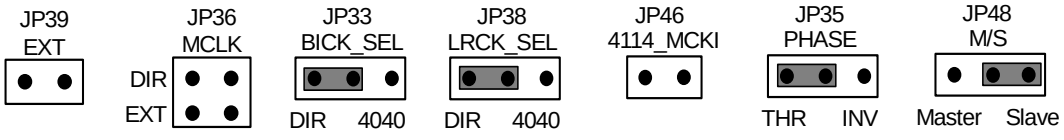
(PLL Reference Clock: BICK pin)



(PLL Reference Clock: LRCK pin)

(3-2-1) Evaluation of A/D using DIT of AK4114

X2 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT4 (DSP). The jumper pins should be set as the following.

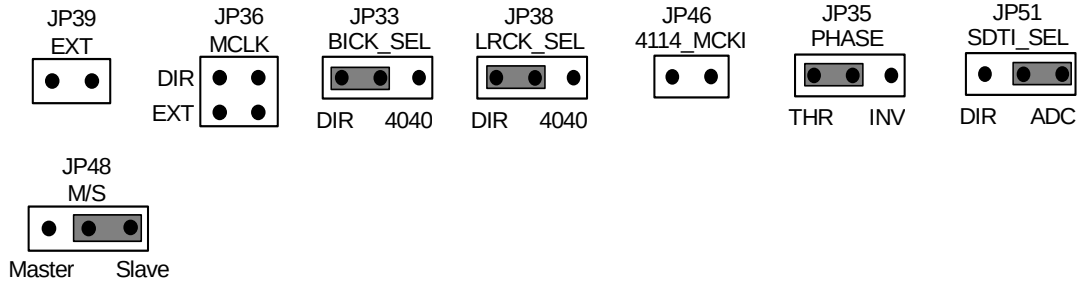


(3-2-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.

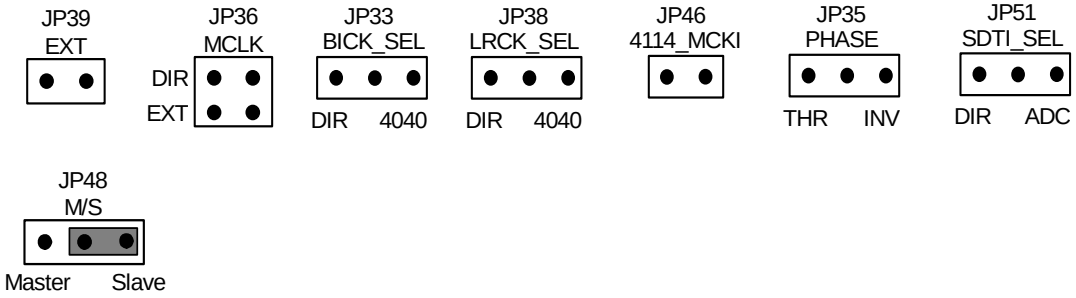
(3-2-3) Evaluation of Loop-back using AK4114

X2 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
The jumper pins should be set as the following.



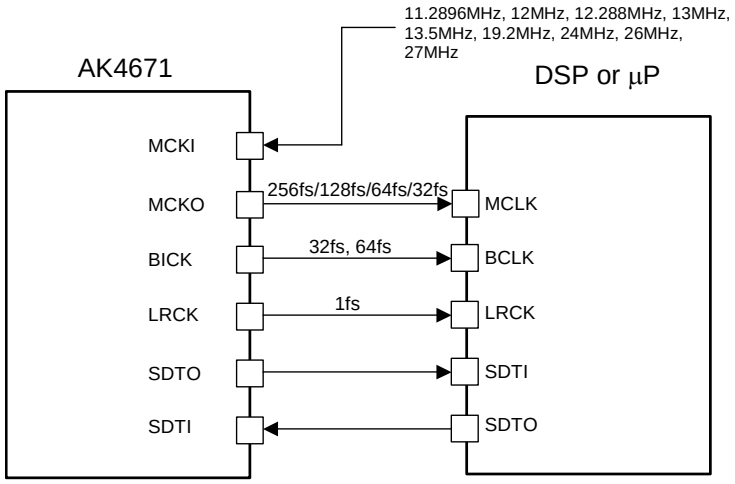
(3-2-4) All interface signals including master clock are fed externally

PORT4 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as the following.



(4) PLL Master Mode

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit.



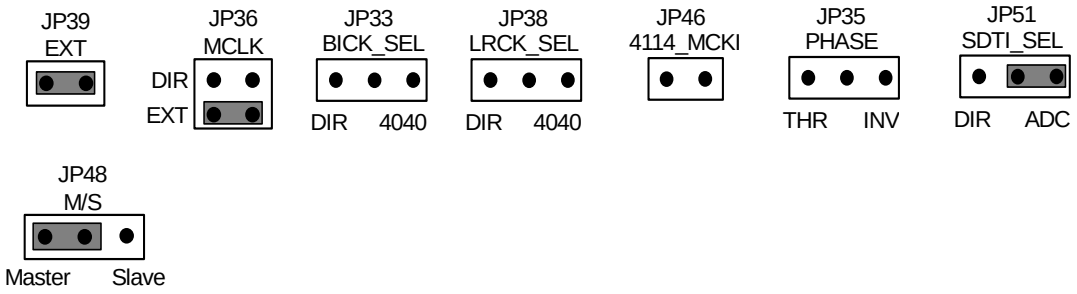
(4-1) Evaluation of A/D using DIT of AK4114

J12 (EXT) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT4 (DSP).
X'tal oscillator should be removed from X2.
In Master Mode, BICK and LRCK of AK4671 should be input to AK4114. Please refer to Table 2 on page 19.
The jumper pins should be set as the following.

When a termination (51Ω) is unnecessary, please set JP39 (EXT) open.

(4-2) Evaluation of Loop-back

J12 (EXT) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT4 (DSP).
X'tal oscillator should be removed from X2.
The jumper pins should be set as the following.



When a termination (51Ω) is unnecessary, please set JP39 (EXT) open.

(4-3) All interface signals including master clock are fed externally

PORT4 (DSP) is used. Nothing should be connected to PORT1 (DIR) and PORT2 (DIT).
The jumper pins should be set as the following.

2. PCM I/F evaluation mode

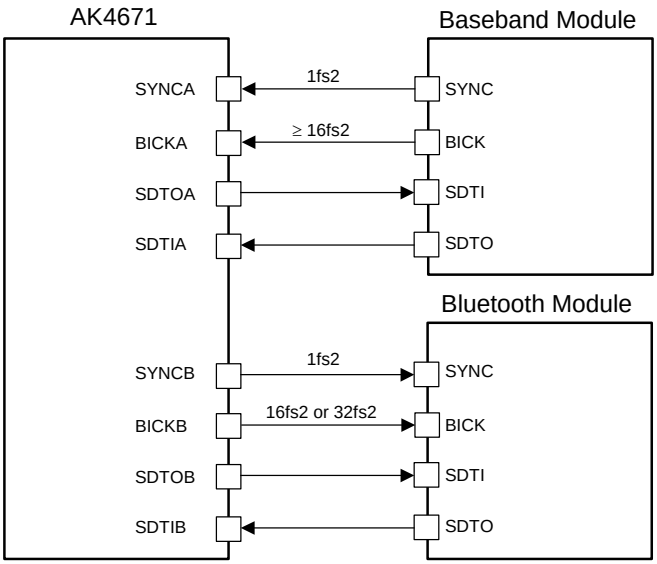
A reference clock of PLLBT is selected among the input clocks to SYNCA, BICKA, SYNCB or BICKB pin. The required clock to PCM I/F is generated by an internal PLLBT circuit. PLLBT circuit is powered up by PMPCM bit. Input frequency is selected by PLLBT2-0 bits. BCKO2 bit select the output clock frequency of BICKA or BICKB pin.
AK4671 does not support master mode for both PCM I/F A and B nor slave mode for both PCM I/F A and B. When PMPCM bit is "0", SYNCA, BICKA, SYNCB and BICKB pins are Hi-Z.

(1) PLLBT reference clock: SYNCA or BICKA pin
(1-1) SYNCA and BICKA are fed from on-board clock generator.
(1-2) SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

(2) PLLBT reference clock: SYNCB or BICKB pin
(2-1) SYNCB and BICKB are fed from on-board clock generator.
(2-2) SYNCB and BICKB are fed externally via PORT6 (Bluetooth Module).

(1) PLLBT reference clock: SYNCA or BICKA pin

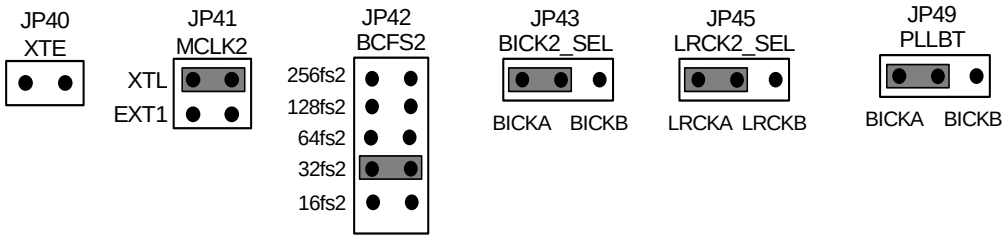
The PLLBT circuit generates the required clock for PCM I/F from SYNCA or BICKA. Generated clocks are output via SYNCB and BICKB pins.



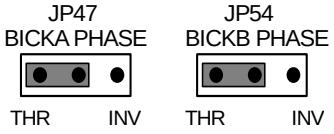
(PLLBT Reference Clock: SYNCA or BICKA pin)

(1-1) SYNCA and BICKA are fed from on-board clock generator.

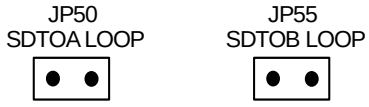
X1 (X'tal), PORT3 (Baseband Module) and PORT6 (Bluetooth Module) are used.
The jumper pins should be set as the following.
Please set JP42 (BCFS2) to the required frequency. Follows are setting in BICKA=32fs.
When clocks are supplied from J13 (EXT1) without using X1, JP41 (MCLK2) should be set to "EXT1".



JP47 (BICKA PHASE) is jumper which decides polarity of BICKA, "THR" or "INV" should be selected according to the PCM I/F format.
JP54 (BICKB PHASE) should be set to "THR".

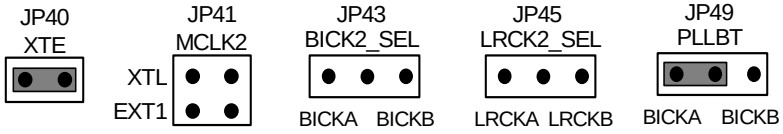


In case of loop-back "SDTOA → SDTIA" and "SDTOB → SDTIB", please set JP50 (SDTOA LOOP) and JP55 (SDTOB LOOP) short.

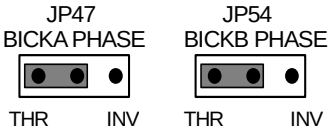


(1-2) SYNCA and BICKA are fed externally via PORT3 (Baseband Module).

PORT3 (Baseband Module) and PORT6 (Bluetooth Module) are used.
SYNCA and BICKA should be supplied from PORT3.
The jumper pins should be set as the following.

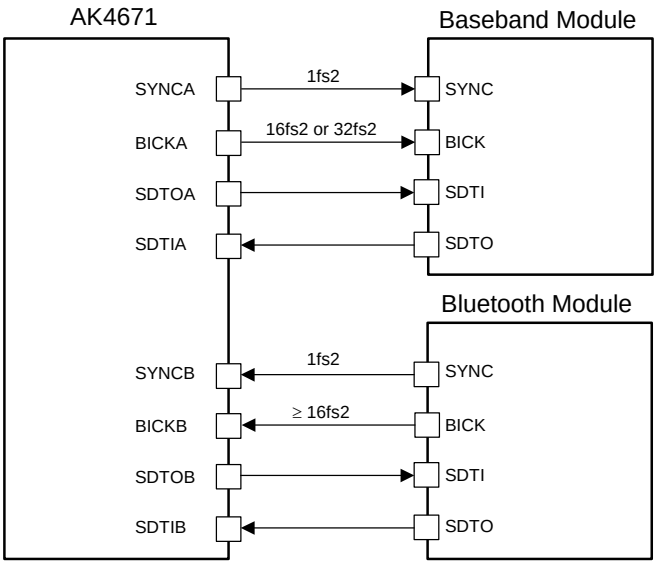


JP47 (BICKA PHASE) is jumper which decides polarity of BICKA, "THR" or "INV" should be selected according to the PCM I/F format.
JP54 (BICKB PHASE) should be set to "THR".



(2) PLLBT reference clock: SYNCB or BICKB pin

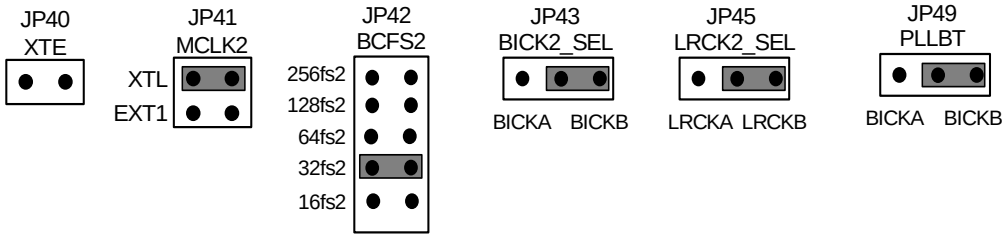
The PLLBT circuit generates the required clock for PCM I/F from SYNCB or BICKB. Generated clocks are output via SYNCA and BICKA pins.



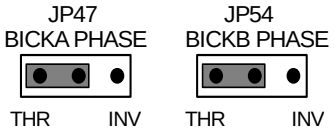
(PLLBT Reference Clock: SYNCB or BICKB pin)

(2-1) SYNCB and BICKB are fed from on-board clock generator.

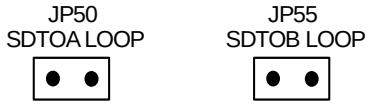
X1 (X'tal), PORT3 (Baseband Module) and PORT6 (Bluetooth Module) are used.
The jumper pins should be set as the following.
Please set JP42 (BCFS2) to the required frequency. Follows are setting in BICKB=32fs.
When clocks are supplied from J13 (EXT1) without using X1, JP41 (MCLK2) should be set to "EXT1".



JP54 (BICKB PHASE) is jumper which decides polarity of BICKB, "THR" or "INV" should be selected according to the PCM I/F format.
JP47 (BICKA PHASE) should be set to "THR".

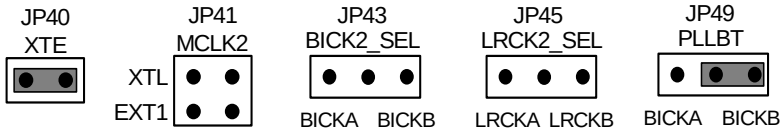


In case of loop-back "SDTOA → SDTIA" and "SDTOB → SDTIB", please set JP50 (SDTOA LOOP) and JP55 (SDTOB LOOP) short.

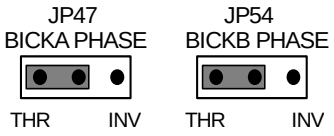


(2-2) SYNCB and BICKB are fed externally via PORT6 (Bluetooth Module).

PORT3 (Baseband Module) and PORT6 (Bluetooth Module) are used.
Please supply SYNCB and BICKB from PORT6.
The jumper pins should be set as the following.



JP54 (BICKB PHASE) is jumper which decides polarity of BICKB, "THR" or "INV" should be selected according to the PCM I/F format.
JP47 (BICKA PHASE) should be set to "THR".



■ DIP Switch set up

[S1] (SW DIP-6): Mode setting for AK4671 and AK4114.

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Audio Format Setting See Table 2		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	AK4114 Master Clock Setting : See Table 3		OFF
5	CAD0	AK4671 Control Mode Setting See Table 4		OFF
6	I2C			ON

Table 1. Mode Setting for AK4671 and AK4114

DIF2	DIF1	DIF0	DAUX	SDTO	LRCK		BICK		
0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	Default
1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 2. Setting for AK4114 Audio Interface Format

OCKS1	MCKO1	X'tal	
0	256fs	256fs	Default
1	512fs	512fs	

Table 3. Setting for AK4114 Master Clock

■ Other jumper pins set up

Sub Board

[JP1] (RIN2) : RIN2 input.
GND : In case of full-differential input.
MPWR : MIC-power is supplied to RIN2.
OPEN : MIC-power is not supplied to RIN2. <Default>

[JP2] (LIN1) : LIN1 input.
SHORT : MIC-power is supplied to LIN1.
OPEN : MIC-power is not supplied to LIN1. <Default>

[JP3] (LIN2) : LIN2 input.
SHORT : MIC-power is supplied to LIN2.
OPEN : MIC-power is not supplied to LIN2. <Default>

[JP4] (RIN1) : RIN1 input.
GND : In case of full-differential input.
MPWR : MIC-power is supplied to RIN1.
OPEN : MIC-power is not supplied to RIN1. <Default>

[JP5] (PVDD) : PVDD of AK4212 power supply.
SHORT : PVDD is supplied from "PVDD" jack. <Default>
OPEN : PVDD is not supplied from "PVDD" jack

[JP6] (PDN) : PDN of AK4212.
SHORT : PDN is supplied from SW2 (PDN). <Default>
OPEN : PDN is not supplied from SW2 (PDN).

[JP7] (MCKO) : MCKO output.
SHORT : When AK4671 outputs MCKO. <Default>
OPEN : When AK4671 does not output MCKO.

[JP8] (SDA) : SDA of AK4212.
SHORT : SDA is supplied from PORT5 (CTRL). <Default>
OPEN : SDA is not supplied from PORT5 (CTRL).

[JP9] (SCL) : SCL of AK4212.
SHORT : SCL is supplied from PORT5 (CTRL). <Default>
OPEN : SCL is not supplied from PORT5 (CTRL).

[JP10] (TVDD) : TVDD of AK4212 power supply.
SHORT : TVDD is supplied from "DVDD" jack. <Default>
OPEN : TVDD is not supplied from "DVDD" jack

[JP11] (AVDD) : AVDD of AK4212 power supply.
SHORT : AVDD is supplied from "AVDD" jack. <Default>
OPEN : AVDD is not supplied from "AVDD" jack

[JP12] (U2 RIN1) : RIN1 of AK4212 input
SHORT : RIN1 is supplied from ROUT2. <Default>
OPEN : RIN1 is not supplied from ROUT2.

[JP13] (U2 LIN1) : LIN1 of AK4212.
SHORT : LIN1 is supplied from LOUT2. <Default>
OPEN : LIN1 is not supplied from LOUT2.

[JP14] (U2 SPRIN) : SPRIN of AK4212.
SHORT : SPRIN is supplied from ROUT3. <Default>
OPEN : SPRIN is not supplied from ROUT3.

[JP15] (U2 SPLIN) : SPLIN of AK4212.
SHORT : SPLIN is supplied from LOUT3. <Default>
OPEN : SPLIN is not supplied from LOUT3.

Main Board

[JP30] (GND) : AGND and DGND.
SHORT : Common. <Default>
OPEN : Separated.

[JP46] (4114_MCKI) : MCKI of AK4114.
SHORT : MCKO of AK4671.
OPEN : X'tal (X2). <Default>

[JP56] (D3V) : Power supply of PORT7
SHORT : It is supplied from "D3V" jack.
OPEN : It is not supplied from "D3V" jack. <Default>

[JP57] (I2C PIN) : AK4671 I2C input.
I2C : It is supplied from S1 (I2C). <Default>
MCLK2 : It is supplied from MCLK2.

■ The function of the toggle SW

[SW2] (PDN) : Power down of AK4671. Keep "H" during normal operation.

[SW1] (DIR) : Power down of AK4114. Keep "H" during normal operation.
Keep "L" when AK4114 is not used.

■ Indication for LED

[LED1] (ERF) : Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4671 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT5 (CTRL) with PC by 10 wire flat cable packed with the AKD4671.Table 4 shows switch and jumper settings for serial control. I2C Mode should be selected in Table 4.

Note) When evaluate it in SAR-ADC of AK4671, 4-WIRE Mode should be selected in Table 4.

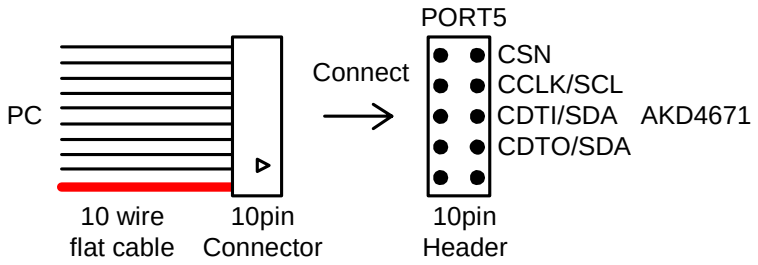


Figure 2. Connect of 10 wire flat cable

Mode		S1 (DIP SW)		JP52	JP53	
		I2C	CAD0	CTRL_SEL	CTRL_SEL2	
4-WIRE		OFF	OFF	4-WIRE	4-WIRE	
I2C	CAD0=0	ON	OFF	I2C	I2C	Default
	CAD0=1	ON	ON			

Table 4. Serial Control Setting

■ Analog Input/Output Circuits

(1) Input Circuits

(1-1) LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 Input Circuit

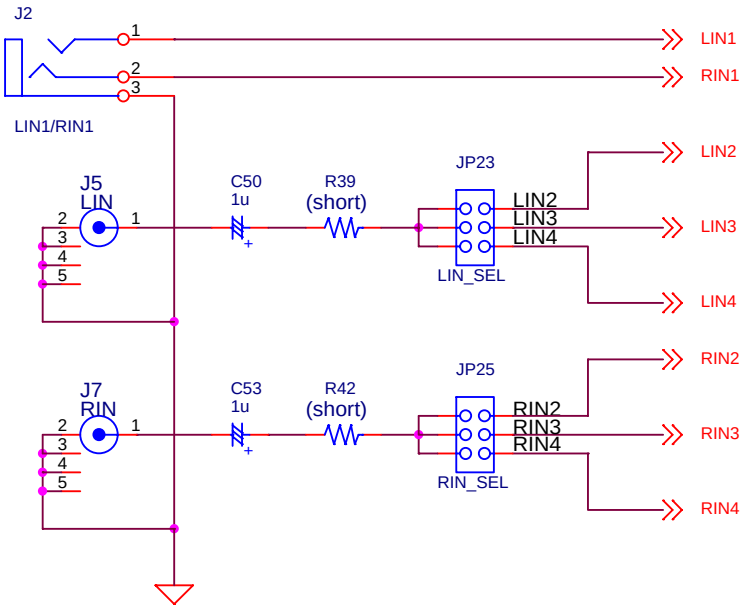


Figure 3. LIN1/RIN1, LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 Input Circuit

LIN2/RIN2, LIN3/RIN3 and LIN4/RIN4 share J5/J7.
JP23 (LIN_SEL) and JP25 (RIN_SEL) select each path.

(1-2) SAIN1, SAIN2 and SAIN3 Input Circuit

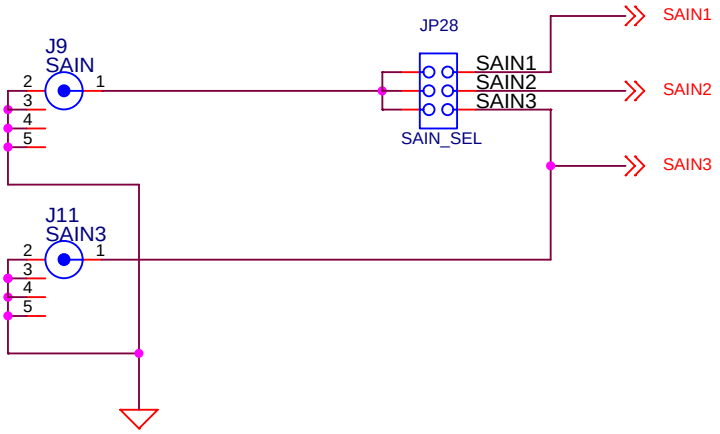


Figure 4. SAIN1, SAIN2 and SAIN3 Input Circuit

SAIN1, SAIN2 and SAIN3 share J9.
JP28 (SAIN_SEL) select each path.

(2) Output Circuits

(2-1) LOUT1/ROUT1, LOUT2/ROUT2 and LOUT3/ROUT3 Output Circuit

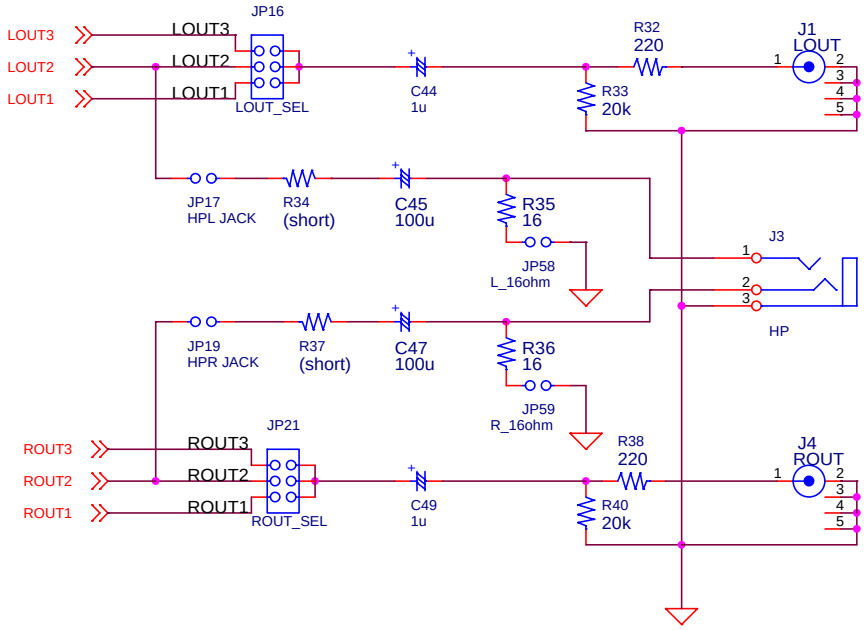


Figure 5. LOUT1/ROUT1, LOUT2/ROUT2 and LOUT3/ROUT3 Output Circuit

LOUT1/ROUT1, LOUT2/ROUT2 and LOUT3/ROUT3 share J1/J4.
JP16 (LOUT_SEL) and JP21 (ROUT_SEL) select each path.

(2-2) Headphone of AK4212 Output Circuit

JP13 (U2LIN1) and JP12 (U2RIN1) on sub board should be shorted, and LOUT2S and ROUT2S signal should be input to Headphone-Amp block of AK4212.

Figure 6. Headphone of AK4212 Output Circuit

(2-3) Speaker of AK4212 Output Circuit

JP15 (U2SPLIN) and JP14 (U2SPRIN) on sub board should be shorted, and LOUT3 and ROUT3 signal should be input to Speaker-Amp block of AK4212.

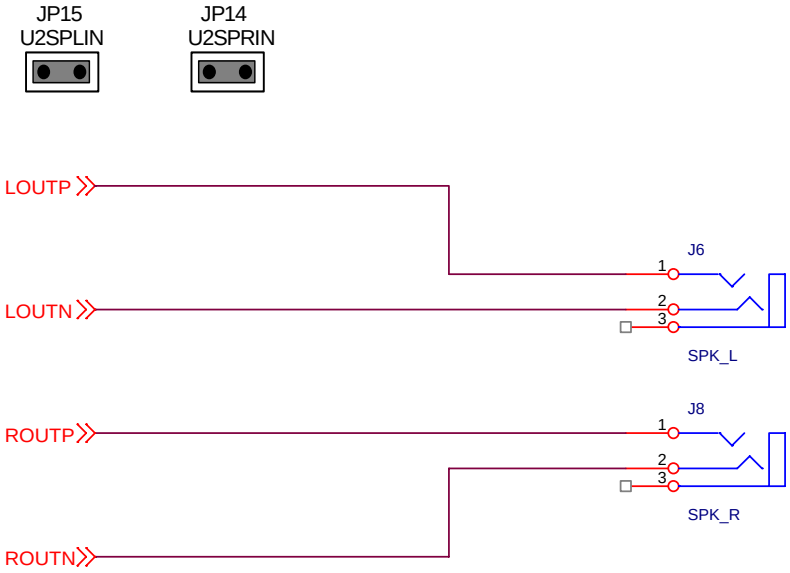


Figure 7. Speaker of AK4212 Output Circuit

* AKM assumes no responsibility for the trouble when using the above circuit examples.

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4671-B according to previous term.

2. Connect IBM-AT compatible PC with AKD4671-B by 10-line type flat cable (packed with AKD4671-B). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AKD4671-B Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4671.exe" and "AKD4212 .exe" to set up the control program. In case of evaluation using AK4212, "AKD4212 .exe" is necessary.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4671.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.
[Filter] :	Set Programmable Filter (FIL1, FIL3, EQ) of AK4671 easily.
[5 Band EQ] :	Set 5Band Equalizer of AK4671 easily.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4671, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4671, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate DATT

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4671 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4671, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

<Operation flow>
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4671. The file type is the same as [Save].

<Operation flow>
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

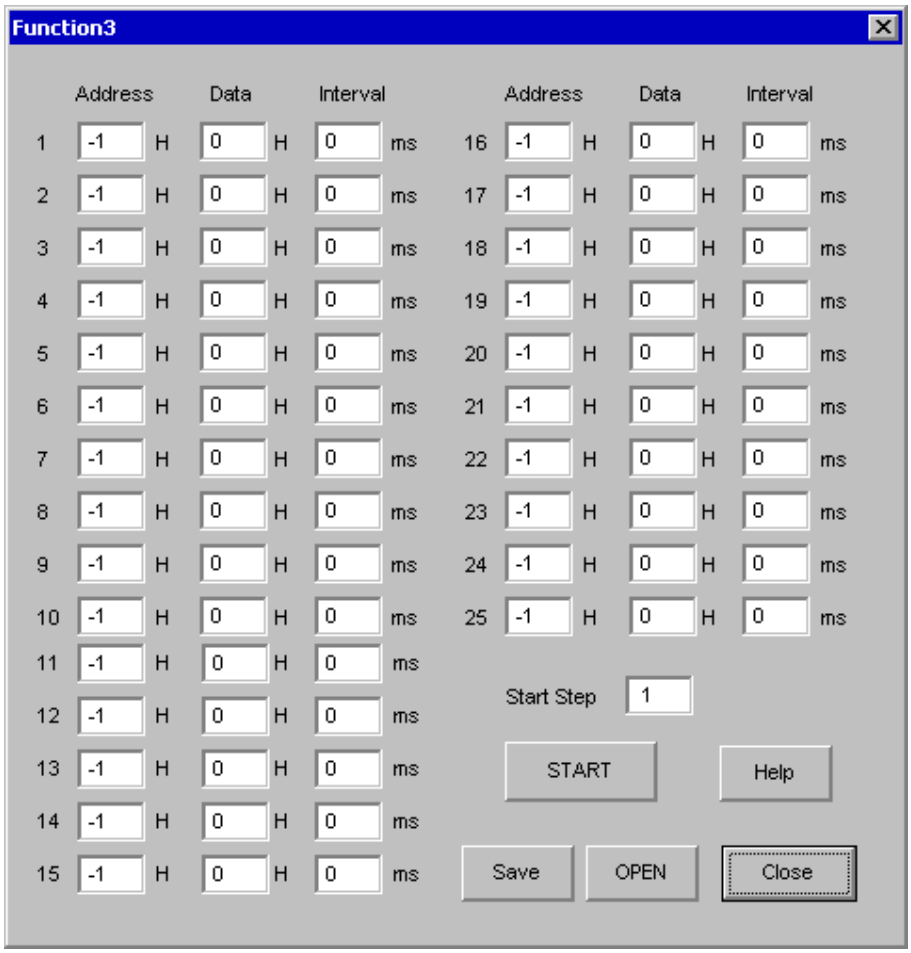


Figure 8. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 9. opens.

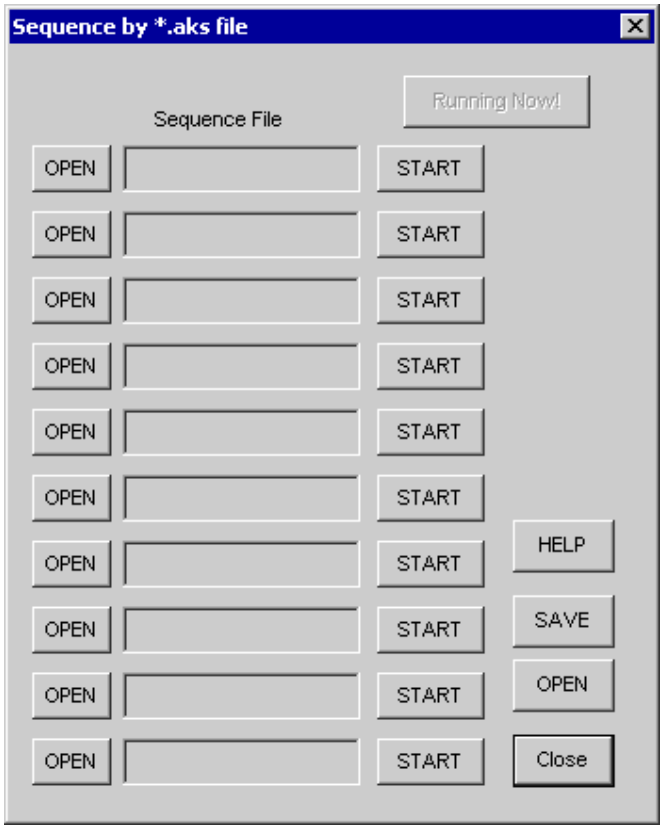


Figure 9. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 10.

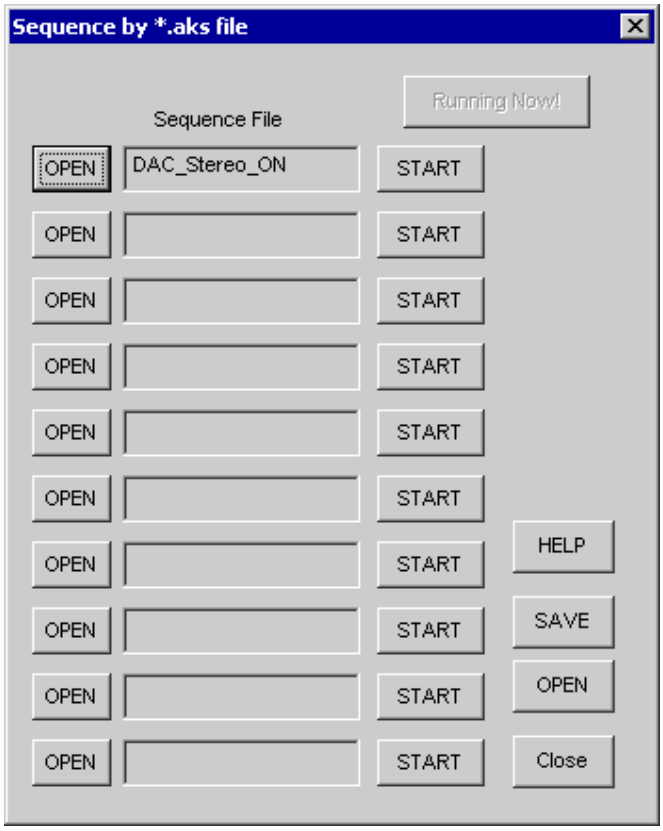


Figure 10. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 11.opens.

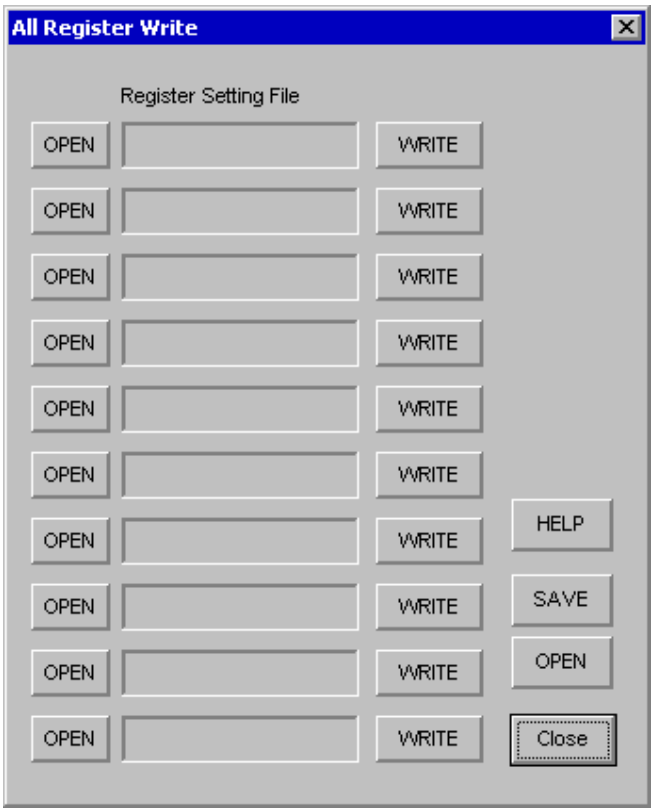


Figure 11. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 12.

(2) Click [WRITE] button, then the register setting is executed.

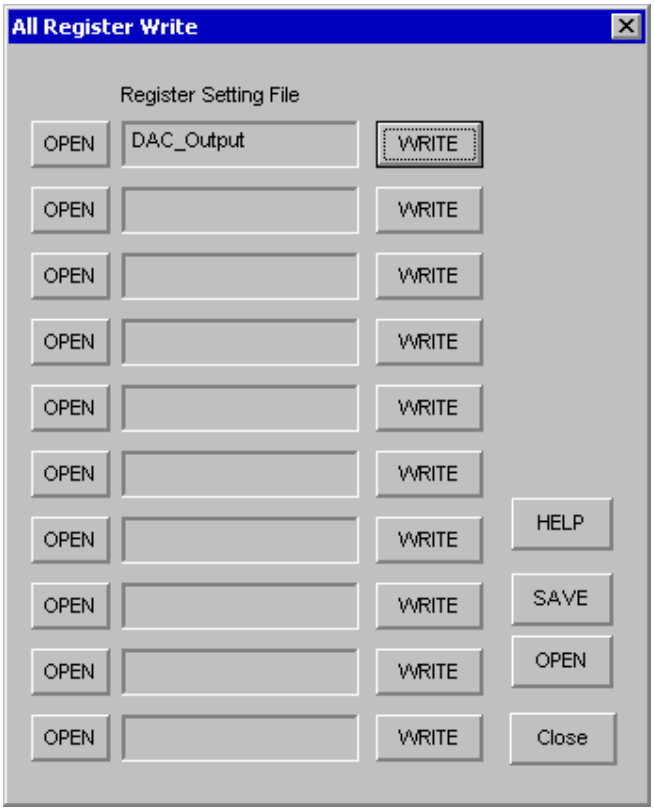


Figure 12. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

8. [Filter Dialog]

This dialog can easily set the AK4671's programmable filter.
A calculation of a coefficient of Digital Programmable Filter such as HPF,EQ filter ,a write to a register and check frequency response.
Window to show to Figure 13 opens when push a [Filter] button .

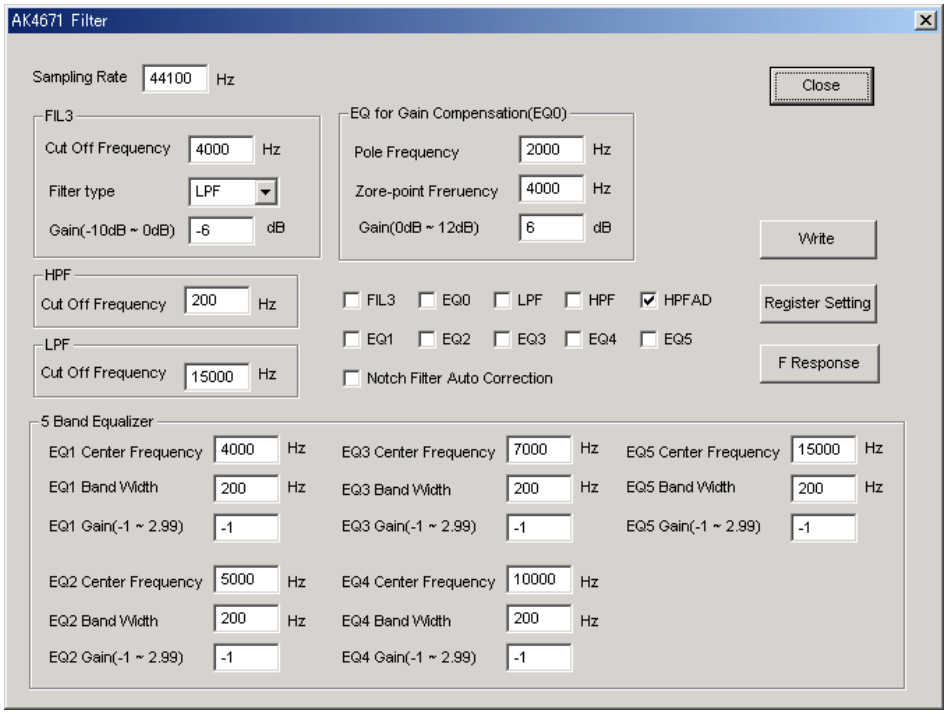


Figure 13. [Filter] window

8-1. Setting of a parameter

(1) Please set a parameter of each Filter.

Item	Contents	Setting range
Sampling Rate	Sampling frequency (fs)	7350Hz ≤ fs ≤ 48000Hz
FIL3		
Cut Off Frequency	Stereo separation emphasis filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
Filter type	Type of stereo separation emphasis filter	LPF or HPF
Gain	Gain of stereo separation emphasis filter	–10dB ≤ Gain ≤ 0dB
HPF		
Cut Off Frequency	High pass filter cut off frequency	fs/10000 ≤ Cut Off Frequency ≤ (0.497 * fs)
LPF		
Cut Off Frequency	Low pass filter cut off frequency	fs/20 ≤ Cut Off Frequency ≤ (0.497 * fs)
EQ for Gain Compensation (EQ0)		
Pole Frequency	Pole Frequency	fs/10000 ≤ Pole Frequency ≤ (0.497 * fs)
Zero-point Frequency	Zero-point Frequency	fs/10000 ≤ Zero-point Frequency ≤ (0.497 * fs)
Gain	Gain	0dB ≤ Gain ≤ +12dB
5 Band Equalizer		
EQ1-5 Center Frequency	EQ1-5 Center Frequency	0Hz ≤ Center Frequency < (0.497 * fs)
EQ1-5 Band Width	EQ1-5 Band Width (Note 1)	1Hz ≤ Band Width < (0.497 * fs)
EQ1-5 Gain	EQ1-5 Gain (Note 2)	-1≤ Gain < 3

Note 1. Bandwidth where the gain gap is 3dB compared with center frequency.
Note 2. When a gain is smaller than "0", EQ becomes a notch filter.

(2) Please set ON/OFF of Filter with check buttons of “FIL3”, “EQ0”, “LPF”, “HPF”, “HPFAD”, “EQ1”, “EQ2”, “EQ3”, “EQ4”, “EQ5”. When the button is checked, Filter becomes ON. When “Notch Filter Auto Correction” is checked, automatic compensation is executed for center frequency of notch filter.
(“Cf. 8-4. automatic compensation for center frequency of a notch filter”)

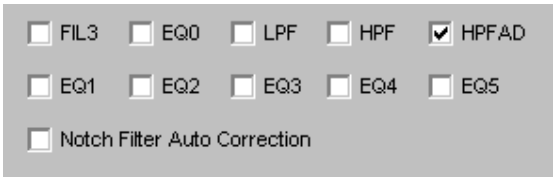


Figure14. Filter ON/OFF setting button

8-2. A calculation of a register

A register setting values are displayed when [Register Setting] button is clicked. When any value is set to out of range, error message is displayed, and a calculation of register setting is not executed.

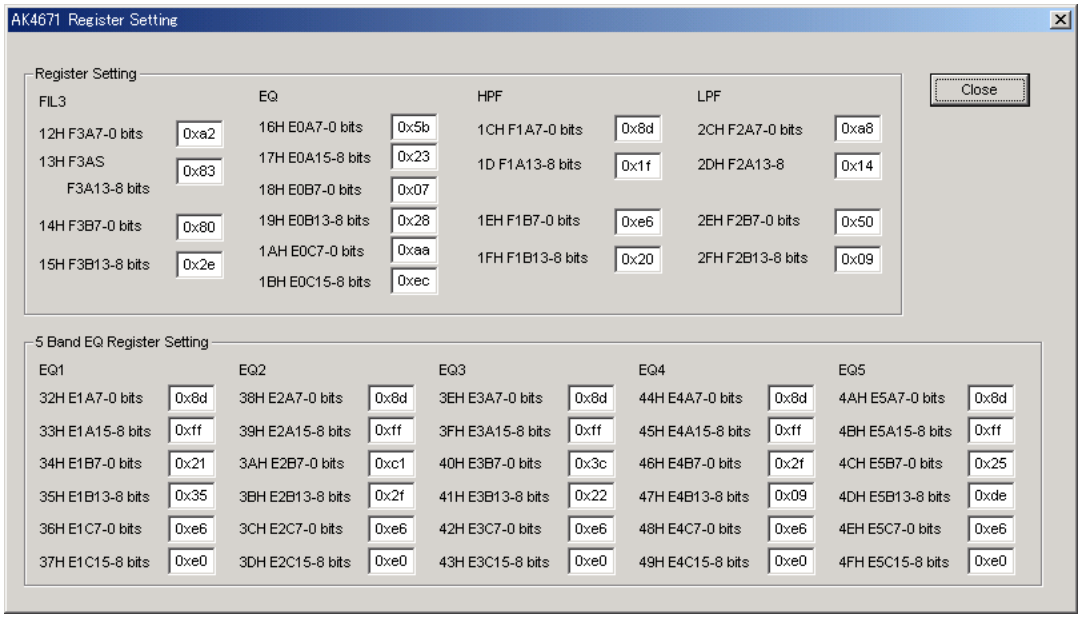


Figure15. A register setting calculation result

In the following cases, a register set values are updated.

(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

8-3.Indication of a frequency characteristic

A frequency characteristic is displayed when [Frequency Response] button is clicked. The register values are updated at the same time.
If "Frequency Range" is changed, and [UpDate] button is clicked, indication of a frequency characteristic is updated.

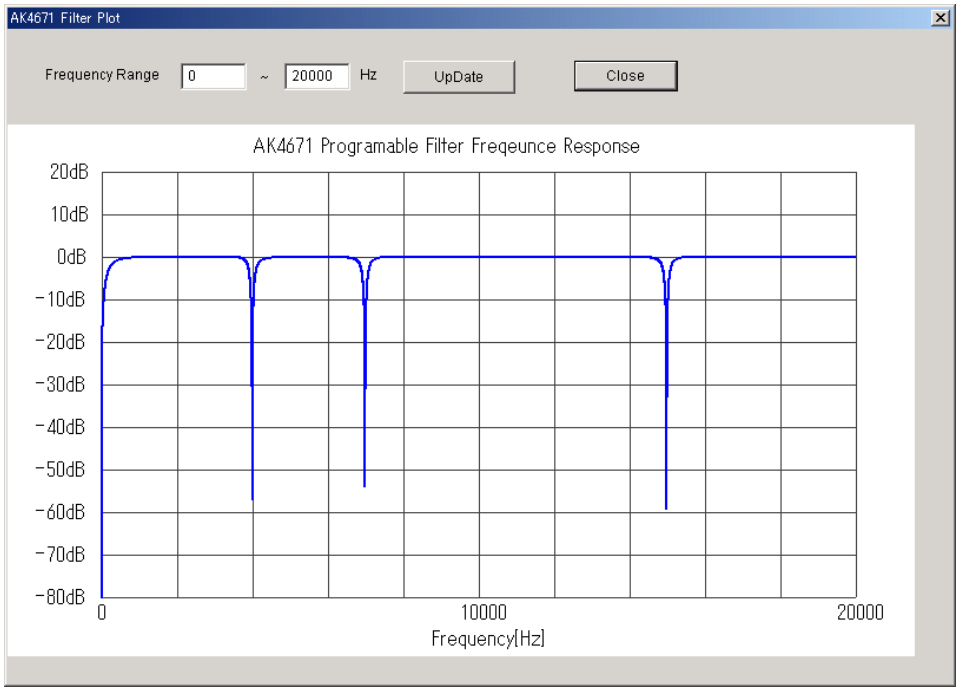


Figure16. A frequency characteristic indication result

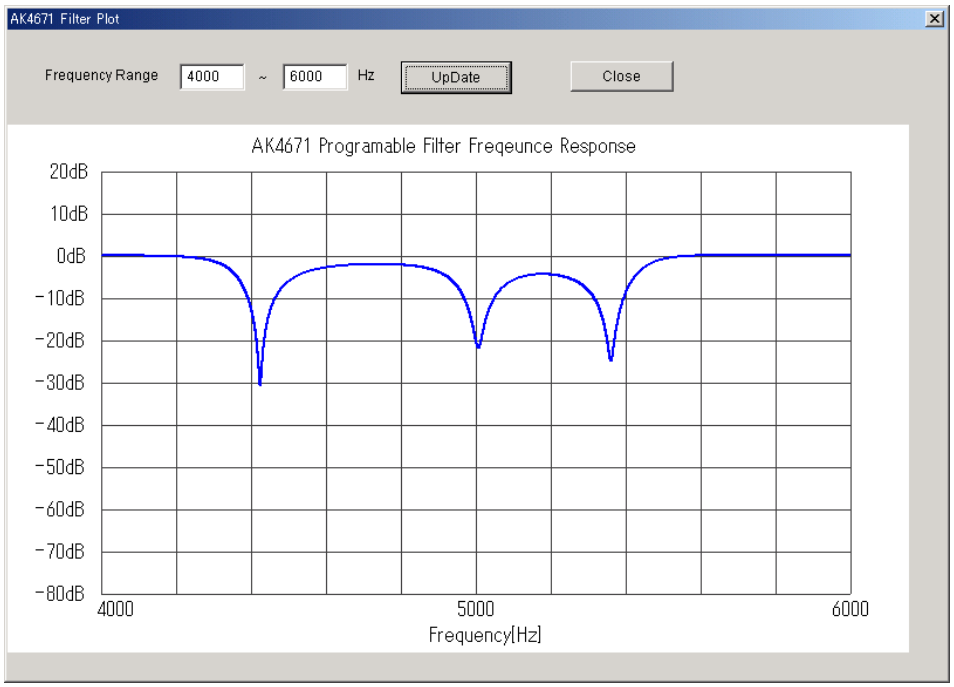
In the following cases, a register set values are updated.

(1) When [Register Setting] button was pushed.
(2) When [Frequency Response] button was pushed.
(3) When [UpDate] button was pushed on a frequency characteristic indication window.
(4) When set ON/OFF of a check button “Notch Filter Auto Correction”

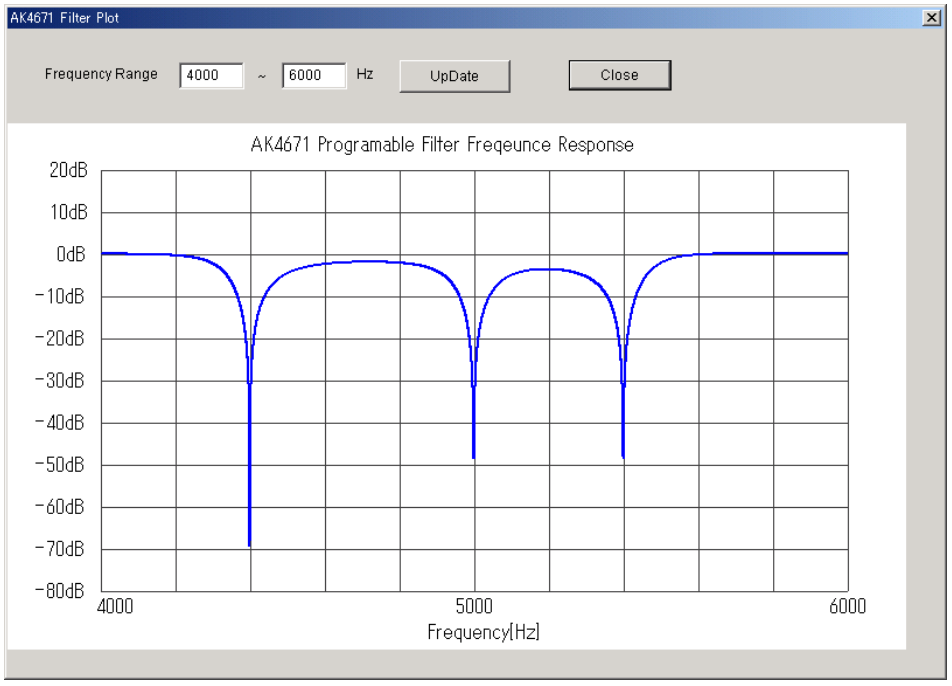
8-4. Automatic compensation for center frequency of a notch filter

When a gain of 5 band Equalizer is set to "-1", Equalizer becomes a notch filter. When center frequency of several notch filters are near frequency each other, center frequency error occurs (Figure 17).
When "Notch Filter Auto Correction" button is checked, automatic compensation is executed for center frequency of a notch filter.
Register setting and frequency characteristics are displayed after automatic compensation (Figure18).
This automatic compensation is available for EqualizerBand where a gain is set to "-1".

(Note) When distance among center frequencies is smaller than band width, there is a possibility that automatic compensation does not operate normally. Please confirm a compensation result by indication of a frequency characteristic.



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width : 200Hz(3 band common)
Figure17. When there is no compensation of center frequency



Setting of center frequency: 4400Hz, 5000Hz, 5400Hz / Band Width : 200Hz(3 band common)
Figure18. When there is compensation of center frequency

9. [5 Band EQ Dialog]

This dialog can easily set the AK4671's 5-Band Equalizer.

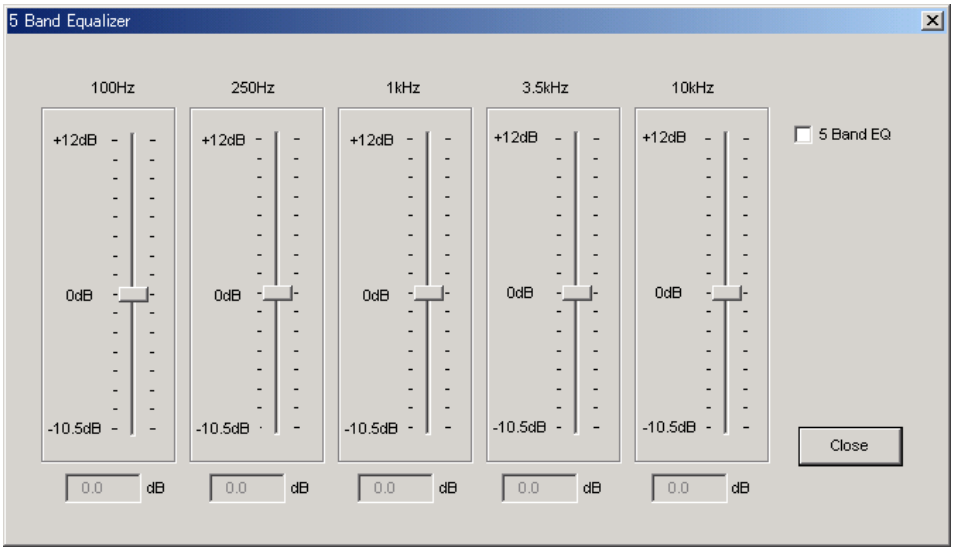


Figure 19. [5 Band EQ] window

When the check box of "5 Band EQ" is checked, 5-Band Equalizer is ON (EQ bit = "1").
When the slide button is changed, its value is written to the internal register immediately.

Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/05/15	KM089000	0	First Edition	

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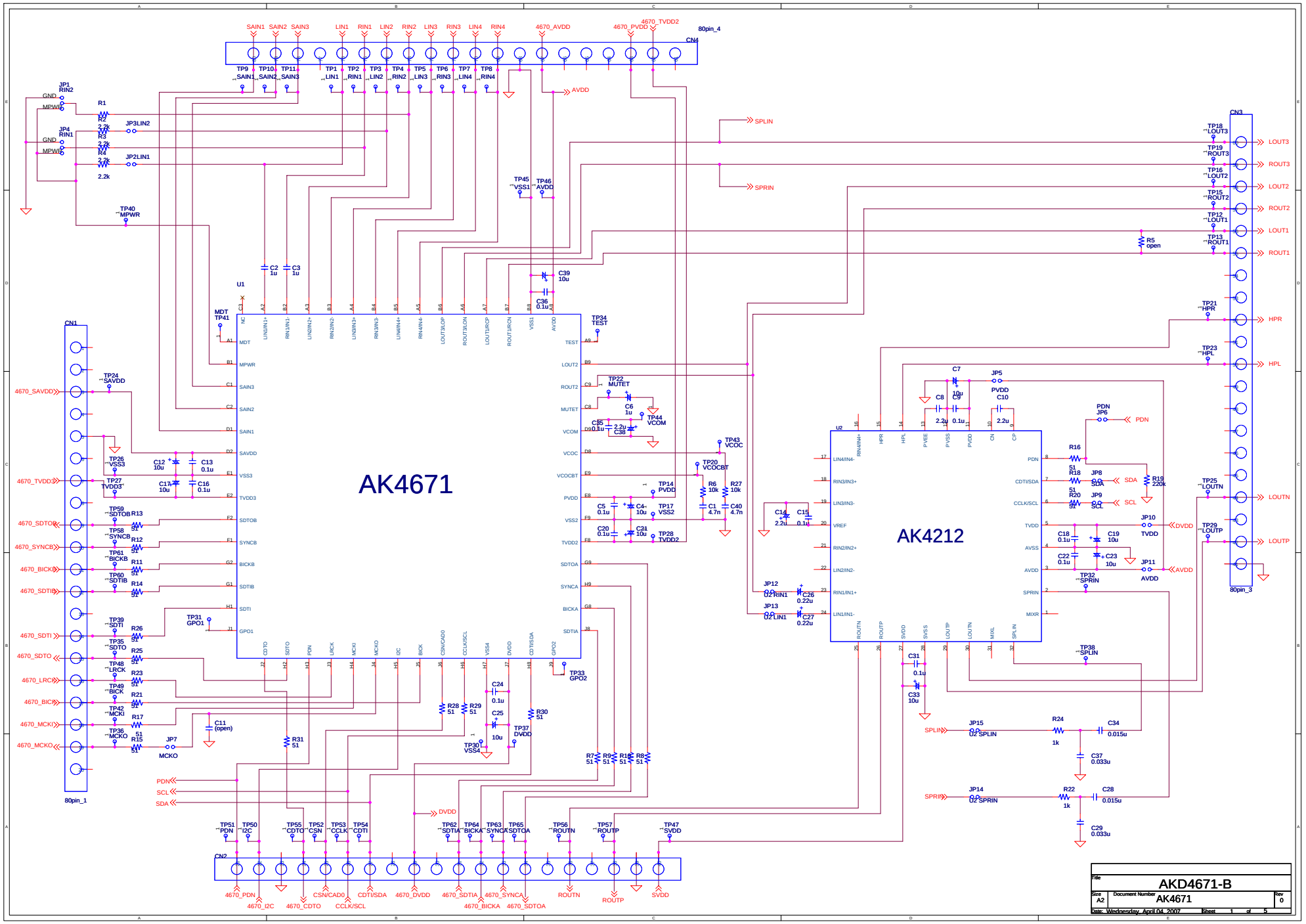
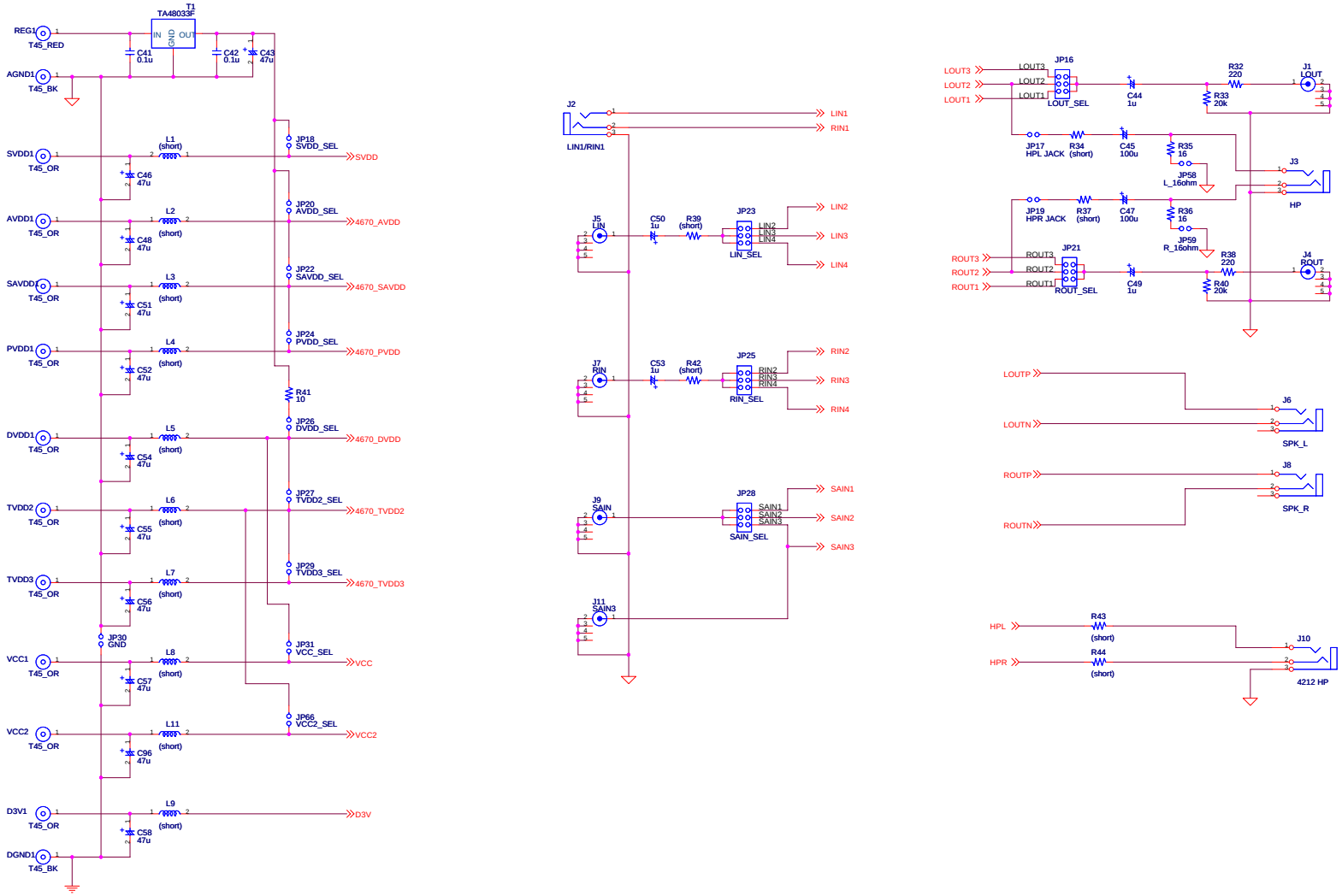

AK4671
AK4212
CN4
80pin_4
CN1
80pin_1
CN2
CN3
80pin_3
U1
U2
SAIN1 SAIN2 SAIN3 LIN1 RIN1 LIN2 RIN2 LIN3 RIN3 LIN4 RIN4
4670_AVDD
4670_PVDD
4670_TVDD2
AVDD
SPLIN
SPRIN
MPWR
LOUT3 ROUT3 LOUT2 ROUT2 LOUT1 ROUT1
HPR HPL LOUTN LOUTP
4670_SAVDD
4670_TVDD3
4670_SDTOB
4670_SYNCB
4670_BICKB
4670_SDTIB
4670_SDTI
4670_SDTO
4670_LRCK
4670_BICK
4670_MCKI
4670_MCKO
PDN
SCL
SDA
DVDD
4670_PDN
4670_I2C
4670_CDTO
CCLK/SCL
CDTI/SDA
4670_DVDD
4670_SDTIA
4670_BICKA
4670_SYNCA
4670_SDTOA
ROUTN
ROUTP
SVDD
AKD4671-B
AK4671
Wednesday, April 04, 2007



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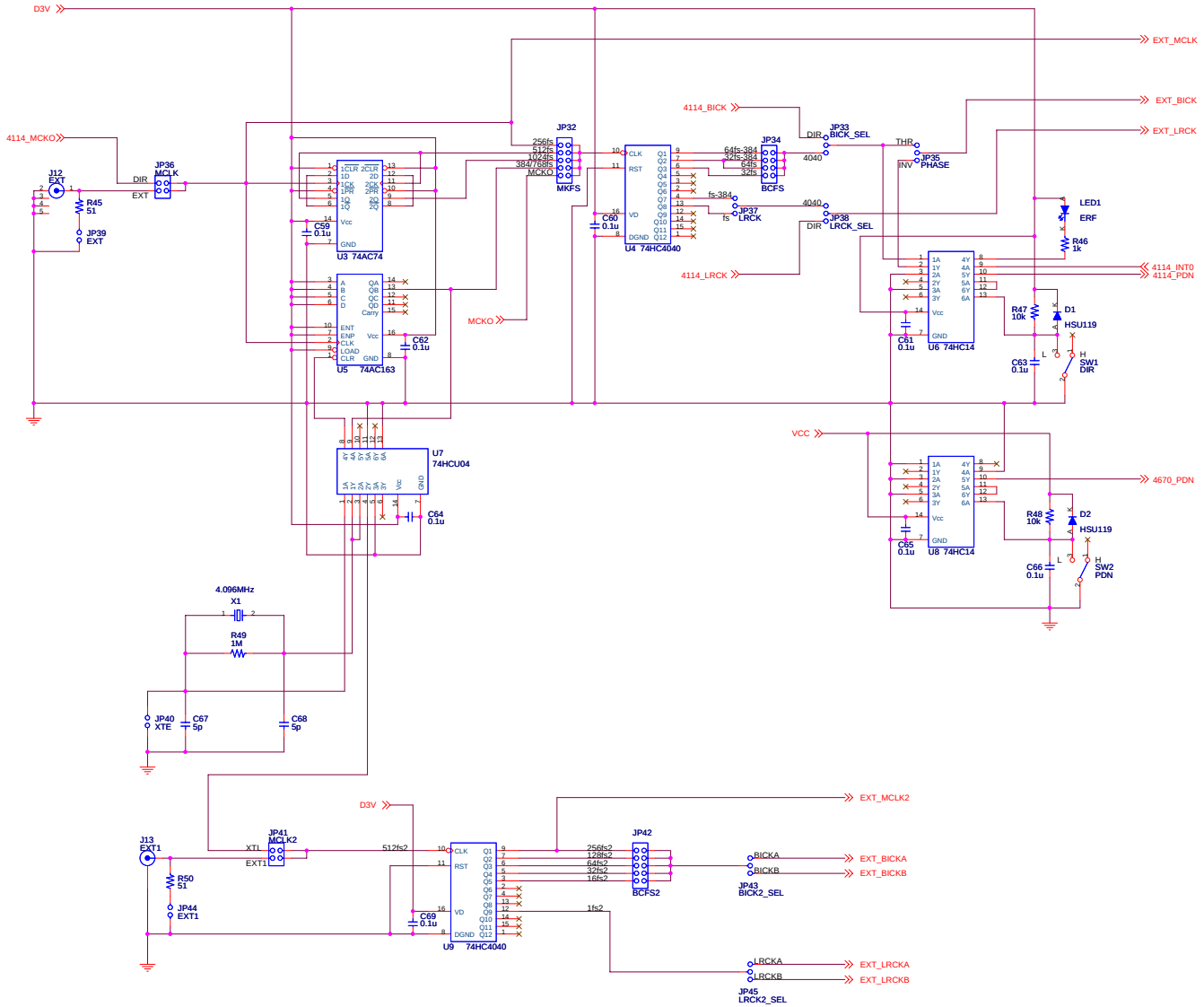
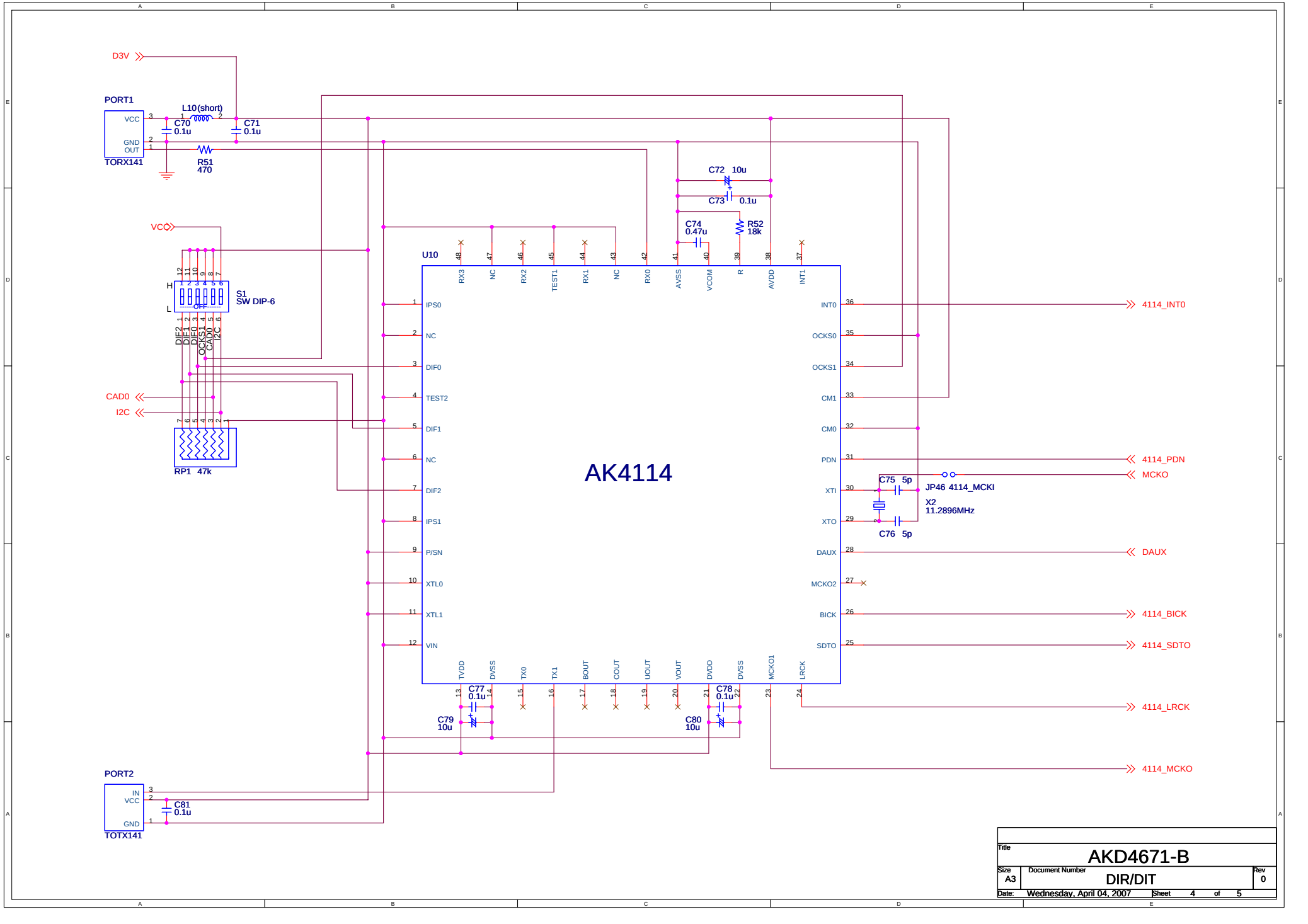
Size A2	Document Number Power Supply, I/O	Rev 0
Date: Wednesday, April 04, 2007	Sheet 2 of 5	



Title	AKD4671-B	
Size: A2	Document Number: CLOCK	Rev: 0
Date: Wednesday, April 04, 2007	Sheet 3 of 5	


D3V
PORT1
VCC
GND
OUT
TORX141
L10(short)
C70
0.1u
C71
0.1u
R51
470
C72 10u
C73 0.1u
C74
0.47u
R52
18k
VCC
S1
SW DIP-6
H
L
OFF
DIF2
DIF1
DIF0
OCKS1
OCKS0
CAD0
I2C
CAD0
I2C
RP1 47k
U10
AK4114
RX3
NC
RX2
TEST1
RX1
NC
RX0
AVSS
VCOM
R
AVDD
INT1
IPS0
NC
DIF0
TEST2
DIF1
NC
DIF2
IPS1
P/SN
XTL0
XTL1
VIN
INT0
OCKS0
OCKS1
CM1
CM0
PDN
XTI
XTO
DAUX
MCKO2
BICK
SDTO
TVDD
DVSS
TX0
TX1
BOUT
COUT
UOUT
VOUT
DVDD
DVSS
MCKO1
LRCK
4114_INT0
4114_PDN
MCKO
C75 5p
JP46 4114_MCKI
X2
11.2896MHz
C76 5p
DAUX
4114_BICK
4114_SDTO
C77
0.1u
C78
0.1u
C79
10u
C80
10u
4114_LRCK
4114_MCKO
PORT2
IN
VCC
GND
TOTX141
C81
0.1u
Title
AKD4671-B
Size
A3
Document Number
DIR/DIT
Rev
0
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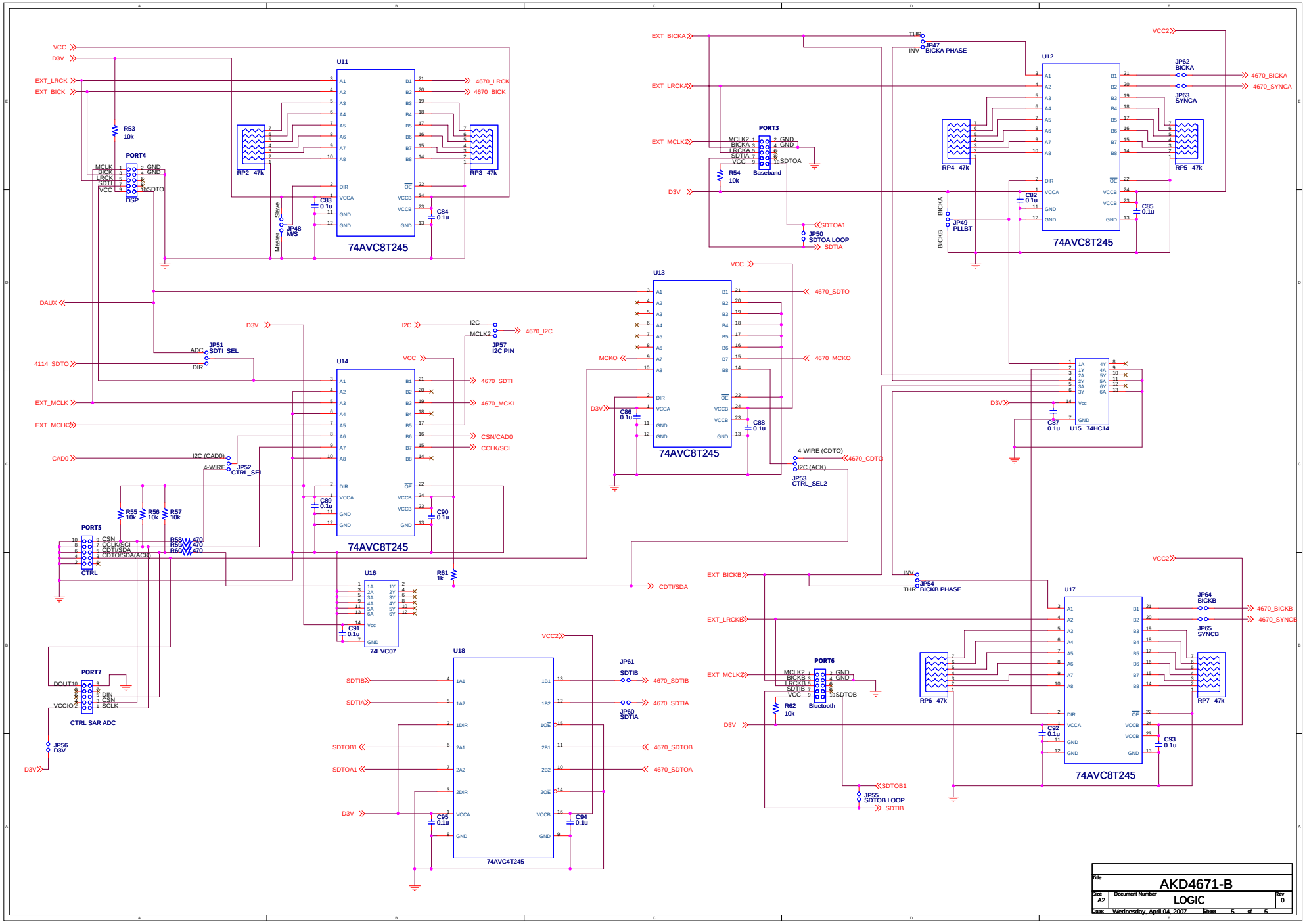
of
5


VCC
D3V
EXT_LRCK
EXT_BICK
R53
10k
PORT4
MCLK
BICK
LRCK
SDTI
VCC
GND
GND
10:SDTO
DSP
U11
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
DIR
OE
VCCA
VCCB
GND
74AVC8T245
4670_LRCK
4670_BICK
RP2 47k
RP3 47k
Slave
Master
JP48
M/S
C83
0.1u
C84
0.1u
EXT_BICKA
EXT_LRCKA
EXT_MCLKA
D3V
PORT3
MCLK2
BICKA
LRCKA
SDTIA
VCC
GND
GND
10:SDTOA
R54
10k
Baseband
SDTOA1
JP50
SDTOA LOOP
SDTIA
THR
JP47
INV
BICKA PHASE
U12
VCC2
JP62
BICKA
JP63
SYNCA
4670_BICKA
4670_SYNCA
RP4 47k
RP5 47k
C82
0.1u
C85
0.1u
BICKA
BICKB
JP49
PLLBT
DAUX
D3V
I2C
I2C
MCLK2
JP57
I2C PIN
4670_I2C
ADC
JP51
SDTI_SEL
DIR
4114_SDTO
U13
VCC
4670_SDTO
MCKO
4670_MCKO
C86
0.1u
C88
0.1u
U14
VCC
4670_SDTI
4670_MCKI
CSN/CAD0
CCLK/SCL
EXT_MCLK
EXT_MCLK
CAD0
I2C (CAD0)
4-WIRE
JP52
CTRL_SEL
4-WIRE (CDTO)
4670_CDTO
I2C (ACK)
JP53
CTRL_SEL2
R55
10k
R56
10k
R57
10k
C89
0.1u
C90
0.1u
PORT5
CSN
CCLK/SCL
CDTI/SDA
CDTO/SDA(ACK)
CTRL
R58
470
R59
470
R60
470
U16
74LVC07
R61
1k
CDTI/SDA
U15 74HC14
C87
0.1u
EXT_BICKB
EXT_LRCKB
EXT_MCLKB
D3V
PORT6
MCLK2
BICKB
LRCKB
SDTIB
VCC
GND
GND
10:SDTOB
Bluetooth
R62
10k
SDTOB1
JP55
SDTOB LOOP
SDTIB
INV
THR
JP54
BICKB PHASE
U17
VCC2
JP64
BICKB
JP65
SYNCB
4670_BICKB
4670_SYNCB
RP6 47k
RP7 47k
C92
0.1u
C93
0.1u
U18
VCC2
SDTIB
SDTIA
SDTOB1
SDTOA1
D3V
1A1
1A2
1DIR
2A1
2A2
2DIR
1B1
1B2
1OE
2B1
2B2
2OE
VCCA
VCCB
GND
74AVC4T245
JP61
SDTIB
JP60
SDTIA
4670_SDTIB
4670_SDTIA
4670_SDTOB
4670_SDTOA
C95
0.1u
C94
0.1u
PORT7
DOUT
DIN
CSN
SCLK
VCCIO
CTRL SAR ADC
JP56
D3V
D3V
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AKD4671-B
Size
A2
Document Number
LOGIC
Rev
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Date:
Wednesday, April 04, 2007
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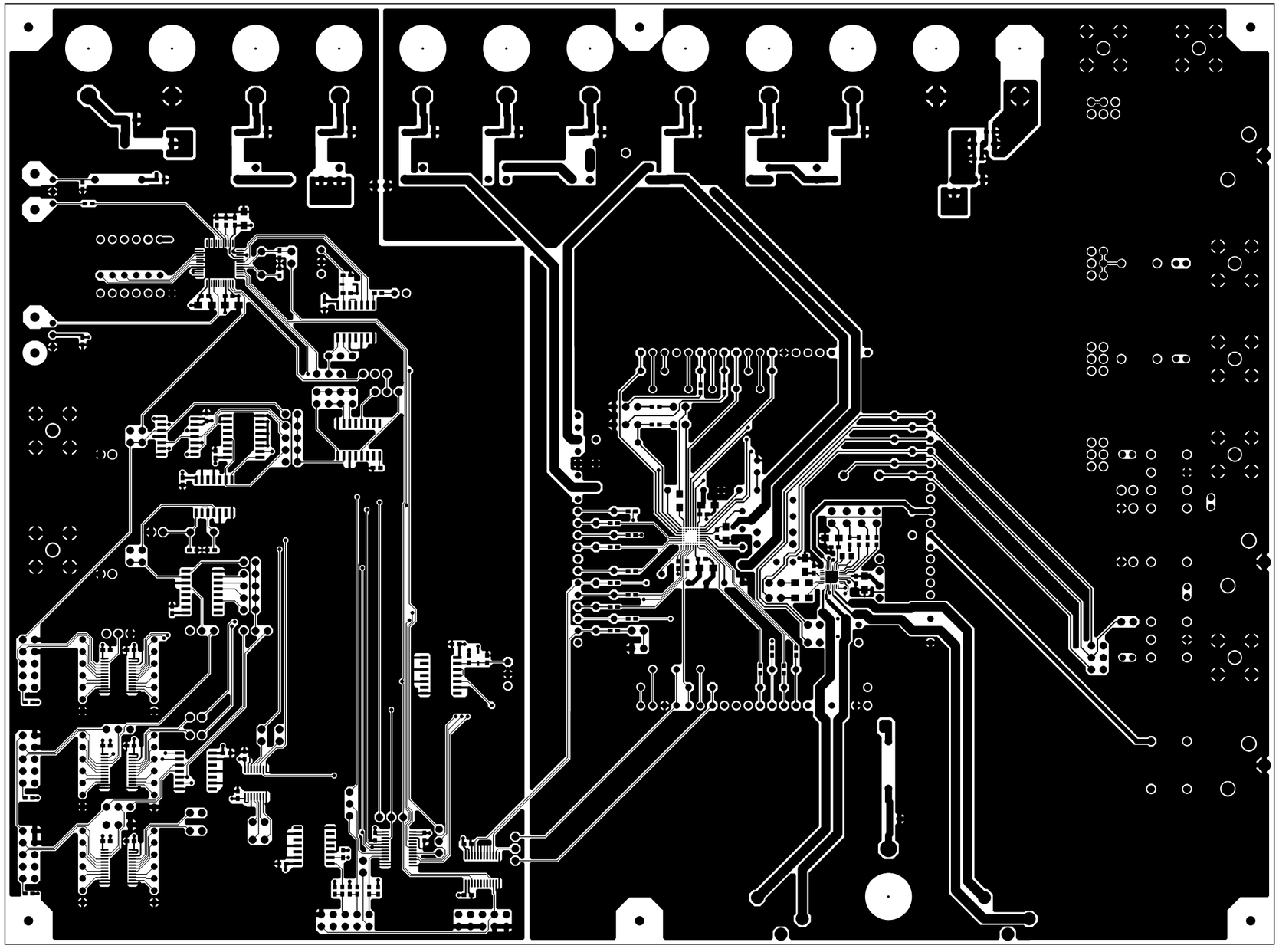

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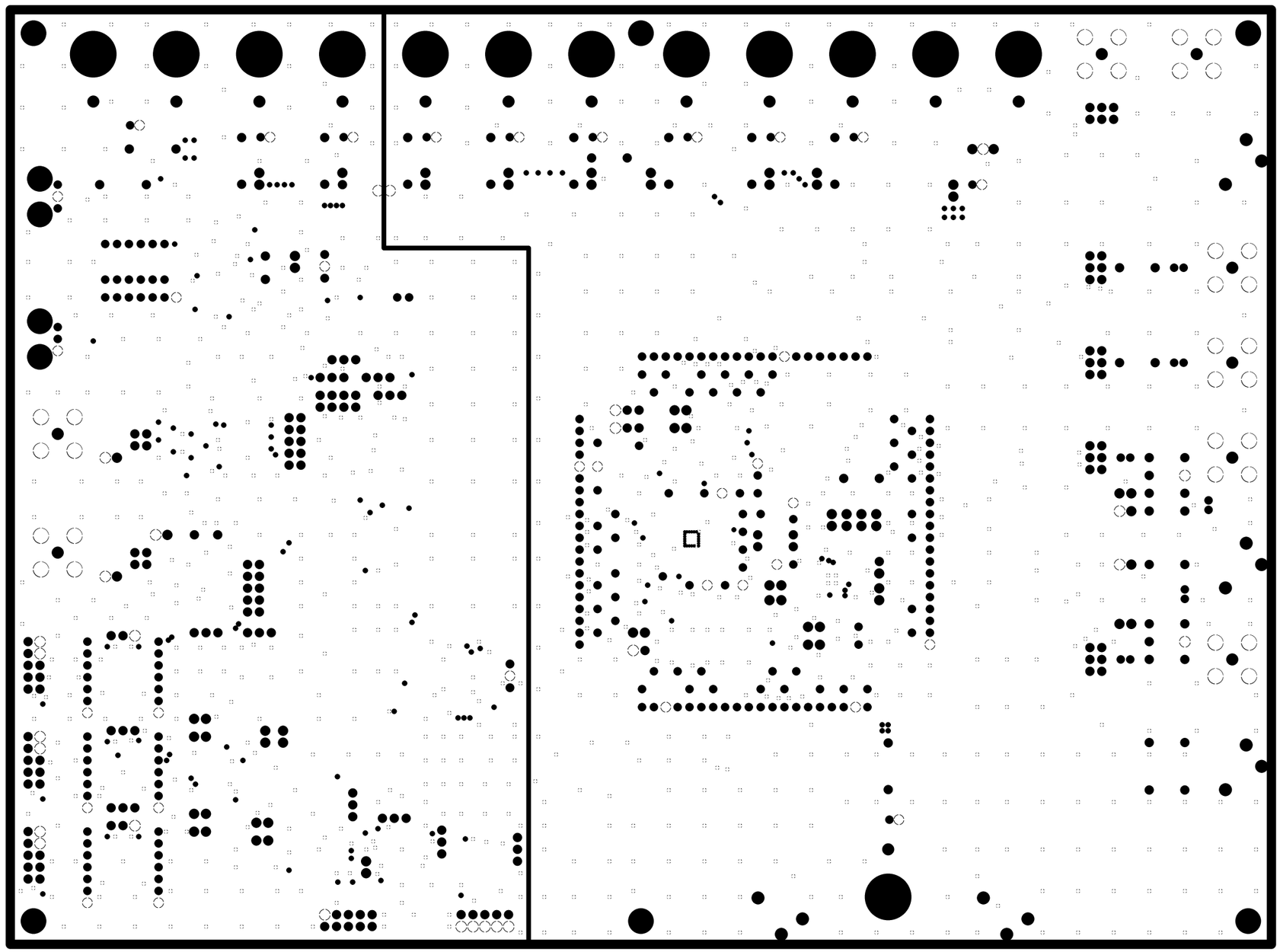

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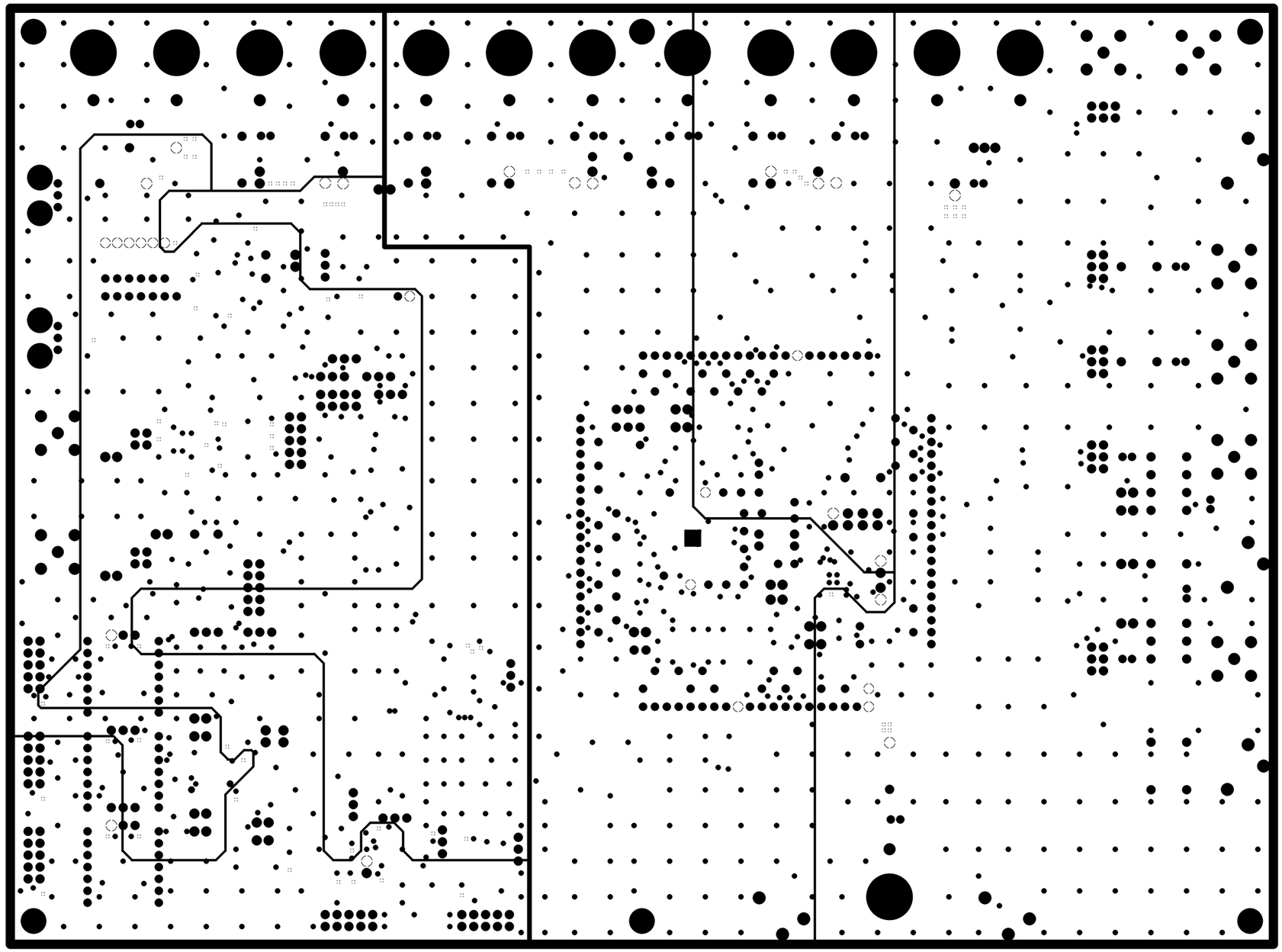
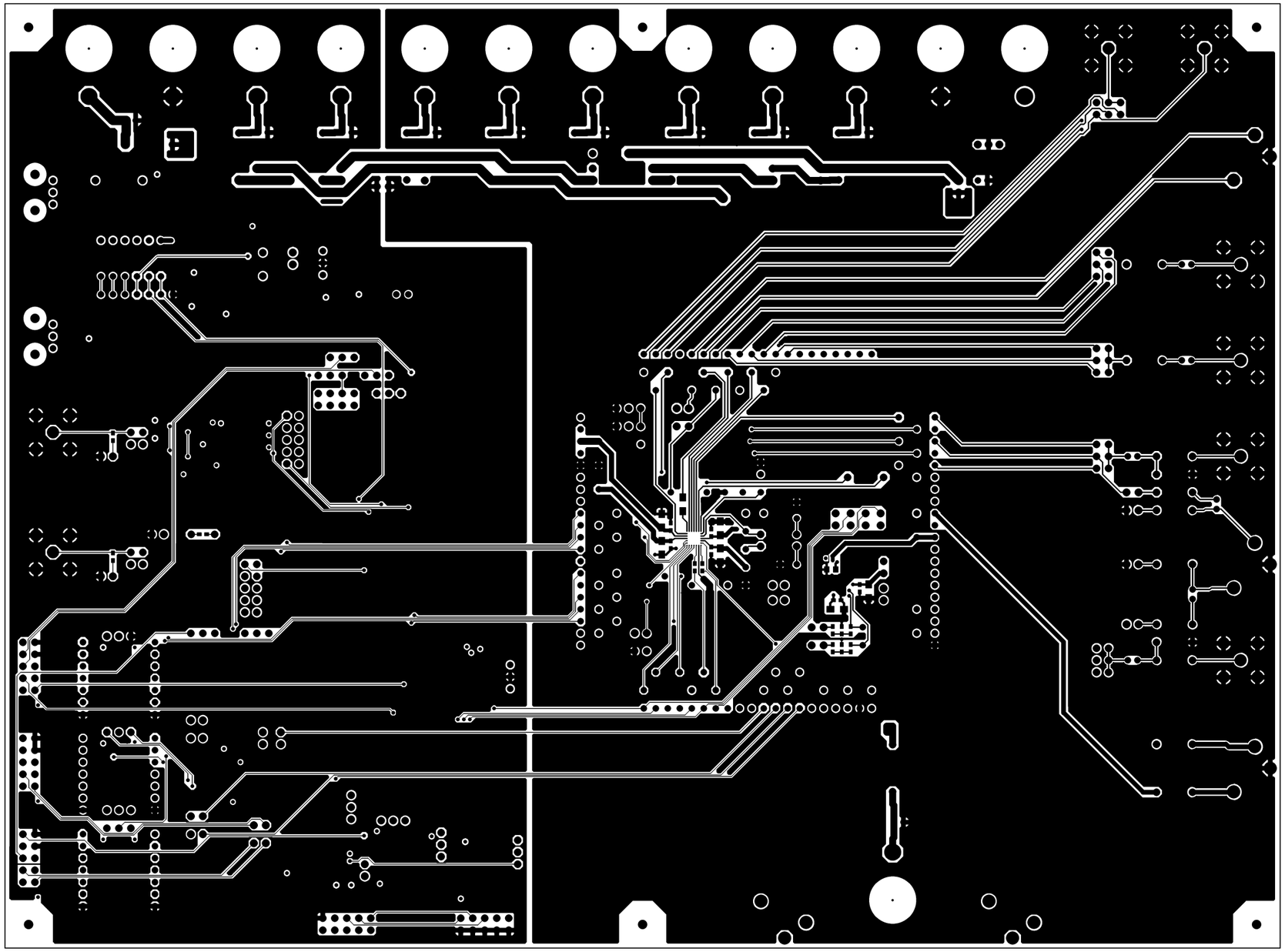


L3層(電源)



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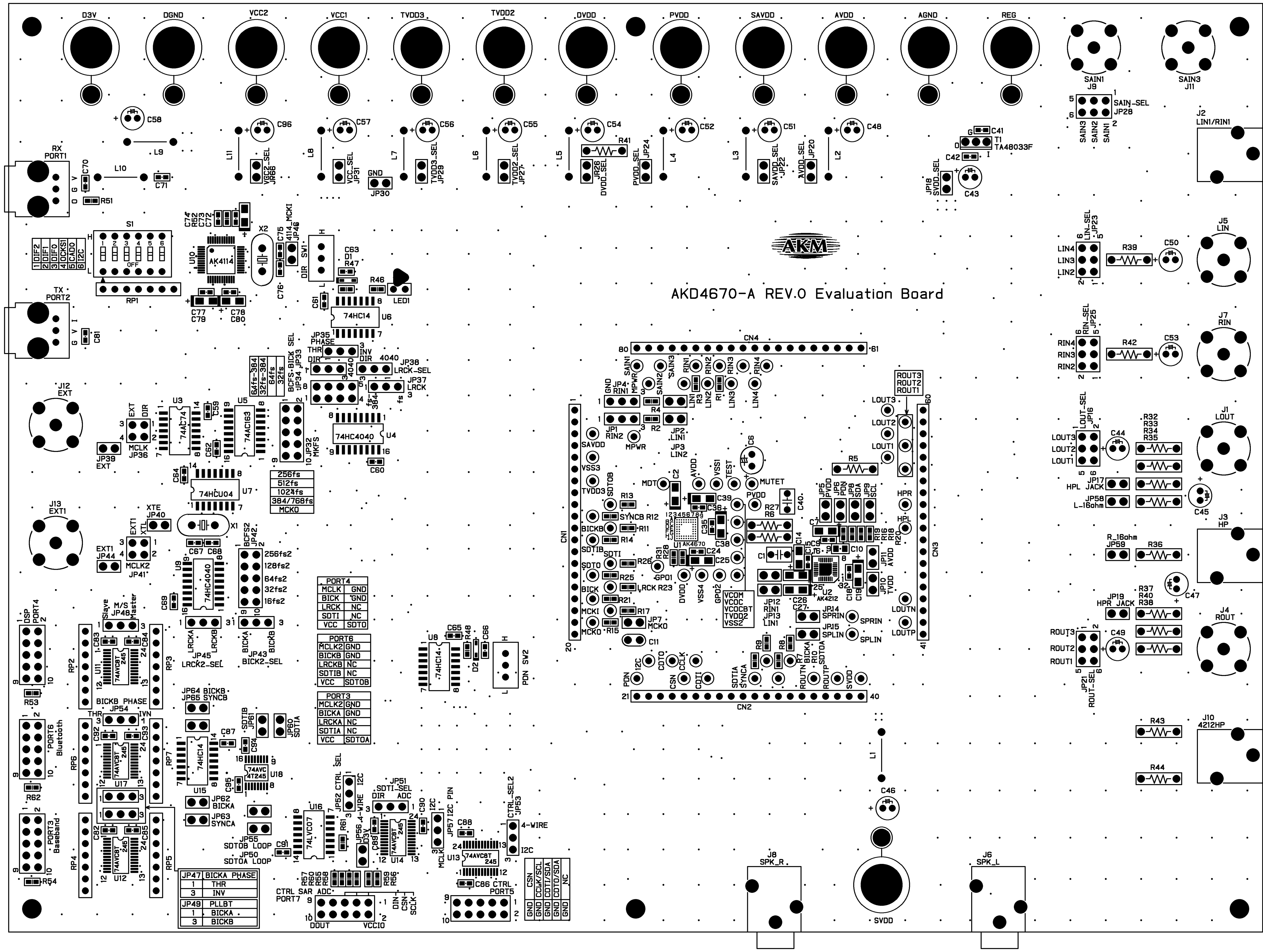
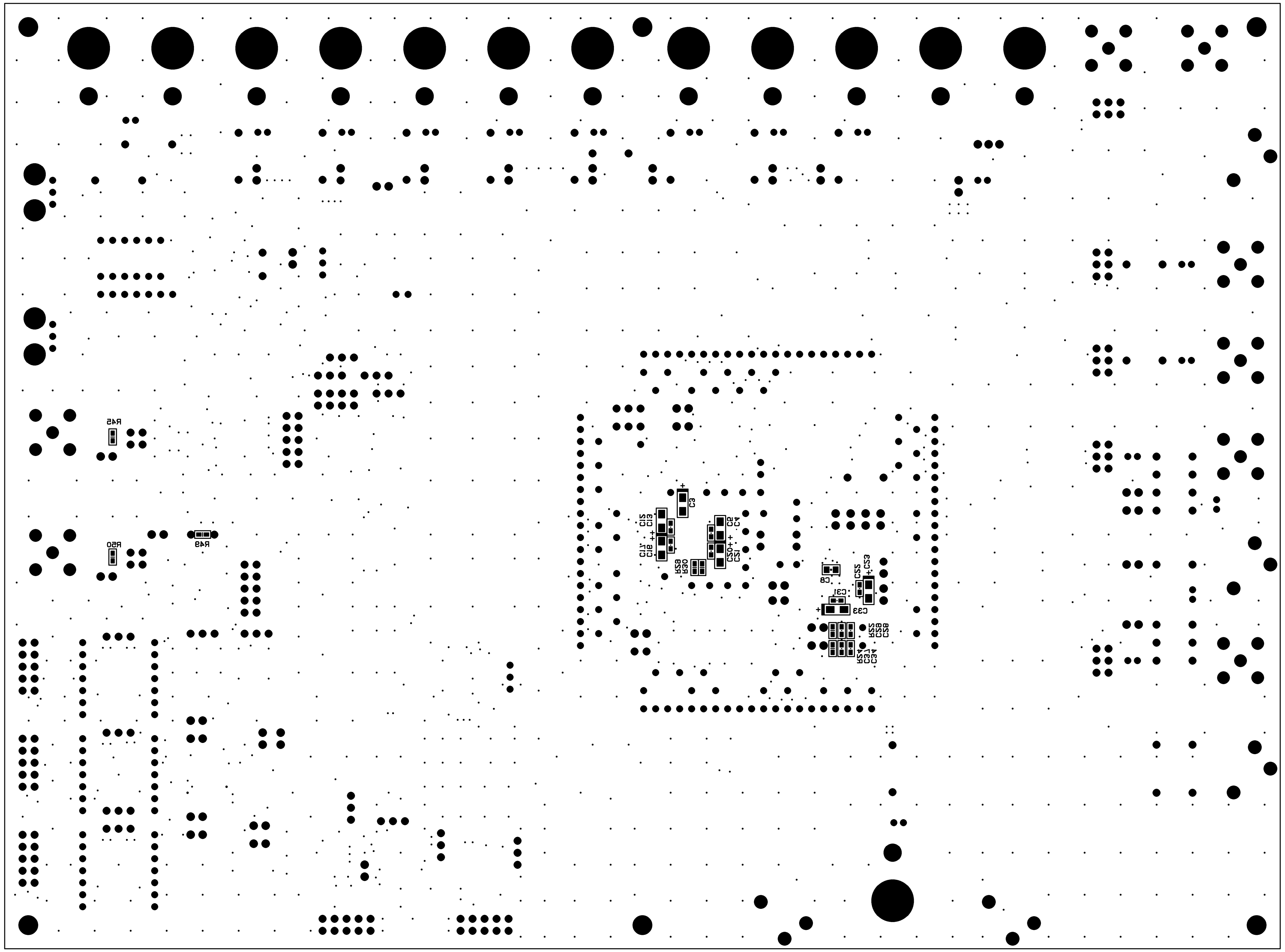

AKD4670-A REV.0 Evaluation Board
AKM
D3V
DGND
VCC2
VCC1
TVDD3
TVDD2
DVDD
PVDD
SAVDD
AVDD
AGND
REG
SAIN1
SAIN3
RX PORT1
TX PORT2
J12 EXT
J13 EXT1
J2 LIN1/RIN1
J5 LIN
J7 RIN
J1 LOUT
J3 HP
J4 ROUT
J10 4212HP
J8 SPK_R
J6 SPK_L
SVDD
CN1
CN2
CN3
CN4
DSP PORT4
Bluetooth PORT6
Baseband PORT3
PORT7
PORT5
PORT4
PORT6
PORT3
AK4114
74HC14
74HC4040
74HCU04
74AC74
74AC163
74LVC07
TA48033F
AK4670
AK4212

L1 層レジスト シルク


R45
R50
R49
C3
C15
C13
C17
C16
R29
R30
C2
C4
C20
C21
C8
C22
C23
C31
C33
R22
C29
C28
R24
C37
C34

L4層レジスト シルク