



## RAIL-TO-RAIL PRECISION OPERATIONAL AMPLIFIER

### GENERAL DESCRIPTION

The ALD1712 is a monolithic precision operational amplifier intended primarily for a wide range of analog applications in +5V single power supply and  $\pm 5V$  dual power supply systems as well as +6V to 12V battery operated systems. All device characteristics are specified for +5V single supply or  $\pm 2.5V$  dual supply systems. It is manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process and is available as a standard cell in ALD's ASIC "Function-Specific" library.

The device has an input stage that operates to +300mV above and -300mV below the supply voltages with no adverse effects and/or phase reversals.

The ALD1712 has been developed specifically with the 5V single supply or  $\pm 2.5V$  dual supply user in mind. Several important characteristics of the device make many applications easy to implement for these supply voltages. First, the operational amplifier can operate with rail-to-rail input and output voltages. This feature allows numerous analog serial stages to be implemented without losing operating voltage margin. Secondly, the device was designed to accommodate mixed applications where digital and analog circuits may work off the same 5V power supply. Thirdly, the output stage can drive up to 400pF capacitive, and 1K $\Omega$  resistive loads in non-inverting unity gain connection, and up to 4000pF at a gain of 5. These features, coupled with extremely low input currents, high voltage gain, useful bandwidth of 1.5MHz, slew rate of 2.1V/ $\mu$ s, low power dissipation, low offset voltage and temperature drift, make the ALD1712 a truly versatile, user friendly, operational amplifier.

On-chip offset voltage trimming allows the device to be used without nulling in most applications. The device offers typical offset drift of less than 5 $\mu$ V/ $^{\circ}$ C which eliminates many trim or temperature compensation circuits. For precision applications, the 1712 is designed to settle to 0.01% in 8 $\mu$ s. The unique characteristics at input and output are modeled in an available macromodel.

### FEATURES

- Linear mode operation with input voltages 300mV beyond supply rails
- Symmetrical complementary output drive
- Output voltages to within 2mV of power supply rails
- High load capacitance capability -- 4000pF typical
- No frequency compensation required -- unity gain stable
- Extremely low input bias currents -- 0.01pA typical
- Dual power supply  $\pm 2.5V$  to  $\pm 6.0V$
- Single power supply +5V to +12V
- High voltage gain -- typically 85V/mV @  $\pm 2.5V$  and 250V/mV @  $\pm 5.0V$
- Drive as low as 1K $\Omega$  load with 5mA drive current
- Output short circuit protected
- Unity gain bandwidth of 1.5MHz
- Slew rate of 2.1V/ $\mu$ s

### APPLICATIONS

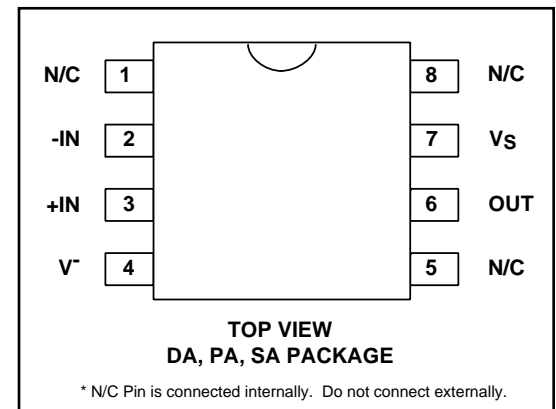
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter
- Coaxial cable driver

### ORDERING INFORMATION

Operating Temperature Range		
-55 $^{\circ}$ C to +125 $^{\circ}$ C	0 $^{\circ}$ C to +70 $^{\circ}$ C	0 $^{\circ}$ C to +70 $^{\circ}$ C
8-Pin CERDIP Package	8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package
ALD 1712A DA	ALD 1712 ASA	ALD 1712A PA
ALD 1712B DA	ALD 1712 BSA	ALD 1712B PA
ALD 1712 DA	ALD 1712 SA	ALD 1712 PA

\* Contact factory for industrial temperature range

### PIN CONFIGURATION



## ABSOLUTE MAXIMUM RATINGS

Supply voltage, V+	13.2V
Differential input voltage range	-0.3V to V+ +0.3V
Power dissipation	600 mW
Operating temperature range	PA,SA package 0°C to +70°C DA package -55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature, 10 seconds	+260°C

## OPERATING ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = 25°C V<sub>S</sub> = ±2.5V unless otherwise specified

Parameter	Symbol	1712A			1712B			1712			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V <sub>S</sub> V+	±2.0 4.0		±6.0 12.0	±2.0 4.0		±6.0 12.0	±2.0 4.0		±6.0 12.0	V	Single Supply
Input Offset Voltage	V <sub>OS</sub>		0.05	0.15 0.35		0.1	0.25 0.55		0.25	0.5 1.0	mV mV	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Offset Current	I <sub>OS</sub>		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Bias Current	I <sub>B</sub>		0.01	10 280		0.01	10 280		0.01	10 280	pA pA	T <sub>A</sub> = 25°C 0°C ≤ T <sub>A</sub> ≤ +70°C
Input Voltage Range	V <sub>IR</sub>	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	-0.3 -2.8		5.3 +2.8	V V	V+ = +5; notes 2,5 V <sub>S</sub> = ±2.5V
Input Resistance	R <sub>IN</sub>		10 <sup>13</sup>			10 <sup>13</sup>			10 <sup>13</sup>		Ω	
Input Offset Voltage Drift	TCV <sub>OS</sub>		5			5			5		μV/°C	R <sub>S</sub> ≤ 100KΩ
Power Supply Rejection Ratio	PSRR	65 65	85 85		65 65	85 85		63 63	85 85		dB dB	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Common Mode Rejection Ratio	CMRR	65 65	83 83		65 65	83 83		63 63	83 83		dB dB	R <sub>S</sub> ≤ 100KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Large Signal Voltage Gain	A <sub>v</sub>	50 20	85 400		50 20	85 400		50 20	85 400		V/mV V/mV V/mV	R <sub>L</sub> = 10KΩ R <sub>L</sub> ≥ 1MΩ R <sub>L</sub> = 10KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Output Voltage Range	V <sub>O</sub> low V <sub>O</sub> high V <sub>O</sub> low V <sub>O</sub> high	4.99 2.35	0.002 4.998 -2.44 2.44	0.01 -2.35 2.44	4.99 2.35	0.002 4.998 -2.44 2.44	0.01 -2.35 2.35	4.99 2.35	0.002 4.998 -2.44 2.44	0.01 -2.35 2.44	V V V	R <sub>L</sub> = 1MΩ V+ = +5V 0°C ≤ T <sub>A</sub> ≤ +70°C R <sub>L</sub> = 10KΩ 0°C ≤ T <sub>A</sub> ≤ +70°C
Output Short Circuit Current	I <sub>SC</sub>		8			8			8		mA	
Supply Current	I <sub>S</sub>		0.8	1.5		0.8	1.5		0.8	1.5	mA	V <sub>IN</sub> = 0V No Load
Power Dissipation	P <sub>D</sub>		4.0	7.5		4.0	7.5		4.0	7.5	mW	V <sub>S</sub> = ±2.5V
Input Capacitance	C <sub>IN</sub>		1			1			1		pF	
Bandwidth	B <sub>W</sub>	1.0	1.5		1.0	1.5		1.0	1.5		MHz	
Slew Rate	S <sub>R</sub>	1.4	2.1		1.4	2.1		1.4	2.1		V/μs	A <sub>v</sub> = +1 R <sub>L</sub> = 10KΩ
Rise time	t <sub>r</sub>		0.2			0.2			0.2		μs	R <sub>L</sub> = 10KΩ
Overshoot Factor			10			10			10		%	R <sub>L</sub> = 10KΩ C <sub>L</sub> = 100pF

**OPERATING ELECTRICAL CHARACTERISTICS (cont'd)**
 **$T_A = 25^\circ\text{C}$   $V_S = \pm 2.5\text{V}$  unless otherwise specified**

Parameter	Symbol	1712A			1712B			1712			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Maximum Load Capacitance	$C_L$		400 4000			400 4000			400 4000		pF pF	Gain = 1 Gain = 5
Input Noise Voltage	$e_n$		26			26			26		$\text{nV}/\sqrt{\text{Hz}}$	$f = 1\text{kHz}$
Input Current Noise	$i_n$		0.6			0.6			0.6		$\text{fA}/\sqrt{\text{Hz}}$	$f = 10\text{Hz}$
Settling Time	$t_s$		8.0 3.0			8.0 3.0			8.0 3.0		$\mu\text{s}$ $\mu\text{s}$	0.01% 0.1% $A_V = -1$ $R_L = 5\text{K}\Omega$ $C_L = 50\text{pF}$

 **$T_A = 25^\circ\text{C}$   $V_S = \pm 5.0\text{V}$  unless otherwise specified**

Parameter	Symbol	1712A			1712B			1712			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		83			83			83		dB	$R_S \leq 100\text{K}\Omega$
Common Mode Rejection Ratio	CMRR		83			83			83		dB	$R_S \leq 100\text{K}\Omega$
Large Signal Voltage Gain	$A_V$		250			250			250		V/mV	$R_L = 10\text{K}\Omega$
Output Voltage Range	$V_{O\text{ low}}$ $V_{O\text{ high}}$	4.80	-4.90 4.93	-4.80	4.80	-4.90 4.93	-4.80	4.80	-4.90 4.93	-4.80	V	$R_L = 10\text{K}\Omega$
Bandwidth	$B_W$		1.7			1.7			1.7		MHz	
Slew Rate	$S_R$		2.8			2.8			2.8		$\text{V}/\mu\text{s}$	$A_V = +1$ $C_L = 50\text{pF}$

 **$V_S = +5\text{V}$   $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$  unless otherwise specified**

Parameter	Symbol	1712A DA			1712B DA			1712 DA			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	$V_{OS}$		0.5	1.0		0.8	1.5		1.2	2.5	mV	$R_S \leq 100\text{K}\Omega$
Input Offset Current	$I_{OS}$			4.0			4.0			4.0	nA	
Input Bias Current	$I_B$			4.0			4.0			4.0	nA	
Power Supply Rejection Ratio	PSRR	60	83		60	83		60	83		dB	$R_S \leq 100\text{K}\Omega$
Common Mode Rejection Ratio	CMRR	60	83		60	83		60	83		dB	$R_S \leq 100\text{K}\Omega$
Large Signal Voltage Gain	$A_V$	10	25		10	25		10	25		V/mV	$R_L = 10\text{K}\Omega$
Output Voltage Range	$V_{O\text{ low}}$ $V_{O\text{ high}}$	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	4.8	0.1 4.9	0.2	V V	$R_L \leq 10\text{K}\Omega$ $R_L \leq 10\text{K}\Omega$

## Design & Operating Notes:

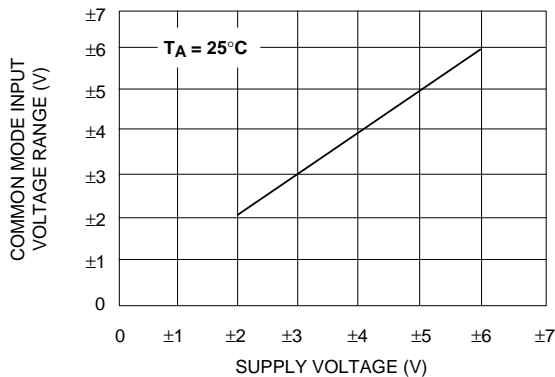
1. The ALD1712 CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. In a conventional CMOS operational amplifier design, compensation is achieved with a pole splitting capacitor together with a nulling resistor. This method is, however, very bias dependent and thus cannot accommodate the large range of supply voltage operation as is required from a stand alone CMOS operational amplifier. The ALD1712 is internally compensated for unity gain stability using a novel scheme that does not use a nulling resistor. This scheme produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency. A unity gain buffer using the ALD1712 will typically drive 400pF of external load capacitance without stability problems. In the inverting unity gain configuration, it can drive up to 800pF of load capacitance. Compared to other CMOS operational amplifiers, the ALD1712 has shown itself to be more resistant to parasitic oscillations.
2. The ALD1712 has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. This means that with the ranges of common mode input voltage close to the power supplies, one of the two differential stages is switched off internally. To maintain compatibility with other operational amplifiers, this switching point has been selected to be about 1.5V above the negative supply voltage. Since offset voltage trimming on the 1712 is made when the input voltage is symmetrical to the supply voltages, this internal switching does not affect a large variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions below this switching point. The user should however, be aware that this

switching does take place if the operational amplifier is connected as a unity gain buffer and should make provision in his design to allow for input offset voltage variations.

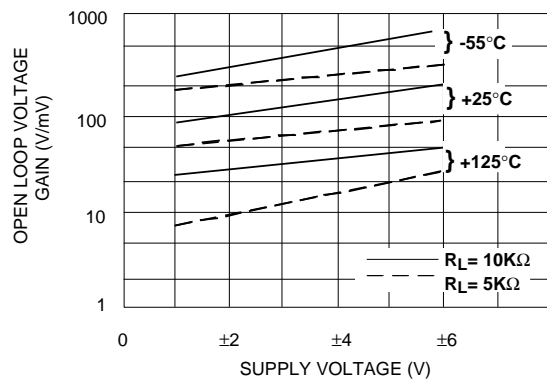
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 1pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than  $10^{12}\Omega$  would not be a problem as the source impedance would limit the node impedance. However, for applications where source impedance is very high, it may be necessary to limit noise and hum pickup through proper shielding.
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. The ALD1712 operational amplifier has been designed to provide full static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. In using the operational amplifier, the user is advised to power up the circuit before, or simultaneously with, any input voltages applied and to limit input voltages to not exceed 0.3V of the power supply voltage levels.

## TYPICAL PERFORMANCE CHARACTERISTICS

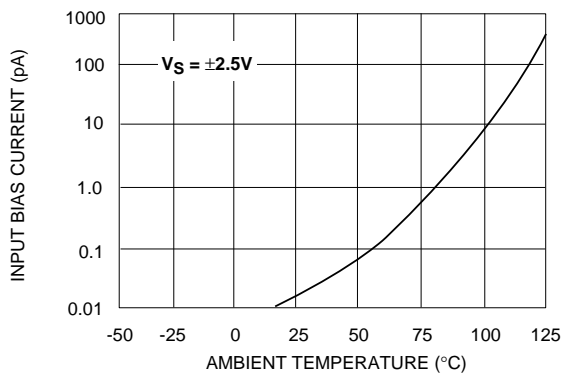
**COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



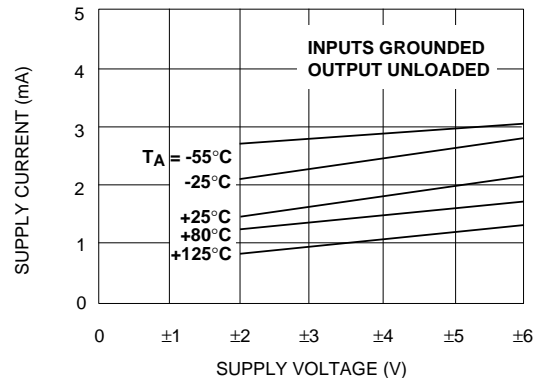
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE**



**INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE**

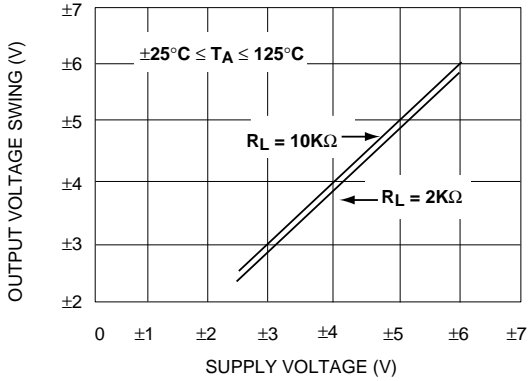


**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**

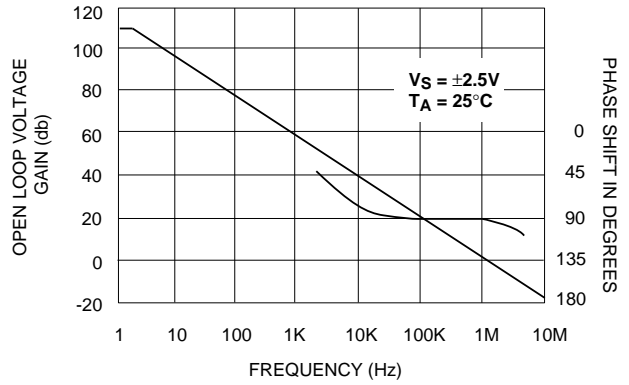


# TYPICAL PERFORMANCE CHARACTERISTICS

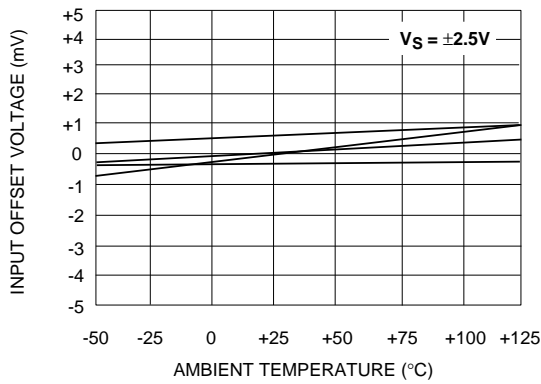
**OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE**



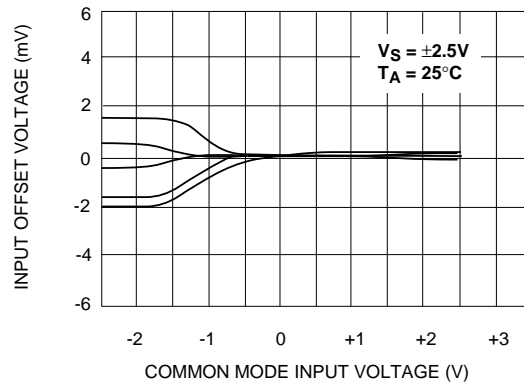
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY**



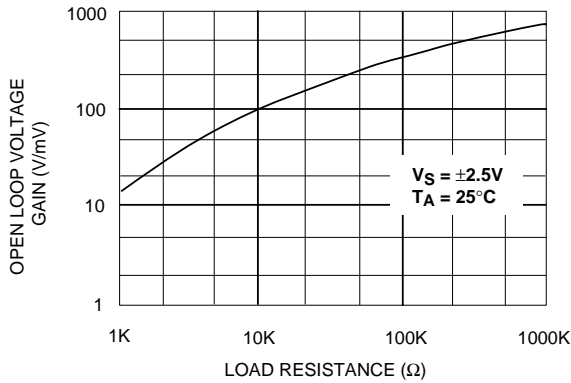
**INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE REPRESENTATIVE UNITS**



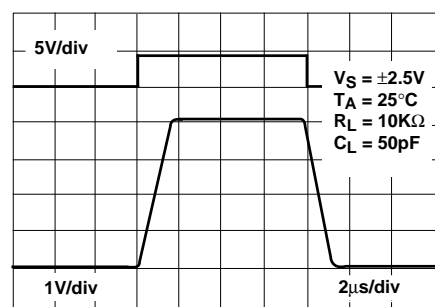
**INPUT OFFSET VOLTAGE AS A FUNCTION OF COMMON MODE INPUT VOLTAGE**



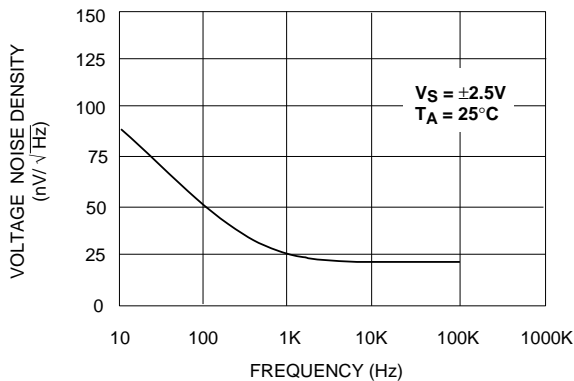
**OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE**



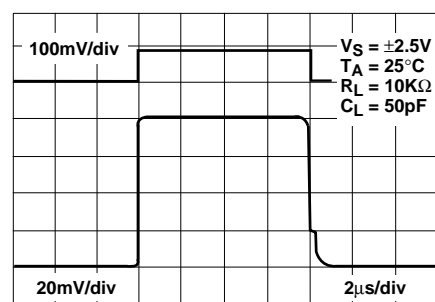
**LARGE - SIGNAL TRANSIENT RESPONSE**



**VOLTAGE NOISE DENSITY AS A FUNCTION OF FREQUENCY**

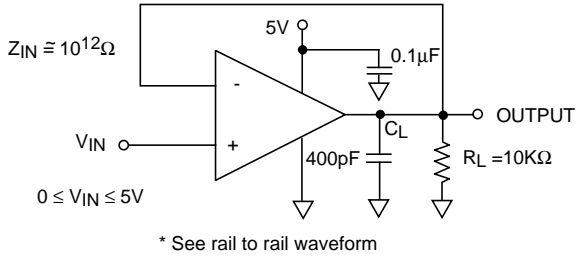


**SMALL - SIGNAL TRANSIENT RESPONSE**

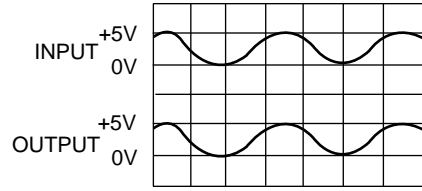


# TYPICAL APPLICATIONS

## RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER

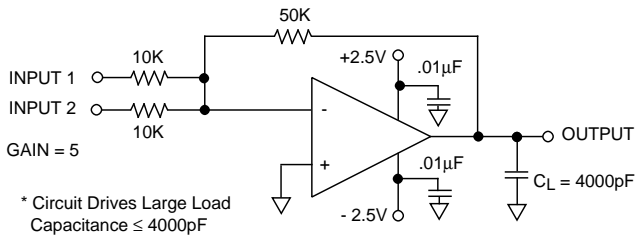


## RAIL-TO-RAIL WAVEFORM

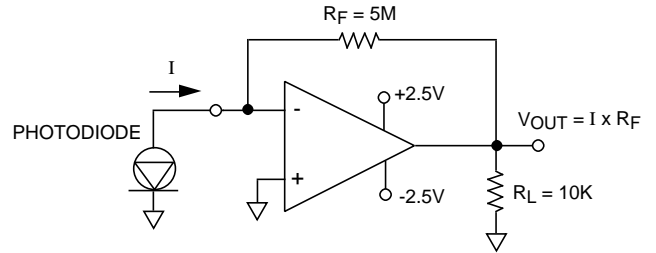


**Performance waveforms.**  
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-Rail voltage follower.

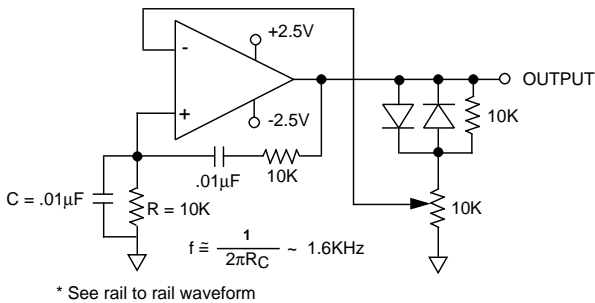
## LOW OFFSET SUMMING AMPLIFIER



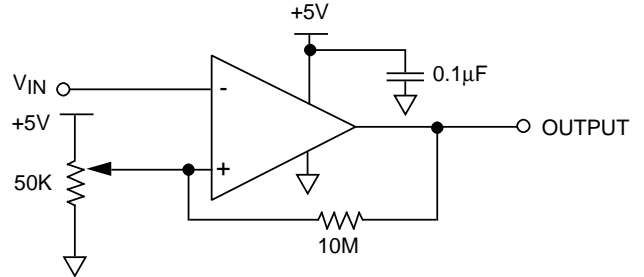
## PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER



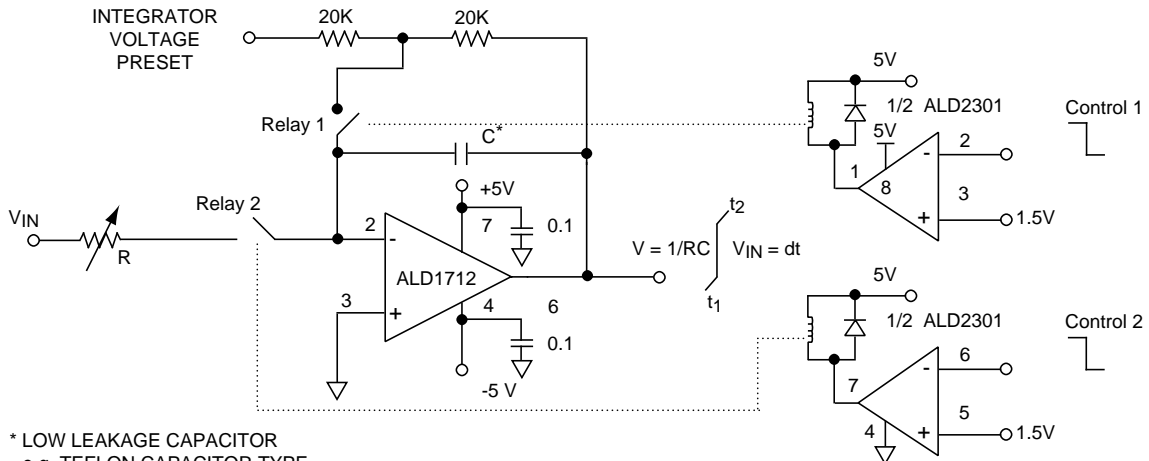
## WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR



## RAIL-TO-RAIL VOLTAGE COMPARATOR



## ULTRA LONG TIME CONSTANT INTEGRATOR



- \* LOW LEAKAGE CAPACITOR  
e.g. TEFLON CAPACITOR TYPE  
K11B104KSW Component  
Research Inc.
- All capacitance values are in μF unless otherwise specified.
- RELAYS 1 & 2 are of type 4705, Gordos Corporation.