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GTLP Power Configuration

Introduction

In order to drive high performance backplanes, GTLP devices require power. This power comes from three discrete levels: device power V_{CC}, termination voltage V_T, and threshold voltage V_{REF}. Each of these power sources have different needs both in terms of energy used and more importantly, noise characteristics.

This application note provides an analysis of a GTLP backplane from a power perspective. This application note will provide insight into the appropriate power requirements and configurations for a GTLP backplane at each of the discrete levels.

Device Bias V_{CC}

Datasheet specifications for GTLP devices list V_{CC} as ranging from 3.15V to 3.45V, a variance of almost ±5%. In order to meet all datasheet performance specifications, this voltage range must be conformed to. Maintaining a level in this range is relatively simple to do and is often generated by a master supply, possibly a switching or linear regulator in the backplane cage. The common problem is the distance between the cleanly filtered master supply output and the GTLP device that it is powering. It is over this distance that a problem is most often introduced.

When troubleshooting a device, it is imperative that the V_{CC} oscilloscope probe and ground be placed as close to the device as possible. It is here that disturbances are seen. Putting the device through the various configurations that the device might encounter during operation is also important. Clocking data in the AB direction while under Multiple Outputs Switching (MOS) is perhaps a worse case condition, but this can vary between applications. It can also be beneficial to monitor the ground plane for noise. There is often more than one V_{CC} pin on GTLP devices to better distribute power inside the device. Each of these pins will be wired to the V_{CC} plane of the PCB, but each pin should also have its own bypass and or decoupling capacitors as close as possible to the device. Depending on the size and frequency of the disturbance, more than one size and type of capacitor may be required.

How much noise is acceptable? Of the three voltage levels that GTLP devices require, V_{CC} has the greatest amount of noise tolerance. However, a V_{CC} spike of relative magnitude can be seen on the edge rate integrity of the device outputs. It is at this point that noise reduction measures should be taken such as including a local voltage regulator.

Termination Voltage V_T

Due to the open drain technology used in GTLP output buffers, a pull-up voltage level known as V_T, nominally 1.5V, is required. When a GTLP device receives a HIGH on the TTL input, it simply turns the output buffer OFF allowing the voltage level of the trace, labeled as V_{OH}, to be equal to the termination voltage.

Since the level of V_T directly affects the V_{OH} level there are advantages to adjusting V_T. Observations to be made during V_T adjustment include:

1. Noise Margin Associated with V_{REF}

   When V_{REF} adjustment is not available similar results can be accomplished by adjusting V_T.

2. Power Consumption

   As V_T is increased, the current through the device in a LOW state, I_{OL}, will increase. This may be a concern if minimizing power is a priority. The obvious trade-off to lowering V_T, thus lowering power consumption, is potential noise margin violations.

It is not until a LOW bit is received that the connection is made between the termination voltage and ground. The effective LOW on the bus, labeled as V_{OL}, is then the factor of a voltage division between the termination resistance R_T, and the On Resistance of the GTLP device R_{DSON}. Figure 1 illustrates this.

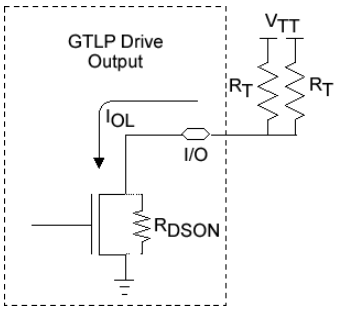

FIGURE 1. GTLP Output Buffer Showing Device R_{DSON}

Devices with higher drive, 100mA versus 50mA, have a lower R_{DSON}, V_{OL} calculation can vary between devices. The V_{OL} calculation can also vary considerably with temperature. Each GTLP device has its own V_{OL} vs. I_{OL} plot across temperature that can be used to calculate R_{DSON}. It is important to note that two devices capable of driving 100mA do not necessarily have the same R_{DSON} due to slight design differences. Always consult the datasheet or extended characterization for specific values.

A common question regarding open drain technologies is "what is required of the voltage source V_T and what are possible configurations for it?" It is evident that large amounts of current can be demanded from V_T based on the number of bits switching on the backplane and the value of R_T. But keep in mind that since the level of V_T sets V_{OH}, any drops in the voltage level of V_T will result in a degradation of the upper noise margin, the distance between V_{OH} and V_{REF}.

Termination Voltage V_T (Continued)

Current spikes are also experienced by the termination voltage supply. The two major factors that affect the value of this spike are inductance (L) in the transmission line and the rate at which the current is changing with respect to time ($\Delta I/\Delta t$). A Time Domain Reflectometry (TDR) device can be used to measure the amount of inductance associated with a given trace. The TDR device can also show the location of the inductance. Figure 2 shows the current measured at the output of one of two V_T regulators (one regulator is at each end of the backplane) while 3 bits are toggling at a slow rate in a GTLP16T1655. Because of the type of probe that is used, the DC current level that the signal settles to is not correct. These small spikes should be considered when calculating power ratings for supply components.

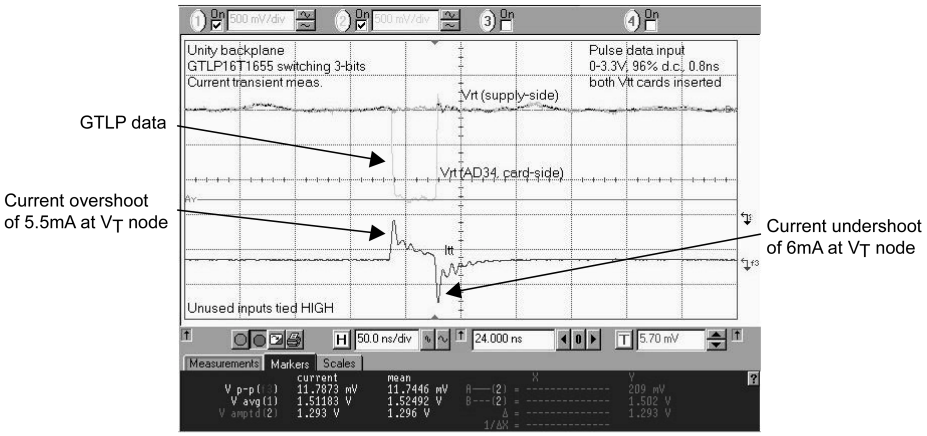

FIGURE 2. Current Spikes on V_T when 3 Bits are Simultaneously LOW

V_T Power Consumption

As previously stated, each bit switching in a GTLP device contributes to the power required from the V_T source. Figure 3 shows the linear increase in current as a series of bits are pulled LOW.

Conditions:

- Unloaded Backplane
- $R_T = 50\Omega$
- $V_T = 1.5V$
- Data Rate = 1MHz
- Each additional bit has same pattern
- Device is GTLP16T1655

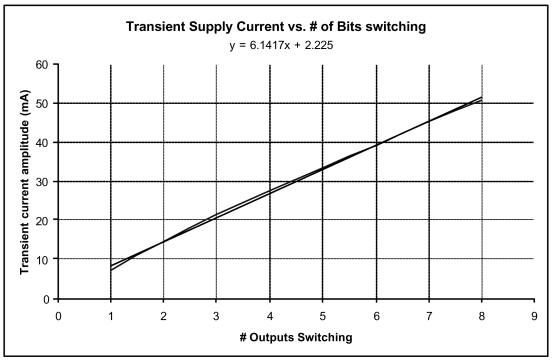

FIGURE 3. Outputs Switching versus Termination Supply Current

Linear Regulator V_T

One approach to generating a fixed termination level is to use a voltage regulator such as the Fairchild Semiconductor RC1585. This device is a 5A adjustable/fixed low dropout linear regulator designed specifically for GTLP use. With an input voltage of 5V or less, the RC1585 offers a regulated output range of 1.5V to 3.6V. Regulators are known for their ability to source relatively high amounts of current given their size. The RC1585 circuit, when properly designed into an application, can handle microsecond surge currents of 50A to 100A. These regulators also have the ability to sink fair amounts of heat based on their physical size and structure. One disadvantage of this robust device is power efficiency. Depending on the make and model of a linear regulator and the application at hand, it is possible to se a relatively low efficiency. With such a range for input and output power ratings, the benefits of linear regulators are often good trade-offs for efficiency. The solid regulator output coupled with a storage cap for “tough to manage” loads is an effective solution.

Regardless of the regulator chosen, this method still requires a capable master voltage supply for input. Assuming that a single regulator was used as a V_T source and provided the desired output at 60% efficiency. If one 100mA drive device were in operation and all 16 bits were held LOW at maximum current (i.e. R_T and V_T is set such that 100mA is traveling through each output buffer), the total power required from V_T is 1.6A. At 1.5V, the required output power of the linear regulator is 2.4W. Operating at 60% efficiency, this equates to 4W required from the master voltage supply.

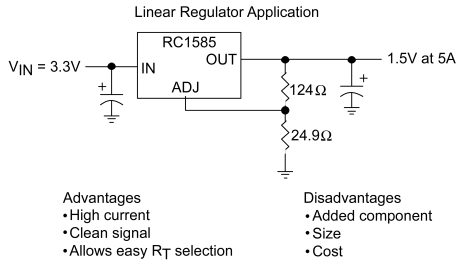

FIGURE 4. GTLP Termination Circuit Using a Linear Regular

Thevenin Equivalent V_T

As PCB real estate decreases, there are instances where it is not feasible to use a voltage regulator for V_T. Another option is to use voltage divider circuits off the V_{CC} supply. If done correctly, this can be a low cost solution to any design. Since the circuit is tied directly to the master V_{CC} source, all noise and transients will be evident on V_T. Precautions such as appropriate decoupling and resistor power ratings must be made close to each 1.5V node.

The major concern with this method is determining exactly how much resistance (R_T) is seen by each trace and what is the associated pull-up voltage level after properly considering all voltage drops. With GTLP backplane designs, a termination resistor variation of even 5Ω can be easily spotted in the signal's shape.

A sample divider from 3.3V down to 1.5V is not the complete solution. All resistances must be considered simultaneously. One resistance that cannot be changed is internal to the device – R_{DSON}. The drive of the device dictates this value, ranging from 3Ω to 6Ω for 100mA to 50mA drive, respectively. Since R_1 in parallel with R_2 is the Thevenin equivalent termination resistor, selecting resistors such that the parallel combination matches the effective impedance of the backplane and produces the correct voltage levels can be difficult. Figure 5 is a general representation of the complete circuit when a low bit is on the transmission line and R_{DSON} is seen.

When a high bit is on the transmission line, the V_T node only has the high impedance input of the receiver to contend with. At this time, 1.5V is required from the node. It is for this reason that each transmission line requires a separate Thevenin termination. If two transmission lines were connected to the same V_T node and one bit was LOW while the other was HIGH there would be contention. Therefore, while this Thevenin approach is somewhat less complicated than the linear regular method, some tradeoffs are made. Resistors are less costly than a regulator but an additional 128 individual resistors would be required for a 64-bit backplane if Thevenin were used instead of a regulator with R_T.

After considering appropriate resistor values and power ratings, what other concerns exist? As with all voltage dividers, a constant path to ground is provided. Therefore, power is constantly dissipated through the resistor combination. Considering this during the Thevenin circuit design, power consumption can be minimized during the resistor selection process. The result can be an effective power supply design that may be more cost effective to produce.

Keep in mind that the Thevenin method consumes twice the power of an “ideal” linear regulator method. The efficiency of the regulator, which varies between applications, will be the deciding factor between choosing the Thevenin or regulator method. Opting for a V_T supply with higher efficiency, such as a fly-back switching supply, can be another consideration, although this option tends to be expensive. Both the Thevenin and regulator methods can provide the same level of noise isolation if supplied with the proper bypass capacitors.

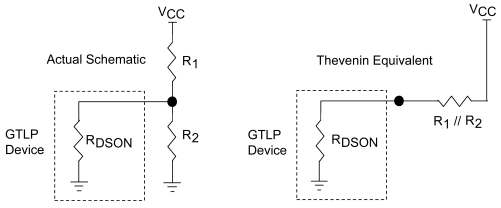

FIGURE 5. Representation of Thevenin Equivalent Circuit for GTLP Termination

Termination Summary

When is the V_T source at fault for signal integrity issues? This is a difficult task since R_T selection is often the largest culprit relating to signal integrity problems. The first sign of an inadequate termination is GTLP signals not reaching the proper V_{OH} level of 1.5V. It is true that R_T can be at fault here, but to further isolate the problem down to the termination supply, adjust the operating frequency to a very low rate thus minimizing line reflections. At 1MHz, a signal not reaching V_{OH} is more than likely due to improper resistor selection, for Thevenin applications, or current limiting. Note what other events may be simultaneously occurring as well. The transmission of a word consisting of 16 LOWs on the same bus but through a different device may be where all the power is distributed. If a required power level cannot be met by a supply it will sacrifice voltage levels to meet current demands. Pay attention to current specifications on supplies and note at what voltage they are specified.

Insufficient capacitor selection for V_T can also affect signal integrity. This is noticed on the falling edge of GTLP signals, which is when the current is sourced from the termination supply. Adjusting the value of the capacitor(s) on the supply will result in minor edge rate changes and even affect the V_{OL} and V_{OH} levels. After calculating one capacitor or set of capacitors, venture to each side of the spectrum and observe the results in signal integrity. Parasitics and underestimated surge currents can exceed the variables used in calculations.

Variable Threshold Voltage V_{REF}

Capable of adjusting the threshold level at which a GTLP edge results in a TTL edge when operating in the BA direction, V_{REF} has the smallest power requirement of the various GTLP voltage levels. Requiring less than 1µA, a simple voltage divider circuit is recommended. Sizing the resistors accordingly for this consistent, small current will limit the amount of power constantly drawn to ground. There is a trade-off between power and noise immunity. Although larger value resistors will require less power, lower impedances will better dampen noise spikes. Using a linear regulator for V_{REF} would be functional but it is over design. Although V_{REF} requires such a small current, do not underestimate the importance of the voltage.

Datasheet specifications recommend ±2% control on V_{REF}, a normally 1V source. Any shifts on this voltage level at the input pin to the GTLP device can introduce unwanted skew and possibly cause false glitches if the shifts are excessive. Sufficient bypass capacitors placed near the device on the V_{REF} line can help a great deal in eliminating false glitches. Since adjusting V_{REF} can improve noise margin and TTL output duty cycle, it is common practice to implement a potentiometer for minor tweaking in an engineering model. High accuracy discrete resistors are typically used in the final model. If any transceiver is dedicated as a driver only, it is not necessary to connect the V_{REF} pin to the1V supply. A connection to ground will suffice for this application. The V_{REF} pin is only required for the receiving function of GTLP devices.

While adjusting V_{REF}, focus should be on the following parameters:

1. TTL Output Duty Cycle

   On a non-inverting GTLP device, TTL output duty cycle will increase as the V_{REF} level is decreased. Select a level that provides the optimum duty cycle for system timing.

2. Signal Integrity

   While adjusting V_{REF} will not improve the shape of signal edges, it can be adjusted to shift the threshold level above or below particularly degraded sections. If the GTLP signal passed through the threshold region twice, i.e. fell below 1V and experienced a slight reflection bringing the signal back up to 1.01V then continuing to fall, a glitch would be evident in the TTL output. A minor V_{REF} adjustment to 1.05V could be a simple fix.

3. Noise Margin Associated with V_{REF}

   Adjust V_{REF} such that upper and lower noise margin, i.e., the distance from V_{REF} to V_{OH} and V_{OL}, are equal. This adjustment better prepares the bus for an unanticipated EMI or noise event.

After adjusting V_{REF}, it is important to observe the changes in all possible configurations so that the backplane can eliminate undesired side effects. Difficulty can sometimes arise when V_{REF} conflicts occur between various card configurations. V_{REF} is typically set at one level but adjusting it through a dynamic control that can sense backplane loading during operation is possible.

Capacitor Selection

Various types and configurations of capacitors are available and necessary in all backplane designs. In any application, they are used to apply control through filtering or as local energy storage devices. On the power node, such as V_{CC}, the bypass capacitor is used to maintain a set voltage bias for the device during current transients. While current transients are not HIGH on the V_{CC} pins, the voltage they condition is crucial to operation of the chip. A V_{CC} drop below 3V for most 3.3V devices degrades the delays for the device to specifications outside those guaranteed in the datasheet. Capacitors selected to protect a voltage drop of 300mV are not the only decoupling to be designed in. High frequency noise on the V_{CC} line should also be filtered as best as possible.

The largest current transients on any GTLP backplane will occur at the V_T node, as discussed earlier. At the V_T node there is no crucial level that must be maintained. Each application will have different noise margin requirements that dictate the V_T level. It is common to maintain V_T within 100mV, since noise margins are often greater than 200mV.

In either of these cases, to include V_{REF} decoupling, selecting the value and number of capacitors is an art that varies between applications. Items to consider include: supply impedance, allowable voltage delta, trace size, lead inductance, equivalent series resistance, resonant frequency, etc. Cookbook equations can be used as a starting point but text references should be consulted prior to final design. The purpose of this application note is to present the various power requirements and configurations of a backplane, which will aide in the selection of decoupling capacitors.

Conclusion

Several specific voltage levels require attention when designing with GTLP. Although each level has its own set of requirements these voltage levels can each be derived from one master voltage supply which simplifies the design and reduces cost.

Having the ability to set the level of these required GTLP voltages is an added bonus to any design. Keeping the datasheet specifications in mind, adjust V_{REF} and V_T through their recommended ranges and observe the effects on the signals. This offers the designer the opportunity to create a robust and custom backplane with superior performance in the application at hand.