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Migrating from the MC68HC811E2 to the MC68HC11F1

By Timothy J. Airaudi
Applications Engineering
Motorola Embedded Control Division
Austin, Texas

Introduction

This engineering bulletin explains how existing users of the MC68HC811E2 could migrate to the MC68HC11F1. The last date that the MC68HC811E2 can be ordered from Motorola is June 30, 2001. However, beyond that date, parts may be available from Motorola distributors.

The MC68HC811E2 is a versatile part used in many different types of applications. This document addresses applications that use the part in expanded mode only.

Customers using single-chip mode should see *Migrating from the MC68HC811E2 to the MC68HC711E9*, Motorola document order number EB380/D.

Migrating to the MC68HC11F1

For current MC68HC811E2 users with external memory systems (expanded mode operation), the MC68HC11F1 is a possible replacement part (see **Table 1**). The MC68HC11F1 can address 64 Kbytes of external memory in expanded mode and requires less glue logic than the MC68HC811E2.

Other advantages of migrating to the MC68HC11F1 are:

- More RAM
- More expanded mode input/output (I/O)
- Non-multiplexed address/data bus
- 3-volt operation
- Ability to run at higher speeds

For complete information on the MC68HC811E2, see the *M68HC11E Family Technical Data*, Motorola document order number M68HC11E/D. For information on the MC68HC11F1, see the *MC68HC11F1 Technical Data*, Motorola document order number MC68H11CF1/D. Both can be found at http://motorola.com/semiconductor (the Motorola World Wide Web site).

Major Differences

The major differences between these two parts are:

- Package options
- Memory map (memory, registers, etc.)
- EEPROM block protect
- CONFIG register
- External glue logic requirements

Table 1. Comparison Chart

Device	MC68HC811E2	MC68HC811F1
RAM (Bytes)	256	1 K
EE (Bytes)	2048	512
Timer	16-bit, 3-4 IC, 4-5 OC, RTI, pulse accumulator	16-bit, 3-4 IC, 4-5 OC, RTI, pulse accumulator
Input/Output (i/O) Expanded	22	30
Serial	SCI SPI	SCI SPI
Analog-to-Digital (A/D)	8-CH, 8-bit	8-CH, 8-bit
Operating Voltage (V)	5.0	3.0 5.0
Maximum Bus Frequency (MHz)	2	3 5
Temperature	C, V, M	C, V, M
Package Options	52 PLCC (FN); 48 DIP (P)	68 PLCC (FN); 80 LQFP (FU)
Comments	Secure device available, MC68SEC811E2; EEPROM block protect	64-K external address bus, 4-program chip select, non-mux address/data bus, 3-V, 3-MHz version (MC68L11F1)
Document Order Number	MC68HC11E/D	MC68HC811F1/D

Difference: Package Options

The MC68HC811E2 is available in 52-pin PLCC (plastic leaded chip carrier) and 48-pin DIP (dual in-line pack) packages. The MC68HC11F1 is available in 68-pin PLCC and 80-pin LQFP (low-profile quad flat pack) packages.

Case 1

Example: 52-pin PLCC

Issue: Only 68-pin PLCC or 80-pin LQFP available

Change required: Re-layout application to allow use of the 68-pin PLCC or the 80-pin LQFP. See **Figure 1** and **Figure 2**.

Case 2

Example: 48-pin DIP

Issue: Only 68-pin PLCC or 80-pin LQFP available

Change required: Re-layout application to allow use of the 68-pin PLCC or the 80-pin LQFP. See **Figure 1** and **Figure 2**.

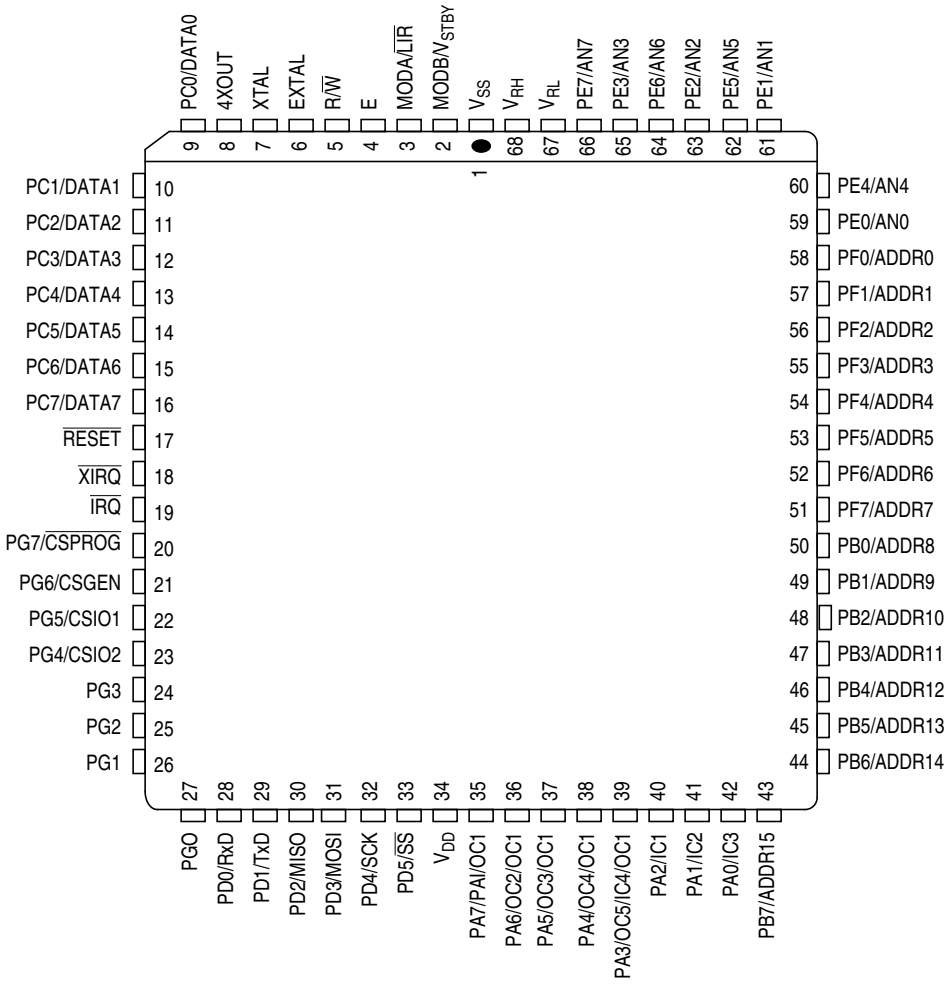


Figure 1. Pin Assignments for MC68HC11F1 68-Pin PLCC

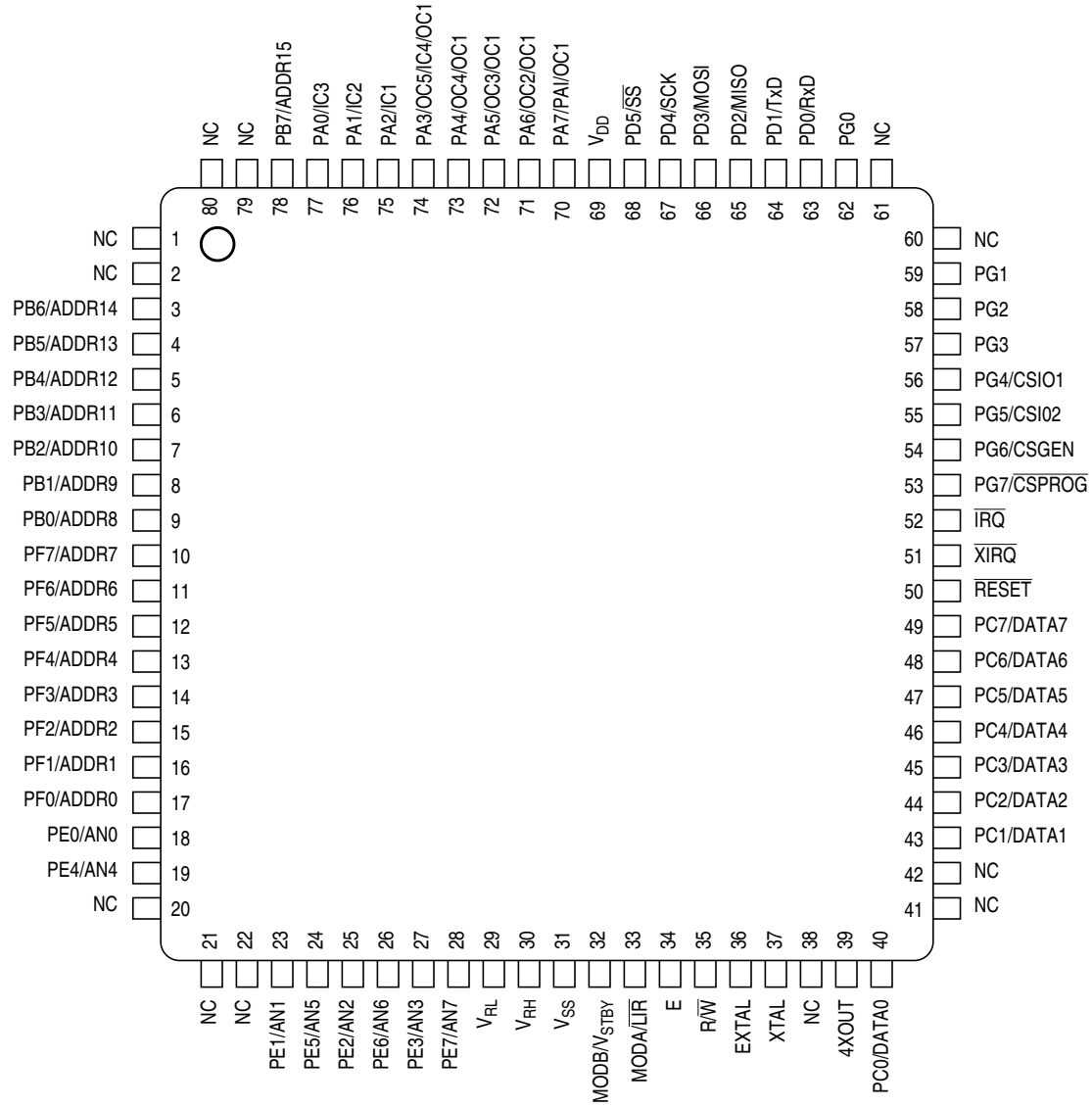


Figure 2. Pin Assignments for MC68HC11F1 80-Pin QFP

Difference: Memory Map (Memory, Registers, etc.)

The MC68HC811E2 has the same memory mapped locations for the normal mode interrupt vectors. The RAM, EEPROM, external addressing, and registers for these devices are different. See **Figure 3** and **Figure 4**.

Case 1

Example:	RAM
Issue:	None
Change required:	None. However, you may want to take advantage of the extra 768 bytes of RAM. This block of RAM is also relocatable on 4-K boundaries in the 64-Kbyte address space by writing an appropriate value into bits 4–7 in the INIT register.

Case 2

Example:	EPROM
Issue:	The MC68HC11F1 has less EEPROM (512 bytes vs. 2048 bytes), and it is located at a different starting address ($FE00 vs. $F800).
Change required:	Change code to use new EEPROM block located from $FE00 to $FFDF.

Case 3

Example:	External address range
Issue:	External address range is different.
Change required:	Change the external address range from $1040–$F7FF to $1060–$FDFF.

Case 4

Example:	Register block
Issue:	Register block is a different size and some register addresses have different meanings.
Change required:	The register block on the MC68HC11F1 is 96 bytes instead of 64-bytes and is located at a default location of $1000–$105F. This block of RAM is also re-locatable on 4-K boundaries in the 64-Kbyte address space by writing to bits 0–3 in the INIT register. These register addresses also have different meanings: $1001, $1002, $1003, $1005, $1006, $1036, $1038, and $103E. $105C–$105F are additional registers.

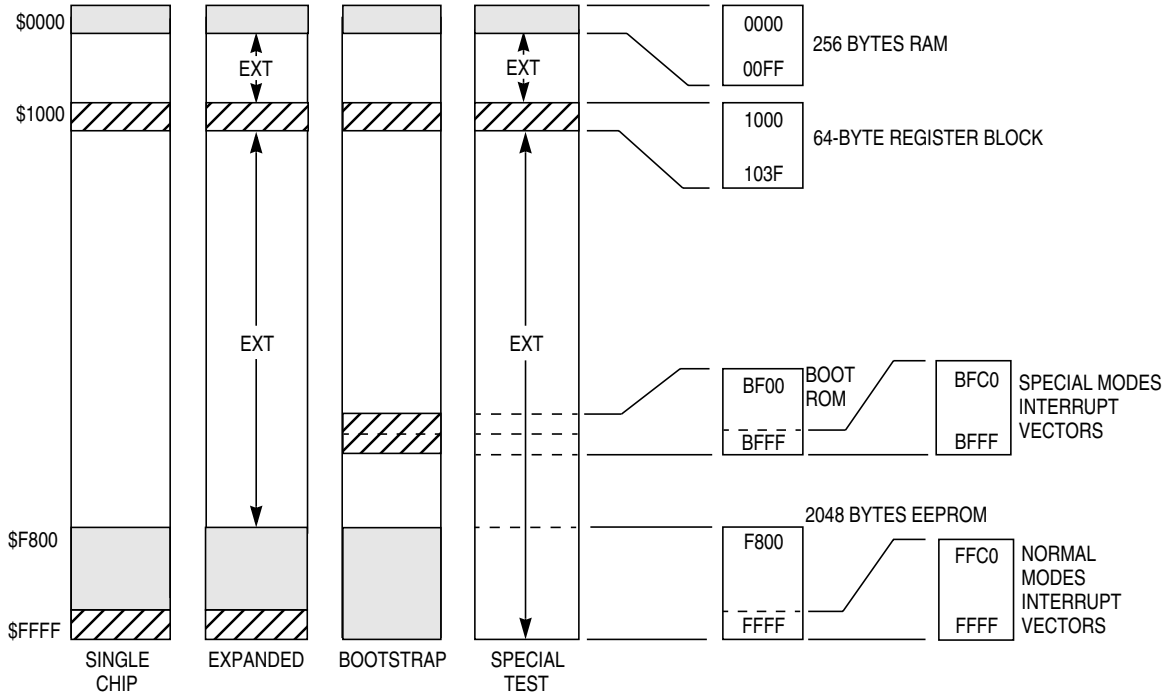
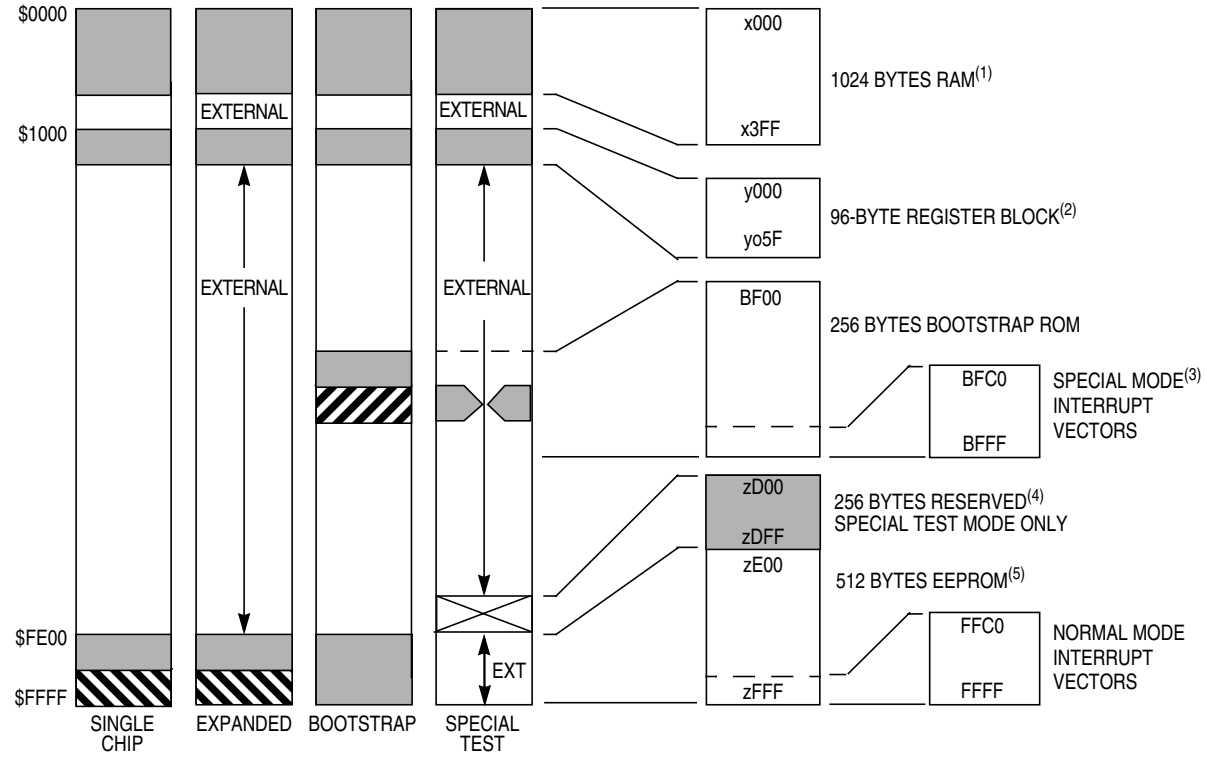


Figure 3. Memory Map for MC68HC811E2



Notes:

1. RAM can be remapped to any 4-byte boundary ($x000). “x” represents the value contained in RAM [3:0] in the INIT register.
2. The register block can be remapped to any 4-byte boundary ($y000). “y” represents the value contained in REG[3:0] in the INIT register.
3. Special test mode vectors are externally addressed.
4. In special test mode the address locations $zD00–$zDFF are not externally addressable. “z” represents the value of bits EE[3:0] in the CONFIG register.
5. EEPROM can be remapped to any 4-byte boundary ($z000). “z” represents the value contained in EE[3:0] in the CONFIG register.

Figure 4. MC68HC11F1 Memory Map

Difference: EEPROM Block Protect

Since these two parts differ significantly regarding EEPROM size and location, the address range and block size that can be protected is different. See **Figure 5**, **Table 2**, and **Table 3**.

Case 1

Example:	EEPROM block protect
Issue:	EEPROM block protect addresses and sizes are different.
Change required:	The BPRT bits in the BPROT register ($1035) must be changed to protect the address ranges and block sizes the user desires.

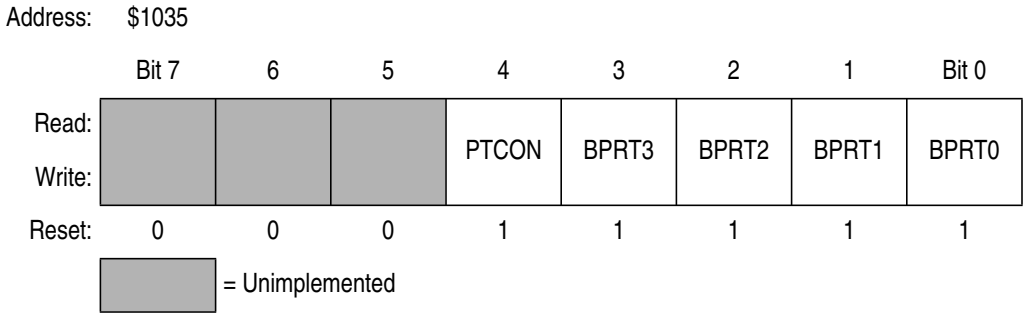


Figure 5. Block Protect Register (BPROT)

Table 2. EEPROM Block Protect in MC68HC811E2 MCUs

Bit Name	Block Protected	Block Size
BPRT0	$xB00–$x9FF	512 bytes
BPRT1	$xA00–$xBFF	512 bytes
BPRT2	$xC00–$xDFF	512 bytes
BPRT3	$xE00–$xFFF	512 bytes

Table 3. EEPROM Block Protection in MC68HC11F1 MCUs

Bit Name	Block Protected	Block Size
BPRT0	$xE00–$xE1F	32 bytes
BPRT1	$xE20-$xE5F	64 bytes
BPRT2	$xE60–$xEDF	128 bytes
BPRT3	$xEE0–$xFFF	288 bytes

Difference: CONFIG Register

The operation of the CONFIG register on the MC68HC811E2 differs from the MC68HC11F1. See **Figure 6**, **Figure 7**, **Table 4**, and **Table 5**.

Case 1

Example: CONFIG register

Issue: Some of the bits in the CONFIG register have different meaning.

Change required: The bits in the CONFIG register ($103F) must be changed to meet the user's requirements. Bit 3 (NOSEC) is not used and bits 4–7 (EEPROM mapping) define different address ranges.

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EE3	EE2	EE1	EE0	NOSEC	NOCOP		EEON
Single-chip reset:	1	1	1	1	U	U	1	1
Bootstrap:	1	1	1	1	U	U(L)	1	1
Expanded:	U	U	U	U	1	U	1	U
Test:	U	U	U	U	1	U(L)	1	0

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

Figure 6. MC68HC811E2 System Configuration Register (CONFIG)

Table 4. MC68HC811E2 EEPROM Mapping

EE[3:0]	EEPROM Location
0000	$0800–$0FFF
0001	$1800–$1FFF
0010	$2800–$2FFF
0011	$3800–$3FFF
0100	$4800–$4FFF
0101	$5800–$5FFF
0110	$6800–$6FFF
0111	$7800–$7FFF

EE[3:0]	EEPROM Location
1000	$8800–$8FFF
1001	$9800–$9FFF
1010	$A800–$AFFF
1011	$B800–$BFFF
1100	$C800–$CFFF
1101	$D800–$DFFF
1110	$E800–$EFFF
1111	$F800–$FFFF

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	EE3	EE2	EE1	EE0		NOCOP		EEON
Reset states:								
Single chip	1	1	1	1	1	P	1	1
Expanded	1	1	1	1	1	P(L)	1	1
Bootstrap	P	P	P	P	1	P	1	P
Special test	P	P	P	P	1	P(L)	1	0

= Unimplemented

P = Previously programmed bit

P(L) = P(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by DISR bit in TEST1 register.

Figure 7. M68HC11F1 System Configuration Register (CONFIG)

Table 5. EEPROM Mapping

EE[3:0]	EEPROM Position
0 0 0 0	$0E00–$0FFF
0 0 0 1	$1E00–$1FFF
0 0 1 0	$2E00–$2FFF
0 0 1 1	$3E00–$3FFF
0 1 0 0	$4E00–$4FFF
0 1 0 1	$5E00–$5FFF
0 1 1 0	$6E00–$6FFF
0 1 1 1	$7E00–$7FFF

EE[3:0]	EEPROM Position
1 0 0 0	$8E00–$8FFF
1 0 0 1	$9E00–$9FFF
1 0 1 0	$AE00–$AFFF
1 0 1 1	$BE00–$BFFF
1 1 0 0	$CE00–$CFFF
1 1 0 1	$DE00–$DFFF
1 1 1 0	$EE00–$EFFF
1 1 1 1	$FE00–$FFFF

Difference:
External Glue Logic Requirements

Case 1

Example: External glue logic

Issue: Some of the external glue logic requirements are different.

Change required: The MC68HC11F1 has a non-multiplexed address/data bus and four programmable chip selects. This will eliminate the need for such external devices as a demultiplexer, a decoder, and a latch. See **Figure 8** and **Figure 9**.

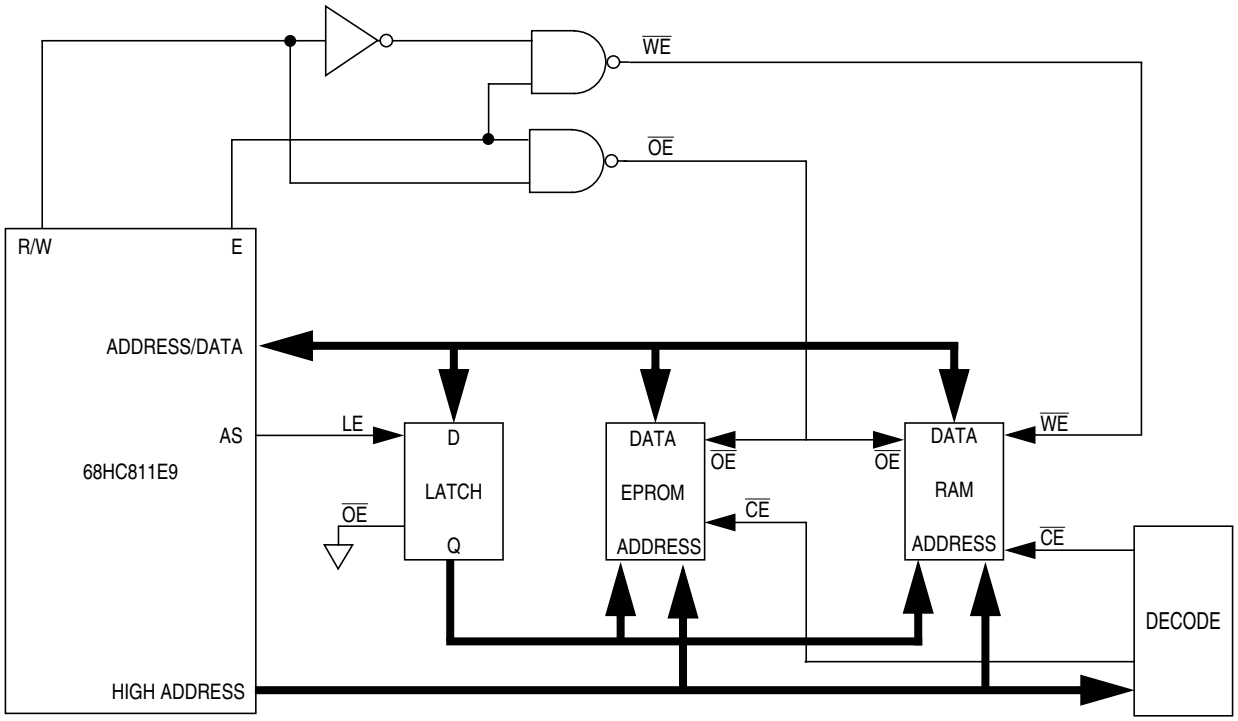


Figure 8. MC68HC811E2 Multiplexed Bus Example

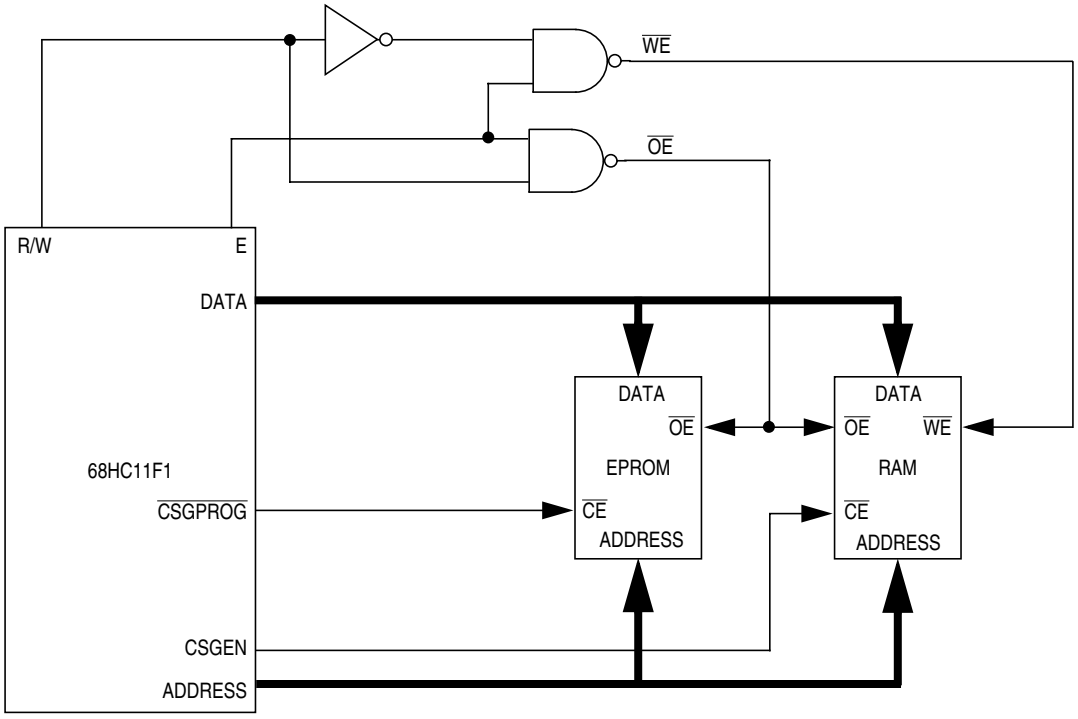


Figure 9. MC68HC11F1 Non-Multiplexed Bus Example

Memory Map Example

This example is for connecting an 8- or 16-Kbyte external RAM and a 32-Kbyte external EPROM. See **Figure 10**.

- Leave internal RAM at default location ($0000–$03FF).
- Leave register block at default location ($1000–$105F).
- Relocate internal EEPROM to address $2E00–$2FFF. This is done by programming the EE0–EE3 bits in the CONFIG register ($103F) to %0010. You may also need to program the EEON bit to ensure that the EEPROM is present in the memory map (see **Figure 7**).
- $\overline{\text{CSPROG}}$ comes up enabled in expanded mode. You will need to program the PSIZA and PSIZB bits in the CSCTL register ($105D) to set an address range. In this example, PSIZA = 0 and PSIZB = 1 ($8000–$FFFF). The user may also want to clear the PSTHA and PSTHB bits in the CSSTRH register ($105C) to ensure no clock stretch is used. Another option with $\overline{\text{CSPROG}}$ is the priority regarding CSGEN. This can be programmed using the GCSPR bit in the CSCTL register.

- For the CSGEN chip select, the G1SZA–G1SZC bits in the CSGSIZ register ($105F) must be programmed to %011 for an 8-Kbyte RAM or to %010 for a 16-Kbyte RAM.
  - Next, the starting address for this address must be programmed. This is done by programming bits GA13 and GA15 for the 8-Kbyte RAM or bits GA14 and GA15 for the 16-Kbyte RAM. Like the $\overline{\text{CSPROG}}$, clear the GSTHA and GSTHB bits to disable the clock stretch.
  - The user should also set the GNPOL bit (bit 4) in the CSGSIZ register to a 0 to make sure chip select CSGEN is an active low. Normally, the chip select for an external RAM device is made active with respect to the E clock going high. In this example, the CSGEN chip select needs to be made active during the address valid time. This is done by setting the GAVLD bit (bit 3) in the CSGSIZ register to a 1.
  - The user should also check the other options available in the CSGSIZ register.

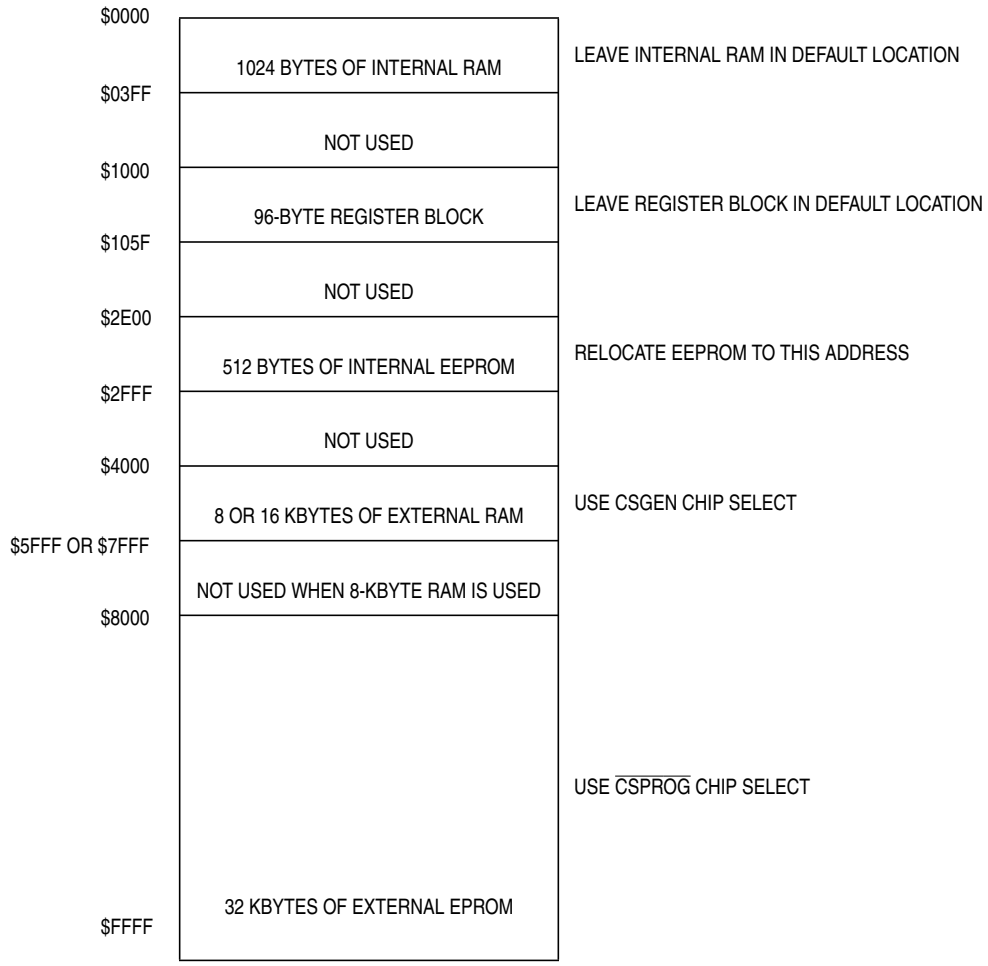


Figure 10. MC68HC11F1 Expanded Mode Memory Map Example

Summary

For those users using the MC68HC811E2 with external memory systems, the MC68HC11F1 is one possible migration path. Customers may also want to look at migrating to the MC68HC711E9 (see *Migrating from the MC68HC811E2 to the MC68HC711E9*, Motorola document order number EB380/D), or to the MC68HC812A4.

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