1. General Description

HE85750 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. Users can chose 32 COM for any one of combination among 【2048 dots LCD Driver + 12 Bit I/O Port】…【1280 dots LCD Driver + 36 Bit I/O Port】etc.. or 48COM for any one of combination among 【2304 dots LCD Driver + 12 Bit I/O Port】…【1152 dots LCD Driver + 36 Bit I/O Port】etc.. The built-in OP comparator can be used with (light、voice、temperature、humility) sensor and used as battery low detection. And the 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The 256KB ROM and 2KB RAM Size can be used in the storage of large speech data, graphic, text etc. It can be applicable to the medium systems such as Small-Scale Dictionary, Data Bank, Medium Level Educational Toy, Lower Second Voice Recording System etc..

The instruction set of HE85750 is easy to learn and simple to use. Only 32 instructions with four addressing modes are provided. Most instructions take only 3 oscillator clocks. The processing power is adequate for most battery operation systems.

2. Features

- Operation Voltage: 2.4V ~ 3.6V
- System Clock: DC ~ 8MHz @ 3.6V
  DC ~ 4MHz @ 2.4V
- Internal ROM: 256K Bytes(64K Program ROM, 192K Data ROM)
- Internal RAM: 2K Bytes.
- Dual Clock System: Fast clock: 32768 ~ 8MHz (No Internal Clock)
  Slow clock: 32.768 Hz
- 4 Operation Mode: Fast, Slow, Idle, Sleep modes.
- Watch Dog Timer to prevent deadlock condition.
- 12~36 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin.
- 2048~1280 dots LCD driver for 32 COM or 2304~1152 dots LCD driver for 48 COM (B TYPE selectable). LV3 must less than 8.5V.
- LCD refresh cycle of 85750 is different from other's 64 Hz. For this IC:
  32 COM: Refresh Cycle=~170Hz，48 COM: Refresh Cycle=~110Hz.
- 7-bit current-type DAC output.
- built-in OP comparator.
- PWM device.
- Two external interrupts and three internal timer interrupts.
- Two 16-bit timer and one Time Base.
- Instruction set: 32 instructions with 4 addressing modes. 11-bit DATA POINTER for RAM and 18-bit TABLE POINTER for ROM.

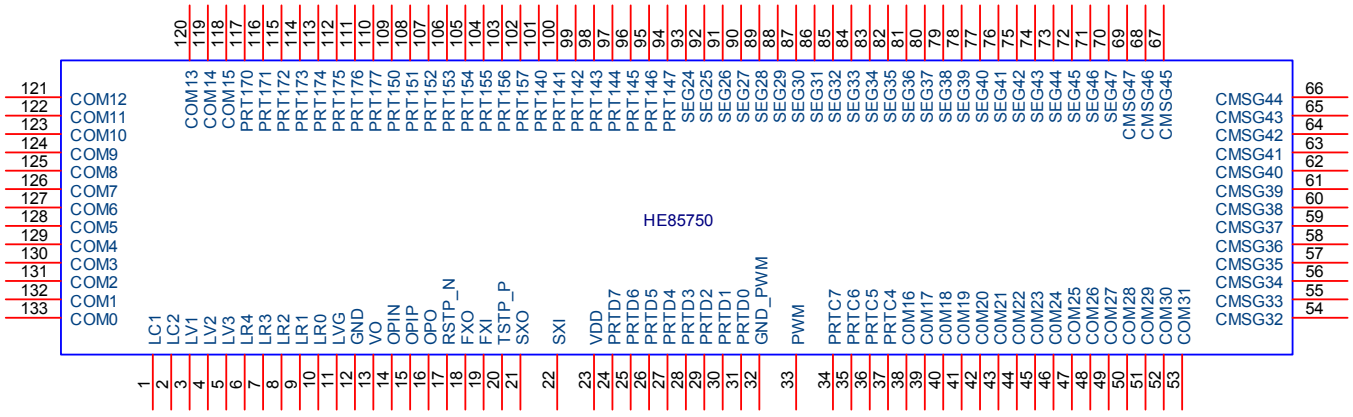
3. Internal Block

Please always keep in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
◎	◎	◎	64KB	192KB	18-bit	◎	2KB	3-bit	8-bit	12~36	—	◎	T1,T2,TB

VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
◎	—	◎	◎	2304~1152	32*64,48*48	1/7, 1/8	—	1,3/2,2,3	◎	4:0	◎	—	—

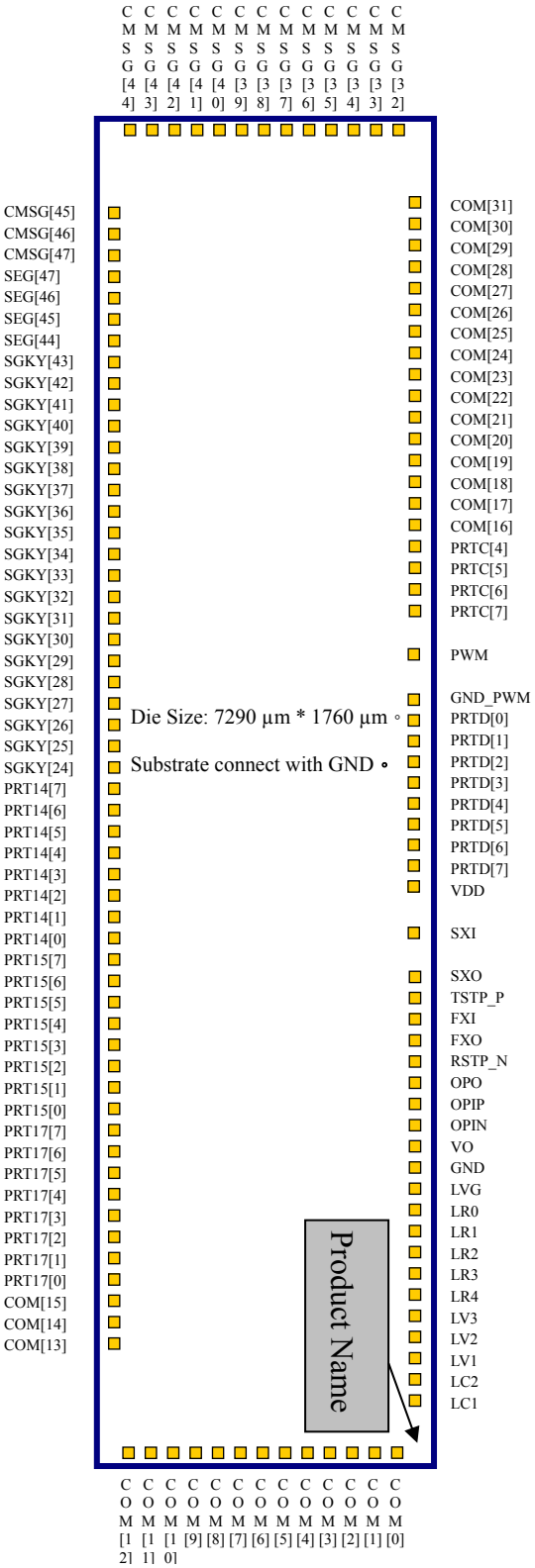
4. Pin Description



Pin No	Pin Name	I/O	Function	Description
19, 18	**FXI, FXO**	B, O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting： MO_FCK/SCKN= 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
22, 21	**SXI, SXO**	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	
17	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
20	**TSTP_P**	I	Test Pin	**Please bond this pin and add a test point on PCB for debugging. Please connect this pin with zero ohm resistor to GND.**

Pin No	Pin Name	I/O	Function	Description
34..37	**PRTC[7:4]**	B	4-pin bi-directional I/O port.	Mask options： MO_CPP[7..5]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
24..31	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external interrupt pin.	Mask options： MO_DPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
94..101	**PRT14[7:0]/ SEG[23:16]**	B/O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO14[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_14PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
102..109	**PRT15[7:0]/ SEG[15:8]**	B/O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO15[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_15PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
110..117	**PRT17[7:0]/ SEG[7:0]**	B/O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO17[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_17PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever uses them as input (No tri-state structure).
53..38 118..133	**COM[31:0]**	O	LCD COMMON Output	LCD Data filled from ***PAGE 6 and 7***, please refer the LCD RAM map.
69..54	**CMSG[47:32]**	O	COM[47:32] / SEG[48:63]	
70..93	**SEG[47:24]**	O	LCD SEGMENT Output	
2	**LC2**	B	Charge Pump Switch 1	Add one 0.1 µF capacitor between LC1 and LC2. Please refer the application circuit.
1	**LC1**	B	Charge Pump Switch 2	
5	**LV3**	B	Charge Pump V3	LV3< 8.5 Volts. Please refer the application circuit.
4	**LV2**	B	Charge Pump V2	
3	**LV1**	B	Charge Pump V1	
6..10	**LR[4..0]**	B	LCD Resister level 4 ~ 1	Please refer the application circuit.
11	**LVG**	I	LCD Virtual Ground	Please refer the application circuit.
33	**PWM**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
13	**VO**	O	D/A output.	Bit 1 of VOC = '1' , Turn on DA
14	**OPIN**	I	DAC Voice Output	Set the VOC[1] (DA=1) to turn on DAC with VO output. Built-in OP comparator. Set the VOC[0] = '1' , Turn on OP
15	**OPIP**	I	OPAMP negative input pin.	
16	**OPO**	O	OPAMP positive input pin.	
23	**VDD**	P	OPAMP output pin.	All of power must connect to power source, can not be floating.
12	**GND**	P	Power Ground Input	
32	**GND_PWM**	P	Dedicated PWM Ground	

5. Pad Location

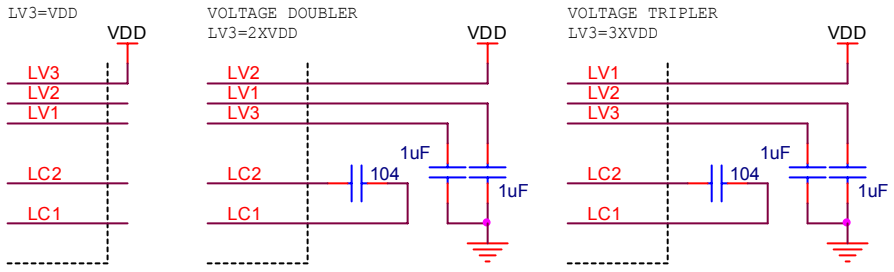


PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	LC1	3149.55	815.00	68	CMSG[46]	-2975.90	-815.00
2	LC2	3033.65	815.00	69	CMSG[47]	-2860.00	-815.00
3	LV1	2917.75	815.00	70	SEG[47]	-2744.10	-815.00
4	LV2	2801.85	815.00	71	SEG[46]	-2628.20	-815.00
5	LV3	2685.95	815.00	72	SEG[45]	-2512.30	-815.00
6	LR4	2570.05	815.00	73	SEG[44]	-2396.40	-815.00
7	LR3	2454.15	815.00	74	SGKY[43]	-2280.50	-815.00
8	LR2	2338.25	815.00	75	SGKY[42]	-2164.60	-815.00
9	LR1	2222.35	815.00	76	SGKY[41]	-2048.70	-815.00
10	LR0	2106.45	815.00	77	SGKY[40]	-1932.80	-815.00
11	LVG	1990.55	815.00	78	SGKY[39]	-1816.90	-815.00
12	GND	1874.65	815.00	79	SGKY[38]	-1659.60	-815.00
13	VO	1758.75	815.00	80	SGKY[37]	-1543.70	-815.00
14	OPIN	1642.85	815.00	81	SGKY[36]	-1427.80	-815.00
15	OPIP	1526.95	815.00	82	SGKY[35]	-1311.90	-815.00
16	OPO	1411.05	815.00	83	SGKY[34]	-1196.00	-815.00
17	RSTP_N	1295.15	815.00	84	SGKY[33]	-1080.10	-815.00
18	FXO	1179.25	815.00	85	SGKY[32]	-964.20	-815.00
19	FXI	1063.35	815.00	86	SGKY[31]	-848.30	-815.00
20	TSTP_P	947.45	815.00	87	SGKY[30]	-732.40	-815.00
21	SXO	831.55	815.00	88	SGKY[29]	-616.50	-815.00
22	SXI	675.55	815.00	89	SGKY[28]	-500.60	-815.00
23	VDD	424.55	815.00	90	SGKY[27]	-384.70	-815.00
24	PRTD[7]	308.65	815.00	91	SGKY[26]	-268.80	-815.00
25	PRTD[6]	192.75	815.00	92	SGKY[25]	-152.90	-815.00
26	PRTD[5]	76.85	815.00	93	SGKY[24]	-37.00	-815.00
27	PRTD[4]	-39.05	815.00	94	PRT14[7]	94.20	-815.00
28	PRTD[3]	-154.95	815.00	95	PRT14[6]	210.10	-815.00
29	PRTD[2]	-270.85	815.00	96	PRT14[5]	326.00	-815.00
30	PRTD[1]	-386.75	815.00	97	PRT14[4]	441.90	-815.00
31	PRTD[0]	-502.65	815.00	98	PRT14[3]	557.80	-815.00
32	GND_PWM	-618.15	815.00	99	PRT14[2]	673.70	-815.00
33	PWM	-778.90	815.00	100	PRT14[1]	789.60	-815.00
34	PRTC[7]	-943.55	815.00	101	PRT14[0]	905.50	-815.00
35	PRTC[6]	-1059.45	815.00	102	PRT15[7]	1021.40	-815.00
36	PRTC[5]	-1175.35	815.00	103	PRT15[6]	1137.30	-815.00
37	PRTC[4]	-1291.25	815.00	104	PRT15[5]	1253.20	-815.00
38	COM[16]	-1409.15	815.00	105	PRT15[4]	1369.10	-815.00
39	COM[17]	-1525.05	815.00	106	PRT15[3]	1485.00	-815.00
40	COM[18]	-1640.95	815.00	107	PRT15[2]	1600.90	-815.00
41	COM[19]	-1756.85	815.00	108	PRT15[1]	1716.80	-815.00
42	COM[20]	-1872.75	815.00	109	PRT15[0]	1832.70	-815.00
43	COM[21]	-1988.65	815.00	110	PRT17[7]	1948.60	-815.00
44	COM[22]	-2104.55	815.00	111	PRT17[6]	2064.50	-815.00

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
45	COM[23]	-2220.45	815.00	112	PRT17[5]	2180.40	-815.00
46	COM[24]	-2336.35	815.00	113	PRT17[4]	2296.30	-815.00
47	COM[25]	-2452.25	815.00	114	PRT17[3]	2412.20	-815.00
48	COM[26]	-2568.15	815.00	115	PRT17[2]	2528.10	-815.00
49	COM[27]	-2684.05	815.00	116	PRT17[1]	2644.00	-815.00
50	COM[28]	-2799.95	815.00	117	PRT17[0]	2759.90	-815.00
51	COM[29]	-2915.85	815.00	118	COM[15]	2894.85	-815.00
52	COM[30]	-3031.75	815.00	119	COM[14]	3010.75	-815.00
53	COM[31]	-3147.65	815.00	120	COM[13]	3126.65	-815.00
54	CMSG[32]	-3580.00	701.00	121	COM[12]	3580.00	-708.95
55	CMSG[33]	-3580.00	585.10	122	COM[11]	3580.00	-593.05
56	CMSG[34]	-3580.00	469.20	123	COM[10]	3580.00	-477.15
57	CMSG[35]	-3580.00	353.30	124	COM[9]	3580.00	-361.25
58	CMSG[36]	-3580.00	237.40	125	COM[8]	3580.00	-245.35
59	CMSG[37]	-3580.00	121.50	126	COM[7]	3580.00	-129.45
60	CMSG[38]	-3580.00	5.60	127	COM[6]	3580.00	-13.55
61	CMSG[39]	-3580.00	-110.30	128	COM[5]	3580.00	102.35
62	CMSG[40]	-3580.00	-226.20	129	COM[4]	3580.00	218.25
63	CMSG[41]	-3580.00	-342.10	130	COM[3]	3580.00	334.15
64	CMSG[42]	-3580.00	-458.00	131	COM[2]	3580.00	450.05
65	CMSG[43]	-3580.00	-573.90	132	COM[1]	3580.00	597.05
66	CMSG[44]	-3580.00	-689.80	133	COM[0]	3580.00	712.95
67	CMSG[45]	-3091.80	-815.00				

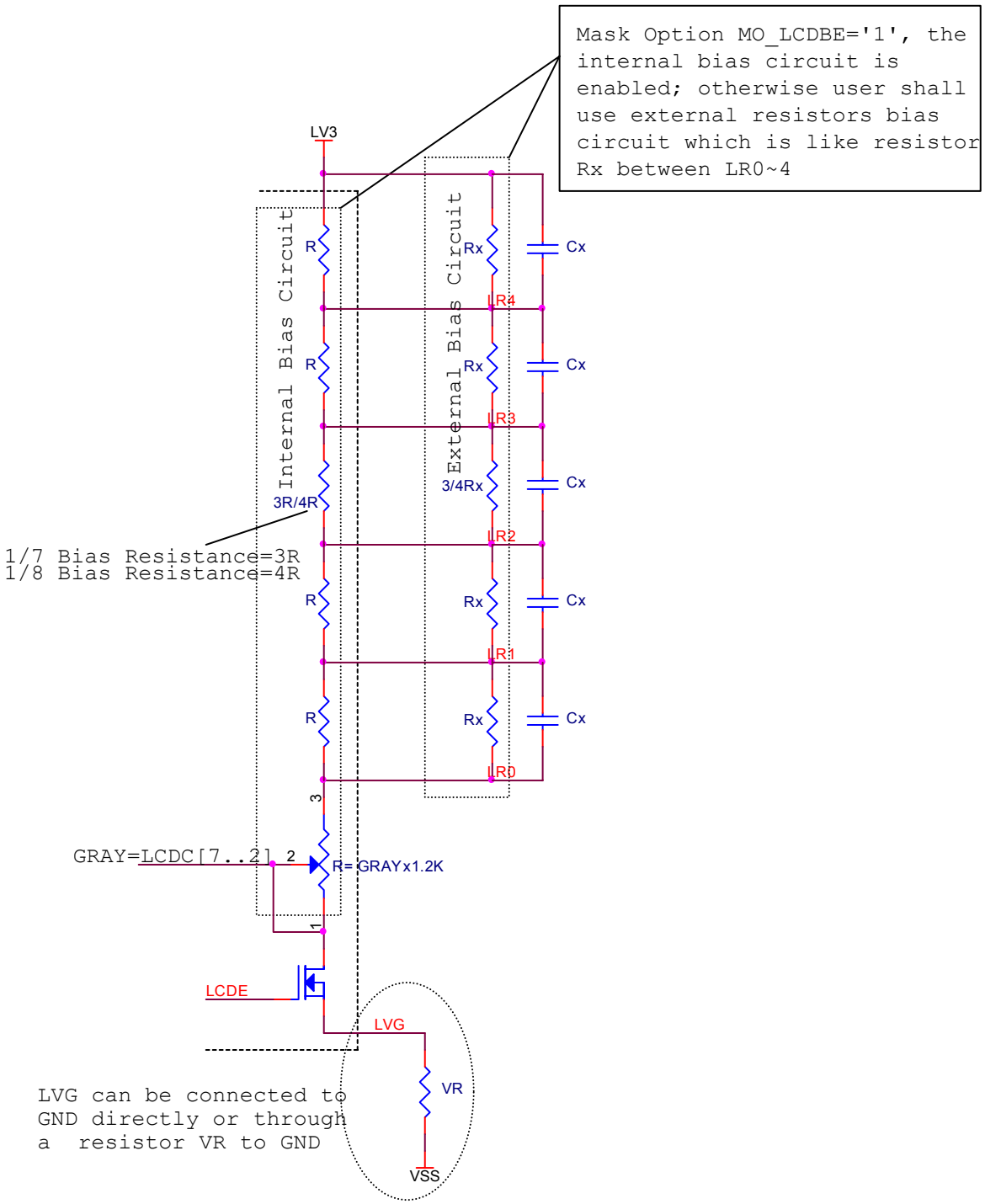
6. LCD Power Supply

The LCD power supply is equipped with voltage charge-pump, and bias voltage generating resistor network. The input power VDD of MCU is charge-pumped to generate LV3. The voltage of LV3 may be up to 1, 2 or 3 times of VDD depending on the external capacitor configurations and VDD connection.



The bias voltages for LCD driver are then generated from LV3 using the internally resistor voltage dividing network if the mask option MO_LCDBE is set to '1' and the resistance of bias voltage generating network can be adjusted by mask option MO_LCDBS[2..0]. Users may select options with smaller resistance to get stronger bias voltages as needed when driving larger LCD panel. However the bias network will consume more power as consequence. Therefore uses must trade off between bias

strength and power consumption. Users also can disable the internal bias circuit and use the external resistor bias circuit by setting the mask option MO_LCDBE to '0'. The LVG pin can be connected to ground directly or connecting to a variable resistor to fine-tune the LCD contrast as below diagram shown.



MO_LCDBS	LCD Bias R ≈
000	30K ohm
001	60K ohm
010	90K ohm
011	120K ohm
100	210K ohm
101	240K ohm
110	270K ohm
111	300K ohm

6.1. LCDC Control register

The contrast of LCD panel can be adjusted by GRAY bits of LCDC register.

LCDC	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Field	GRAY (Contrast adjustment)						BLANK	LCDE
Reset	-	-	-	-	-	-	0	0

Field	Value	Function
GRAY	000000	LCD is darkest
	111111	LCD is lightest
BLANK	0	Normal display
	1	LCD display blanked. LCD driver changes only COM output signal, SEG signal remains unchanged.
LCDE	0	LCD driver disabled, LCD driver has no output signal.
	1	LCD driver Enabled

Please note that LCD driver must be turned off before the entering sleep mode. That means user must clear the bit 0 of LCDC to turn off LCD driving circuit before setting bit6 of OP1 to enter sleep mode. Large current might happen if the procedure is not followed.

Please also note that LCD driver uses slow clock as clock source. The LCD display will not display normally if it works in Fast clock only mode because the LCD refresh action is too fast.
There are two LCD driver configurations.

7. LCD RAM Map

There are two LCD configurations 32/48 COM, user shall write the display data into the related LCD RAM map location to obtain the correct the display image.

32 COM:

Page 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]	SEG [55:48]	SEG [63:56]
COM0	7E0H	7C0H	7A0H	780H	760H	740H	720H	700H
COM1	7E1H	7C1H	7A1H	781H	761H	741H	721H	701H
COM2	7E2H	7C2H	7A2H	782H	762H	742H	722H	702H
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
COM29	7FDH	7DDH	7BDH	79DH	77DH	75DH	73DH	71DH
COM30	7FEH	7DEH	7BEH	79EH	77EH	75EH	73EH	71EH
COM31	7FFH	7DFH	7BFH	79FH	77FH	75FH	73FH	71FH

48 COM:

Page 6, 7	SEG [7:0]	SEG [15:8]	SEG [23:16]	SEG [31:24]	SEG [39:32]	SEG [47:40]
COM0	7C0H	780H	740H	700H	6C0H	680H
COM1	7C1H	781H	741H	701H	6C1H	681H
:	:	:	:	:	:	:
COM15	7CFH	78FH	74FH	70FH	6CFH	68FH
COM16	7D0H	790H	750H	710H	6D0H	690H
:	:	:	:	:	:	:
COM31	7DFH	79FH	75FH	71FH	6DFH	69FH
COM32	7E0H	7A0H	760H	720H	6E0H	6A0H
:	:	:	:	:	:	:
COM46	7EEH	7AEH	76EH	72EH	6EEH	6AEH
COM47	7EFH	7AFH	76FH	72FH	6EFH	6AFH

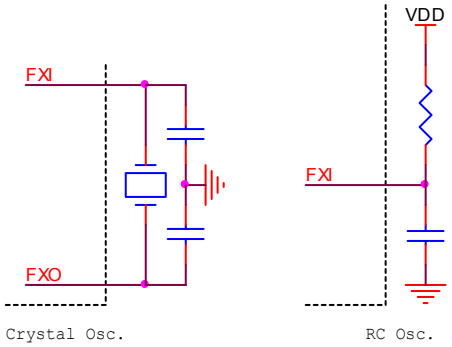
8. Oscillators

The MCU is equipped with two clock sources with a variety of selections on the types of oscillators to choose from. So that system designer can select oscillator types based on the cost target, timing accuracy requirements etc.

OP1	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Field	DRDY	STOP	SLOW	INTE	T2E	T1E	Z	C

OP2	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
Field	IDLE	PNWK	TCWK	TBE	TBS[3..0]			

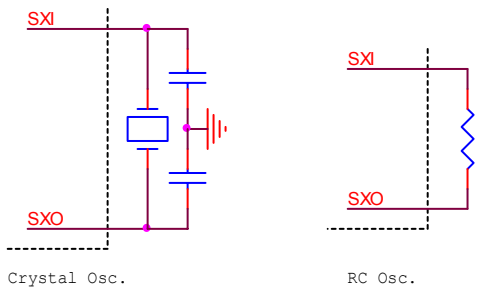
Crystal, Resonator or the RC oscillator can be used as fast clock source, components should be placed as close to the pins as possible. The type of oscillator used is selected by mask option MO_FXTAL.



MO_FXTAL	Fast clock type
0	RC Oscillator.
1	Crystal Oscillator.

Slow clock is the clock source for LCD display, Timer1, and Timer Base, etc. Two types of oscillator, crystal and RC, can be used as slow clock by mask option MO_SXTAL. If used for time keeping function or other applications that required the accurate timing, crystal oscillator is recommended. If the timing accuracy is not important, then RC type oscillator can be used to reduce cost.

MO_SXTAL	Slow clock type
0	R/C oscillator
1	Crystal oscillator



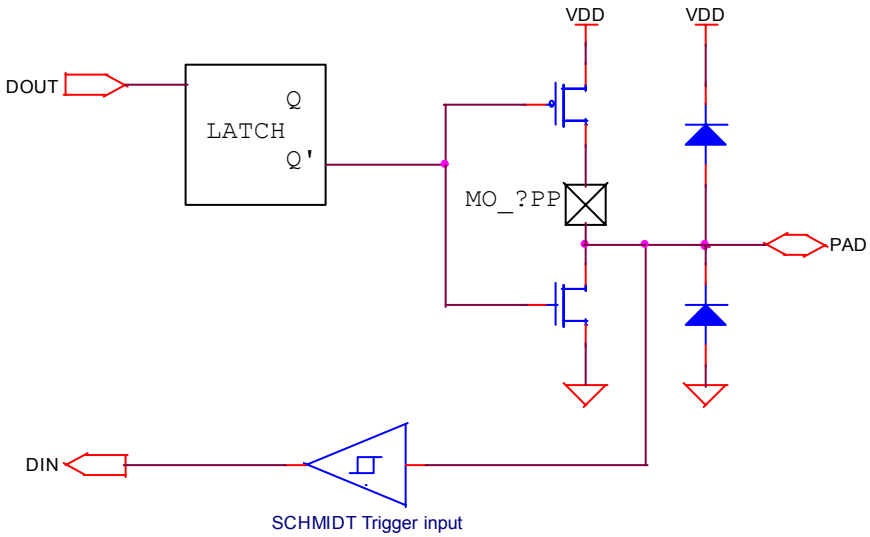
With two clock sources available, the system operation modes can be switched among normal, slow, idle, and sleep modes by the setting of OP1 and OP2 registers as shown in tables below to suit the needs of application such as power saving, etc. If the dual clock mode is used, the LCD display, Timer1 and Timer Base will derive its clock source from slow clock while the other blocks will operate with the fast clock.

9. General Purpose I/O

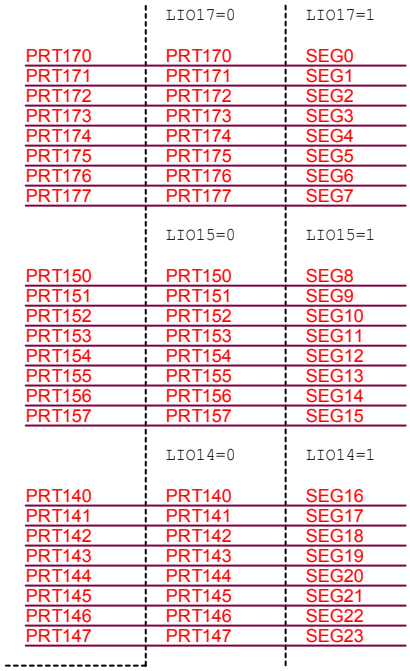
There are two dedicated general purpose I/O port, PRTC[7..4] and PRTD, while PRT14, PRT15 and PRT17 are multiplexed with LCD segment driver pins. All the I/O ports are bi-directional and of non-tri-state output structure. The output has weak sourcing (50 μA) and stronger sinking (1 mA) capability and each can be configured as push-pull or open-drain output structure individually by mask option.

When the I/O port is used as input, the weakly high sourcing can be used as weakly pull-up. Open drain can be used if the pull-up is not required and let the external driver to drive the pin. Please note that a floating pad could cause more power consumption since the noise could interfere with the circuit and cause the input to toggle. A '1' needs to be written to port first before reading the input data from the I/O pin. If the PMOS is used as pull-up, care should be taken to avoid the constant power drain by DC path between pull-up and external circuit.

The input port has built-in Schmidt trigger to prevent it from chattering. Hysteresis level of Schmidt trigger is 1/3*VDD.



As pads of PRT14, PRT15 and PRT17 are shared with LCD segment driver, the function of the pads is determined by mask options.



Following table is the setting for MO_LIO?[...] and MO_?PP[...] and others related to LCD display setting and pin assignment features.

MO_LIO?[…]	MO_?PP[...]	I/O Port	LCD Pin
0	0	Open-drain output	--
0	1	Push-pull output	--
1	0	--	xx
1	1	--	LCD Display

--: Function not available.

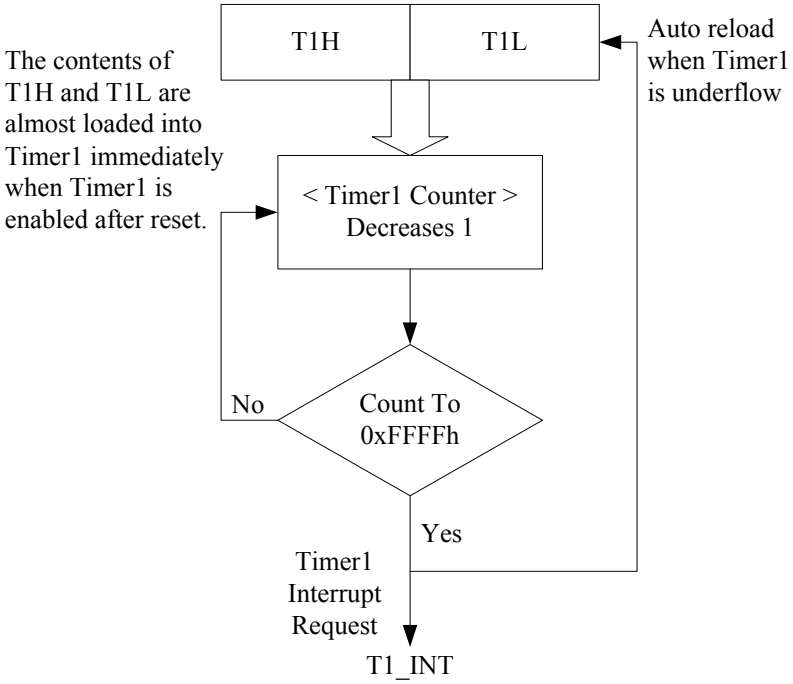
xx: Displayable, but may have abnormal leakage current, do not use.

10. Timer1

The Timer1 consists of two 8-bit write-only preload registers T1H and T1L and 16-bit down counter. If Timer1 is enabled, the counter will decrement by one with each incoming clock pulse. Timer1 interrupt will be generated when the counter underflows - counts down to FFFFH. And the counter will be automatically reloaded with the value of T1H and T1L.

The clock source of Timer1 is derived from slow clock “SCK” at dual clock or slow clock only mode. And it comes from the fast clock “FCK” at fast clock only mode.

Please note that the interrupt is generated when counter counts from 0000H to FFFFH. If the value of T1H and T1L is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this moment, interrupt will be generated immediately and value of T1H and T1L will be loaded since it counts to FFFFH. So the T1H and T1L value should be set before enabling Timer1.



The Timer1 related control registers are list as below:

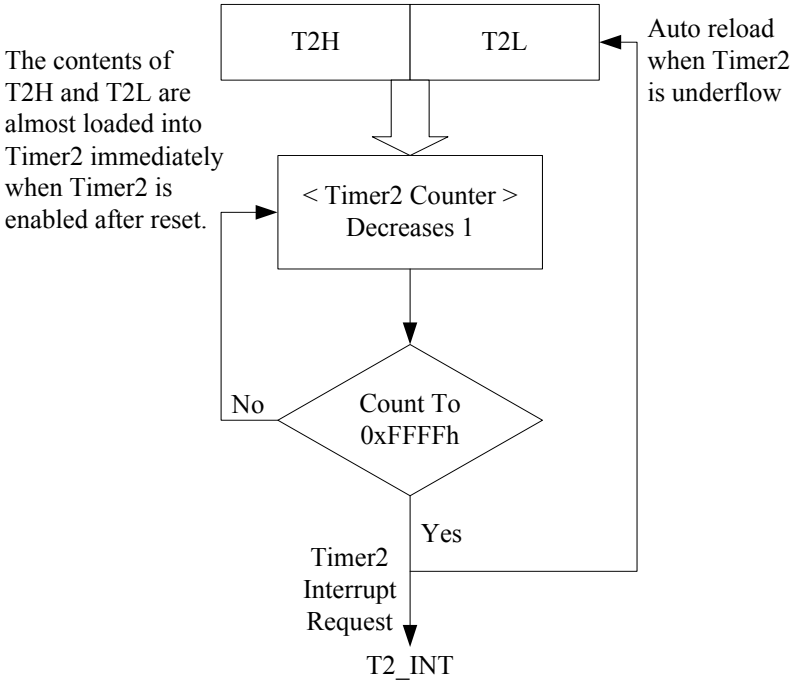
Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC1_IER	2	R/W	0: TC1 interrupt is disabled. (default) 1: TC1 interrupt is enabled.
T1L	0x03	T1L[7:0]	7~0	W	Low byte of TC1 pre-load value
T1H	0x04	T1H[7:0]	7~0	W	High byte of TC1 pre-load value
OP1	0x09	TC1E	2	R/W	0: TC1 is disabled. (default) 1: TC1 is enabled.

11. Timer2

Timer2 is similar in structure to Timer1 except that clock source of Timer2 comes from the system clock "Fsys"/1.5. The system clock "Fsys" varies depending on the operation modes of the MCU.

The Timer2 consists of two 8-bit write-only preload registers T2H and T2L and 16-bit down counter. If Timer2 is enabled, counter will decrement by one with each incoming clock pulse. Timer2 interrupt will be generated when the counter underflows - counts down to FFFFH. And it will be automatically reloaded with the value of T2H and T2L.

Please note that the interrupt signal is generated when counter counts from 0000H to FFFFH. If the value of counter is N, and count down to FFFFH, the total count is N+1. The content of counter is zero when system resets. Once it is enabled to count at this time, the interrupt will be generated immediately and value of T2H and T2L will be loaded since the counter counts to FFFFH. So the T2H and T2L value should be set before enabling Timer2.



The Timer2 related control registers are list as below:

Register	Address	Field	Bit position	Mode	Description
IER	0x02	TC2_IER	1	R/W	0: TC2 interrupt is disabled. (default) 1: TC2 interrupt is enabled.
T2L	0x05	T2L[7:0]	7~0	W	Low byte of TC2 pre-load value
T2H	0x06	T2H[7:0]	7~0	W	High byte of TC2 pre-load value
OP1	0x09	TC2E	3	R/W	0: TC2 is disabled. (default) 1: TC2 is enabled.

12. Time Base Interrupt

The TB timer is used to generate time-out interrupt at fixed period. The time-out frequency of TB is determined by dividing slow clock with a factor selected in OP2[3:0]. TBE (Time Base Enable) bit controls enable or disable of the circuit.

OP2

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IDLE	PNWK	TCWK	TBE	TBS[3..0]			

TBE	Function
0	Disable Time Base
1	Enable Time Base

For example, if the slow clock is 32768 Hz, then the interrupt frequency is as shown in following table.

TBS[3..0]	Interrupt Frequency
0000	16.384 KHz
0001	8.192 KHz
0010	4.096 KHz

TBS[3..0]	Interrupt Frequency
0011	2.048 KHz
0100	1.024 KHz
0101	512 Hz
0110	256 Hz
0111	128 Hz
1000	64 Hz
1001	32 Hz
1010	16 Hz
1011	8 Hz
1100	4 Hz
1101	2 Hz
1110	1 Hz
1111	0.5 Hz

13. Watch Dog Timer

Watch Dog Timer (WDT) is designed to reset system automatically prevent system dead lock caused by abnormal hardware activities or program execution. WDT needs to be enabled in Mask Option.

MO_WDTE	Function
0	WDT disable
1	WDT enable

To use WDT function, "CLRWDT" instruction needs to be executed in every possible program path when the program runs normally in order to clears the WDT counter before it overflows, so that the program can operate normally. When abnormal conditions happen to cause the MCU to divert from normal path, the WDT counter will not be cleared and reset signal will be generated.

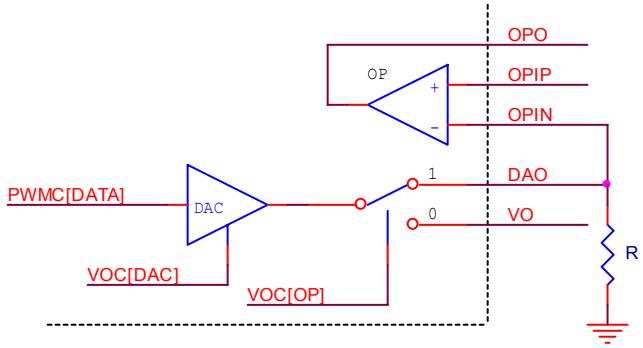
WDT is the enabling signal generated by calculating 32768-clock overflow. Reset Register content is same as TC1 (Timer1 clock), which uses the same clock count source. WDT function can be generated in Normal, Slow and Idle Mode. However, WDT will not function during Sleep Mode (as the TC1 clock has stopped.)

14. Digital-to-Analog Converter

The Digital-to-Analog converter (DAC) converts 7-bit unsigned speech data written to PWMC data register to proportional current.

PWMC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DA & PWM Data	0	DA and PWM output value						
Control	1	PWM O/P driver			-	-	-	PWME

There are two output paths for the DAC. Either VO or DAO can be selected as output port of DAC by VOC register when it is enabled. The VO output is primarily intended for speech generation, although it is not necessary so, while the DAO output path can be used in conjunction with built-in OP comparator to function as an Analog-to-Digital Converter as required in applications such as speech recording, speech recognition or sensor interfaces.



The DAC is enabled by DAC bit of VOC register. Please note that the DAC bit of VOC register will be automatically cleared when the system enter Idle or Sleep mode. So it needs to be set again when returning to Normal mode.

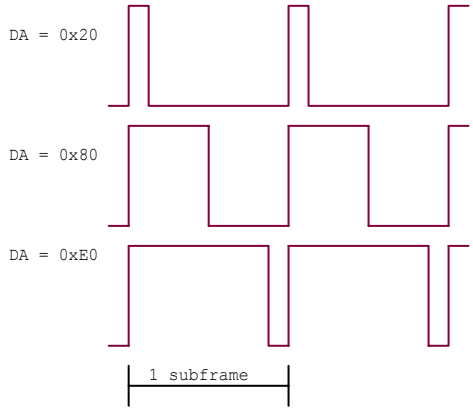
VOC Register

VOC register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Field	-	-	-	-	-	PWM	DAC	OP
Reset	-	-	-	-	-	0	0	0

Bit	Name	Value	Function description
1	DAC	1	DA Enable
		0	DA Disable

15. Pulse-Width Modulation

The pulse-width modulator (PWM) converts 7-bit unsigned speech data written to PWMC data register to proportional duty cycle of PWM output. PWM module shares the PWMC data register with Digit-to-Analog Converter. So PWM and DA output can exist at the same time. When PWM circuit is enabled, it generates signal with duty ratio in proportion to the DA value.



The PWM bit of VOC register controls register to enable the circuit and output driver. When PWM bit of VOC is '0', PWME bit and output drivers settings are both cleared. To use PWM for voice output, PWM bit has to be set to '1' first, then set PWME bit and enable output driver by setting the driver number. If PWM bit is disabled and enabled again, the setting for driver and PWME bit will be clear.

The Fast Clock is gated through PWME bit of PWMC command register to provide the clock source of PWM circuit when it is enabled. As PWM needs higher frequency to operate, it cannot generate correct PWM signal in Slow clock only mode.

When the program enters into Sleep mode or Idle mode, it will automatically turn off all voice outputs by clearing VOC[2:1] to "00". To activate voice output again when returning to Normal Mode, the VOC register needs to be set again.

The PWM output volume can be adjusted by command register PWMC[6:4]. The bit 6 and 5 control 2 time driver, while bit 4 controls 1 time driver, thus it has 5 levels of driver output. By turning on/off the internal drivers, the sound level of PWM output can be turned up and down. Please note that this adjustment apply only to PWM, but not DA output.

PWM output driver selection

PWMC[6..4]	Number of Driver
000	off
001	1
010	2
011	3
100	2
101	3
110	4
111	5

16. Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 5V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

17. Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 3.6V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

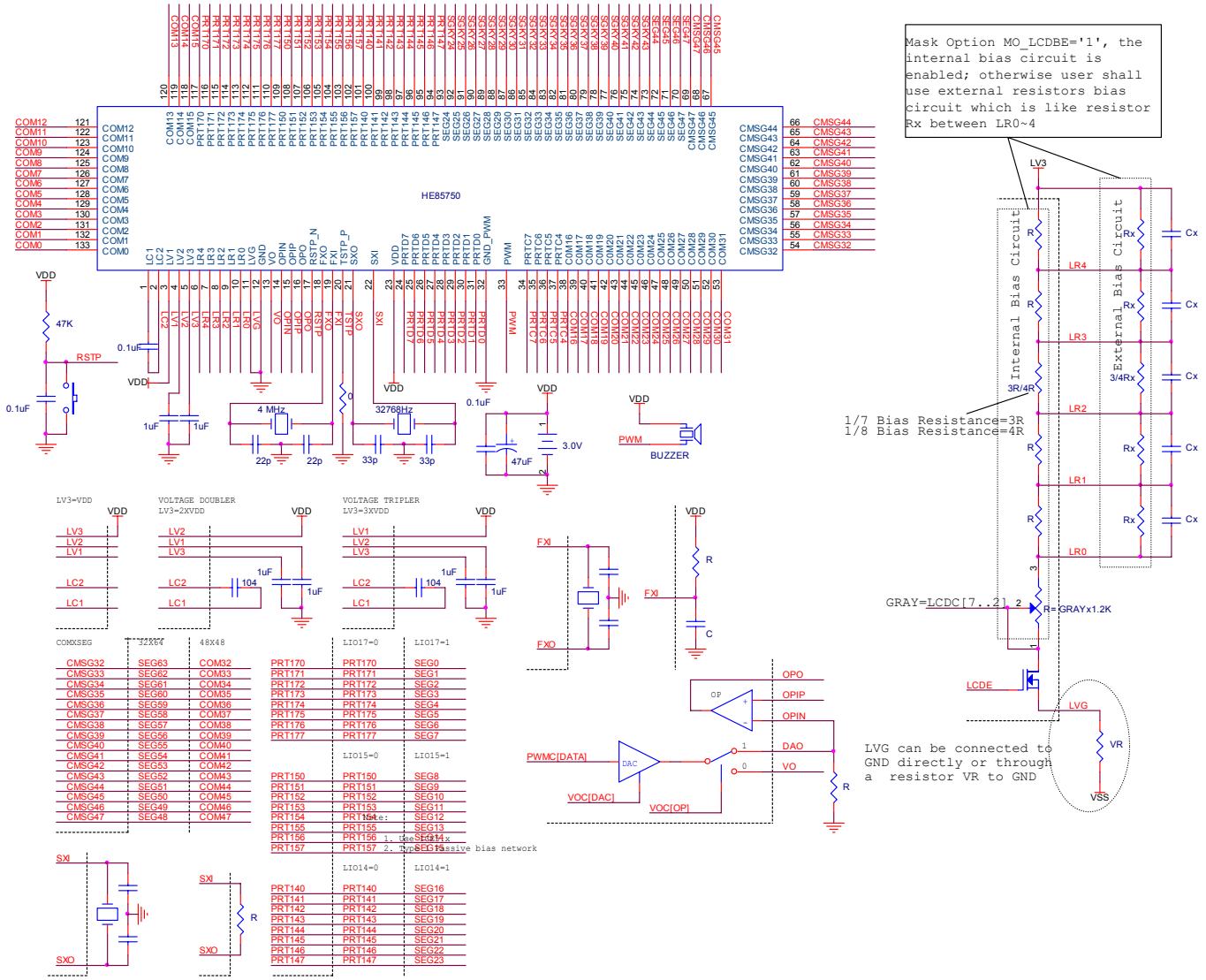
18. DC/AC Characteristics

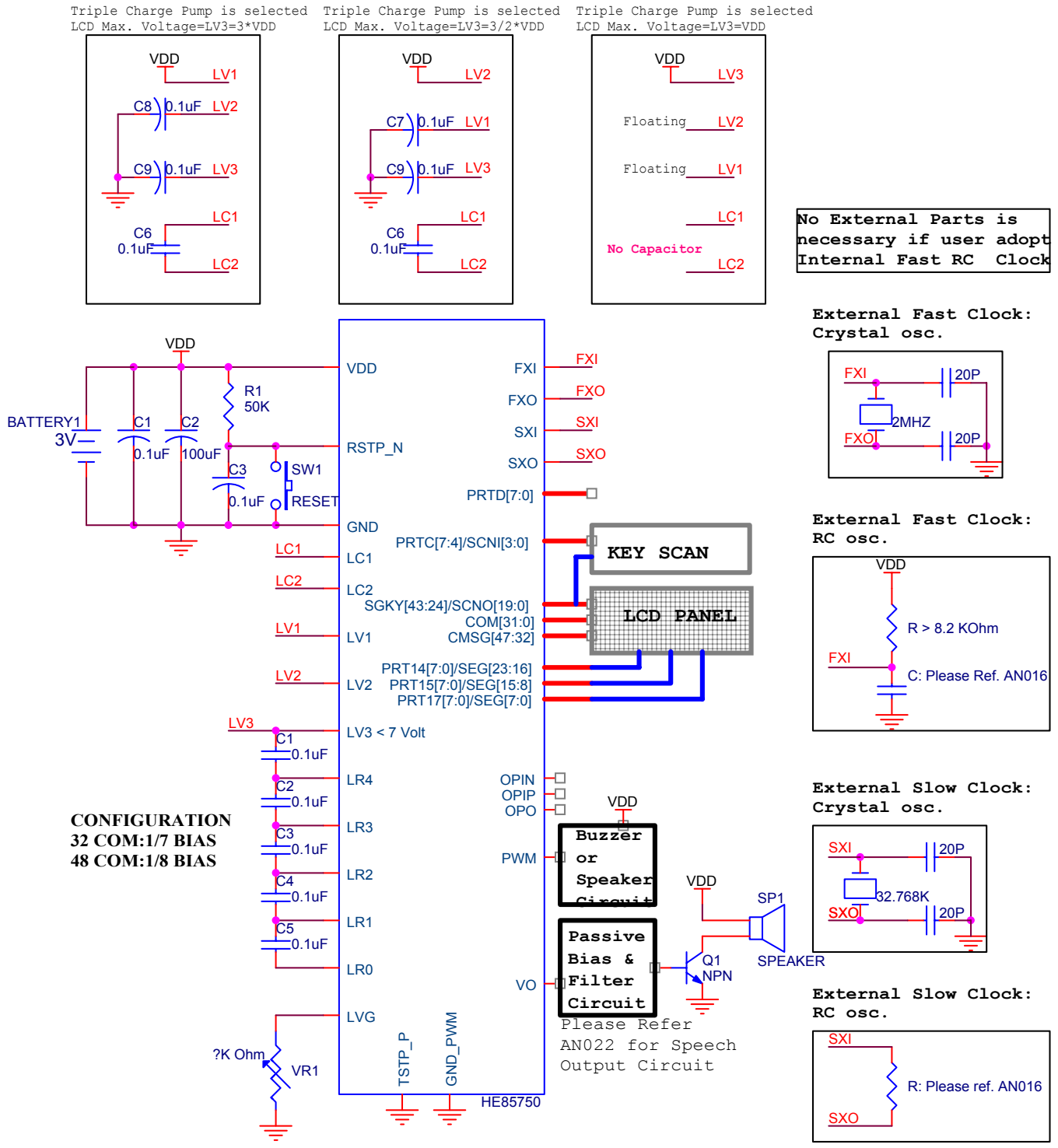
Testing Condition : TEMP=25℃, VDD=3V+/-10%, GND=0V

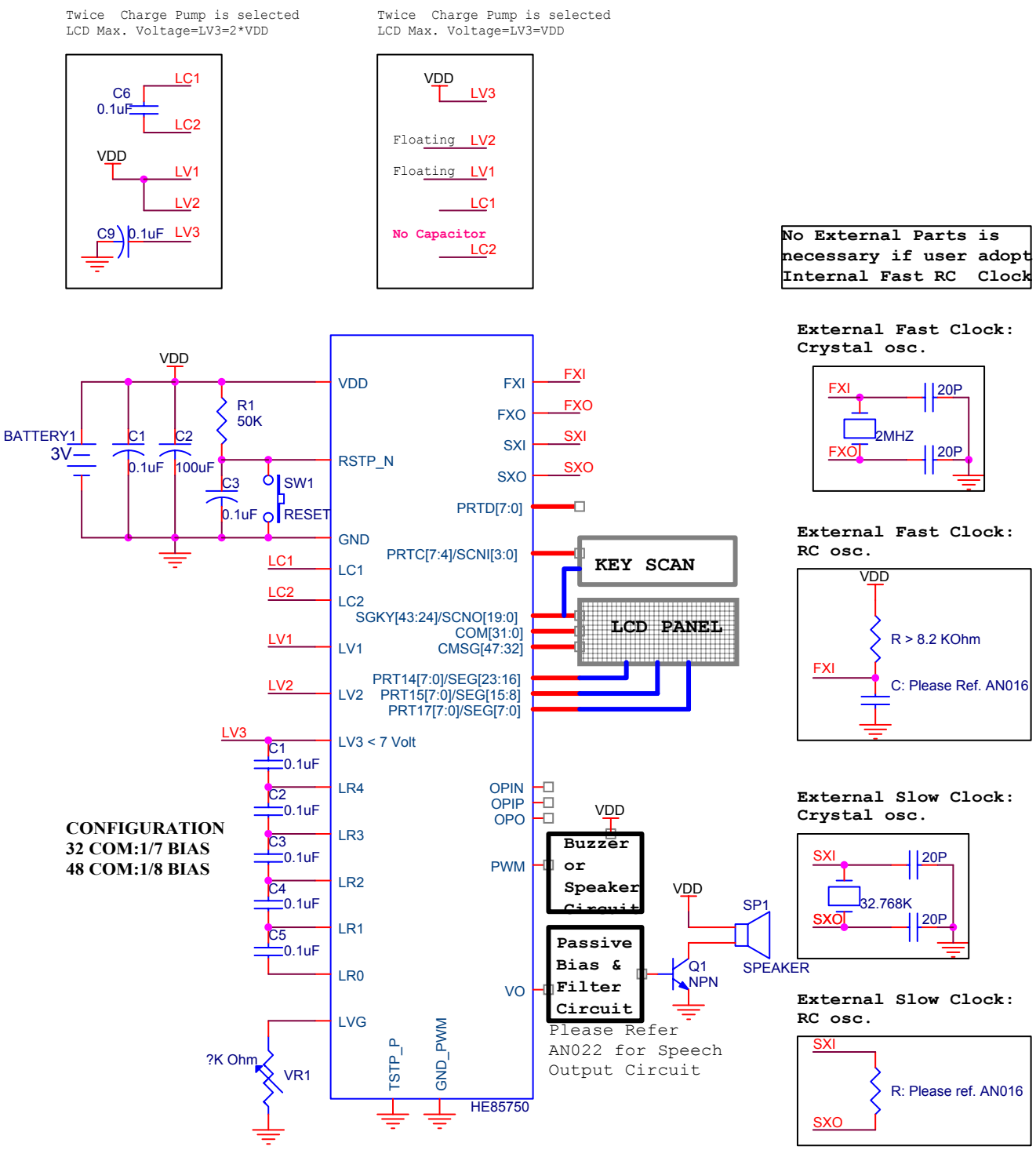
	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		1	1.5	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		15	30	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		10	25	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable, LCD option=128Kohm LV3=6 Volt		65	72	μA
			LCD Enable, LCD option=16Kohm, LV3=6 Volt		300	330	
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{PWM}	PWM Output Current	PWM	With 32Ω Loading	10	14		mA
			With 64Ω Loading	6	8		mA
			With 100Ω Loading	4	5		mA
I_{oVO}	DAC Output Current	VO	V_{DD}=3V;VO=0~2V, Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note:*1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current.
(IPWM * N; N=0,1,2,3,4,5)

19. Application Circuit

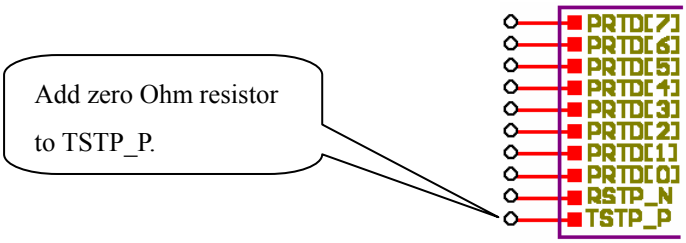






20. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.
2. LCD driving circuit must be turn off before IC goes into sleep mode.
3. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB to do some testing when it's necessary and TSTP_P shall tie to low for normal operation.



4. LV3 must small than 8.5 Volt. Otherwise IC may breakdown.
5. The LCDC of 85750 is different from other IC of HE80000 series. Please Use ICE5.0/5.1 to emulate the LCDC configuration. The LCDC:[G5G4G3G2 G1G0BE]; G[5:0]: gray level control, 64 levels for this body. B: blank control bit. E: LCD enable bit.

21. Updated Record

Version	Date	Section	Original Content	New Content
V1.52	July 30, 2003			Modify the datasheet format and review all the contents, add some sections.