

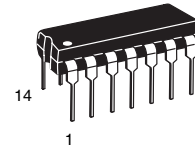
Legacy Device: Motorola MC12002

The ML12002 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

There are two package offerings:

- Plastic Dual Inline 14 Lead, P Dip.
- Plastic Surface Mount 14 Lead SOIC.
- Operating Temperature Range: $T_A = -30^\circ$ to $+85^\circ\text{C}$



P DIP 14 = CP
PLASTIC PACKAGE
CASE 646



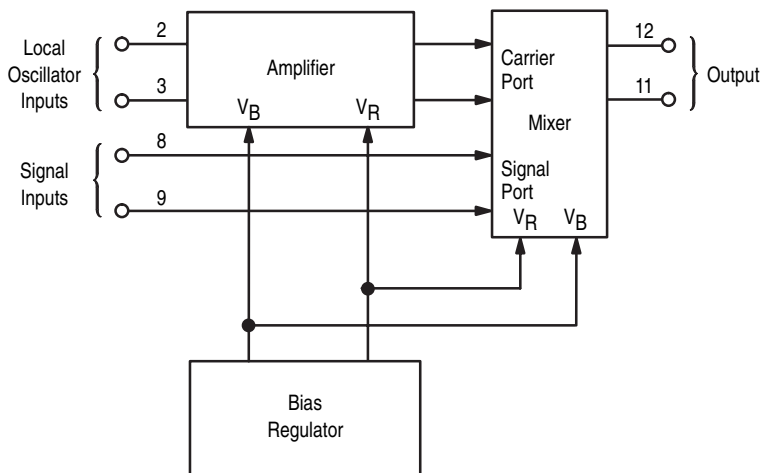
SOG 14 = -5P
SOG
CASE 751A

CROSS REFERENCE/ORDERING INFORMATION

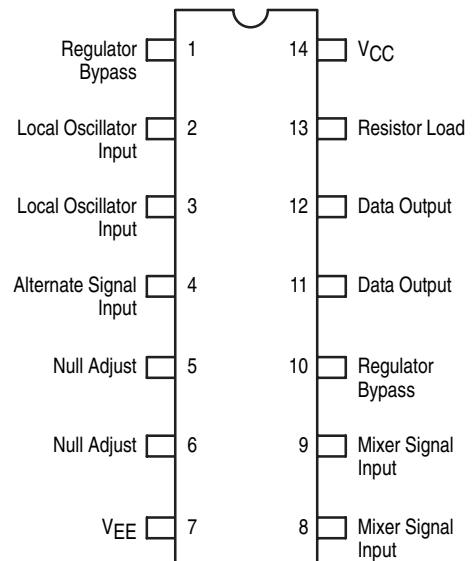
<u>PACKAGE</u>	<u>MOTOROLA</u>	<u>LANSDALE</u>
P DIP 14	MC12002P	ML12002CP
SOG 14	MC12002D	ML12002-5P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

Figure 1. Logic Diagram



PIN CONNECTIONS



(Top View)

ELECTRICAL CHARACTERISTICS										TEST VOLTAGE VALUES			Gnd	
										Volts				
										V _{IHmax}	V _{ILmin}	V _{CC}		
										+2.9	+2.0	+5.0		
Characteristic	Symbol	Pin Under Test	Test Limits						VOLTAGE APPLIED TO PINS LISTED BELOW					
			-30°C		+25°C		+85°C		V _{IHmax}	V _{ILmin}	V _{CC}	Gnd		
			Min	Max	Min	Max	Min	Max					Unit	
Power Supply Drain	I _{CC}	14	—	—	—	16	—	—	mAdc	—	—	11,12,14	5,6,7	
Input Current	I _{inH}	2	—	—	—	0.75	—	—	mAdc	2	—	11,12,14	5,6,7	
		3	—	—	—	0.75	—	—	mAdc	3	—	11,12,14	5,6,7	
		8	—	—	—	0.75	—	—	mAdc	8	—	11,12,14	5,6,7	
		9	—	—	—	0.75	—	—	mAdc	9	—	11,12,14	5,6,7	
	I _{inL}	2	—	—	-0.7	—	—	—	mAdc	—	2	11,12,14	5,6,7	
		3	—	—	-0.7	—	—	—	mAdc	—	3	11,12,14	5,6,7	
		8	—	—	-0.7	—	—	—	mAdc	—	8	11,12,14	5,6,7	
		9	—	—	-0.7	—	—	—	mAdc	—	9	11,12,14	5,6,7	
Output Current	I _{O1}	11	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7	
		12	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7	
	I _{O2}	11	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7	
		12	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7	
	I _{out}	11	—	—	4.2	7.8	—	—	mAdc	2.9	—	11,12,14	5,6,7	
		11	—	—	4.2	7.8	—	—	mAdc	3.8	—	11,12,14	5,6,7	
12		—	—	4.2	7.8	—	—	mAdc	2.8	—	11,12,14	5,6,7		
12		—	—	4.2	7.8	—	—	mAdc	3.9	—	11,12,14	5,6,7		
Differential Current	ΔI _{O1}	11,12	-100	+100	-100	+100	-100	+100	μAdc	—	—	11,12,14	7	
	ΔI _{O2}	11,12	-200	+200	-200	+200	-200	+200	μAdc	—	—	11,12,14	5,6,7	
Bias Voltage	V _{Bias}	1	2.33	2.53	2.32	2.52	2.3	2.5	Vdc	—	—	11,12,14	5,6,7	
		4	390	590	400	600	410	610	mVdc	—	—	11,12,14	5,6,7	
		5	275	415	285	425	295	435	mVdc	—	—	11,12,14	7	
		6	275	415	285	425	295	435	mVdc	—	—	11,12,14	7	
		10	1.26	1.46	1.185	1.385	1.105	1.305	Vdc	—	—	11,12,14	5,6,7	
AC Gain (See Figure 1) (Frequency = 100 MHz) *Note	A _V	11	—	—	5.0	—	—	—	V/V	Pulse In	Pulse Out	-3.0 V	Gnd	V _{EE}
		11	—	—	0.28	—	—	—	V/V	2	11	9	14	7
										8	11	3	14	7

NOTE: *Note: AC Gain is a function of collector load impedance.

Figure 2. Analog Mixer Circuit Schematic

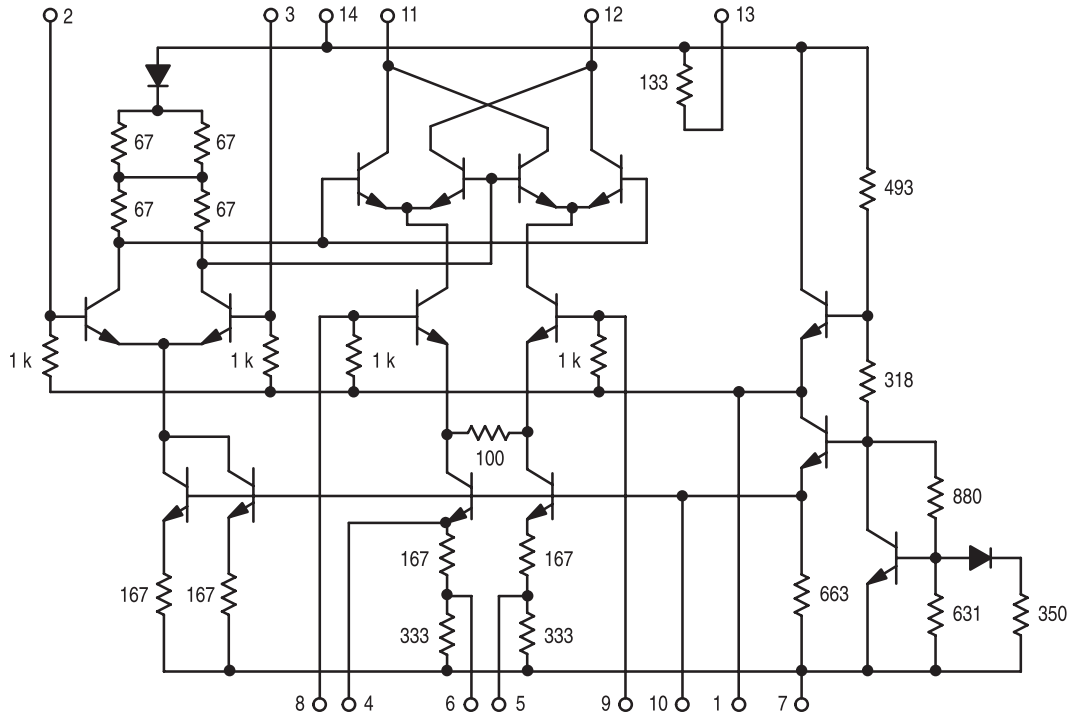
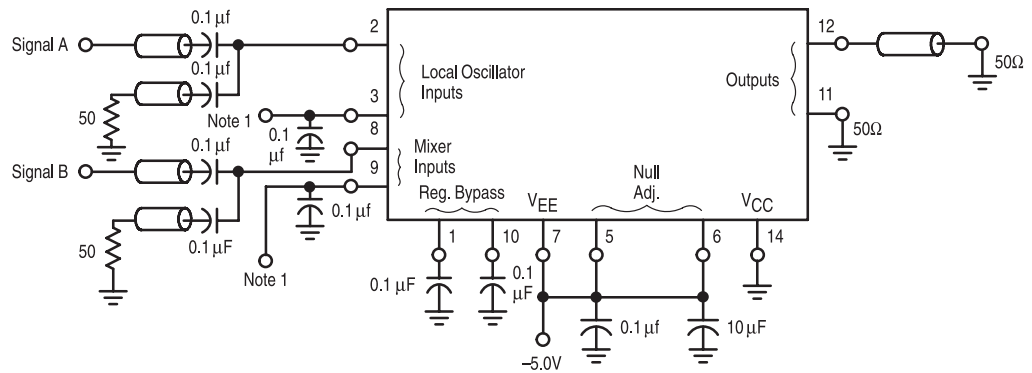


Figure 3. AC Gain Test

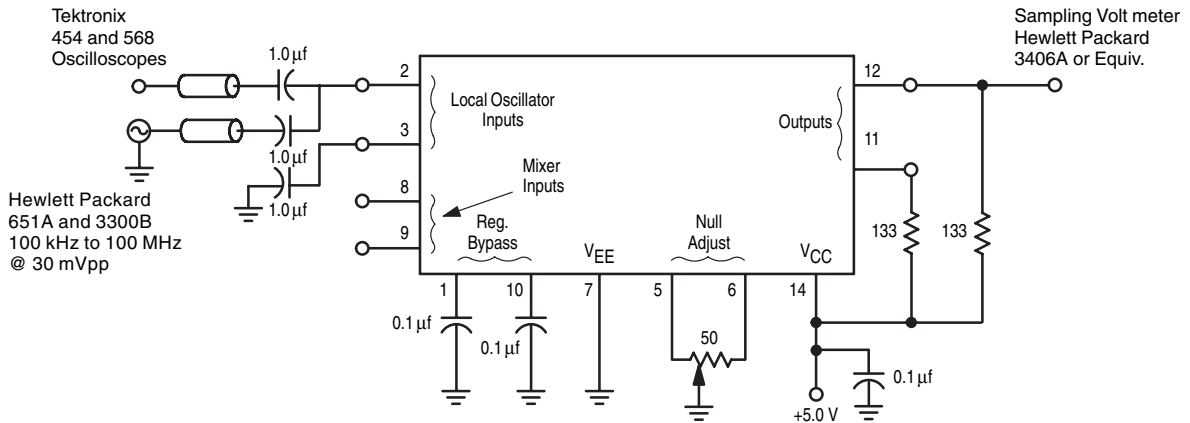
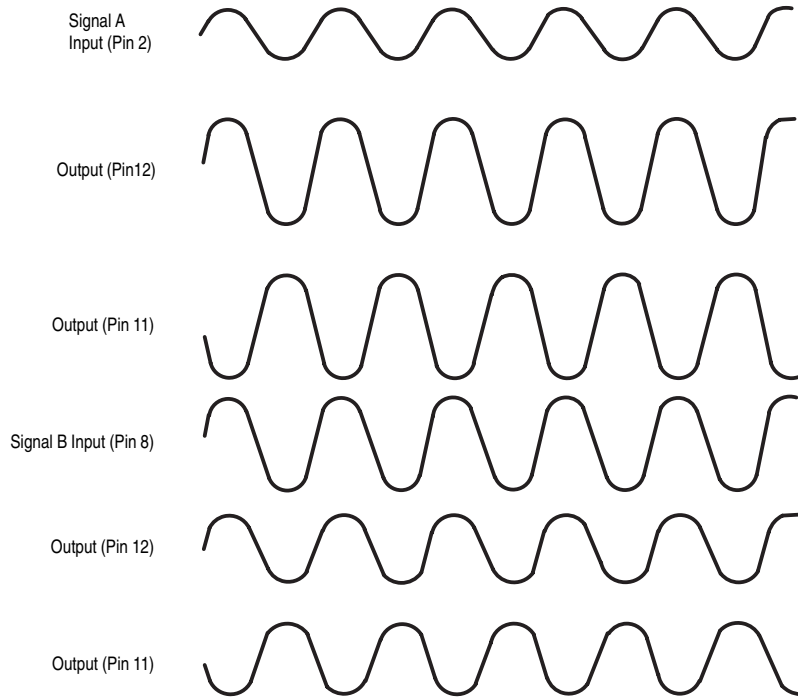


Note 1:
 $V_{IL} = -3.0\text{ V}$ on pin 3 when pin 8 is under test.
 $V_{IL} = -3.0\text{ V}$ on pin 9 when pin 2 is under test.

Signal A = 30 mVpp
 Signal B = 300 mVpp
 Freq. = 100 MHz

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. The unused output is connected to a 50-ohm resistor to ground.

Figure 4. Carrier Feedthrough Test Circuits



Notes:
 Test 1 – Adjust potentiometer for carrier null at $f_c = 100$ kHz.
 Test 2 – Connect pins 5 and 6 to Gnd.

All Input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Figure 5. Carrier Feedthrough versus Frequency (Test 1)

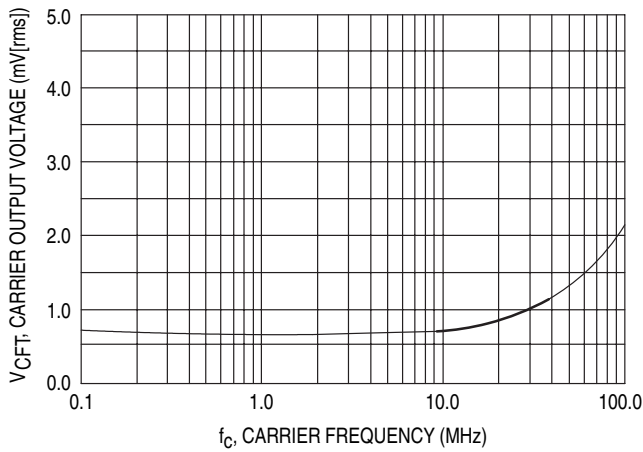


Figure 6. Carrier Feedthrough versus Frequency (Test 2)

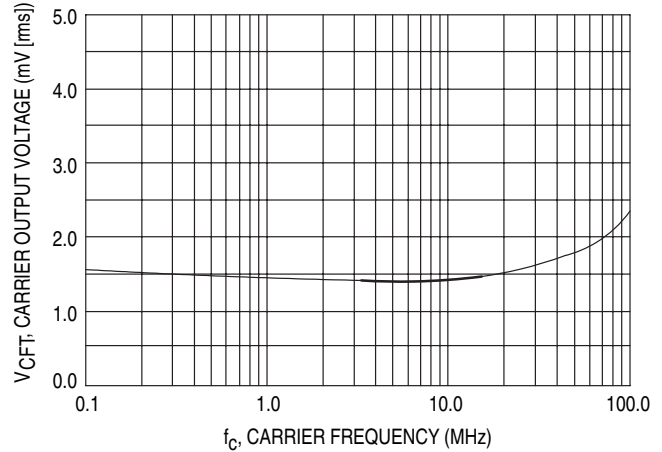
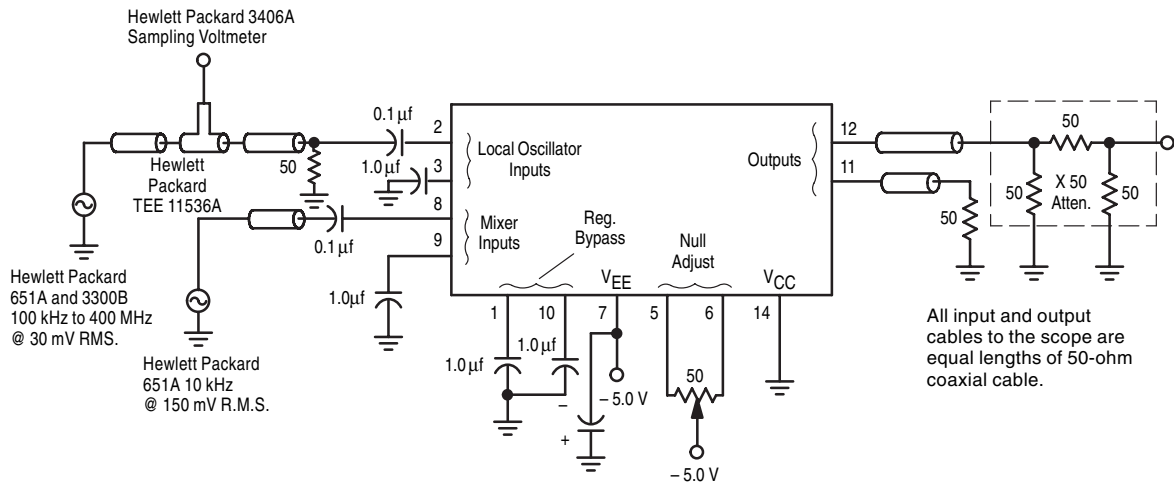


Figure 7. Carrier Suppression Test Circuit



- Notes:
 Test 1 – Adjust potentiometer for carrier null @ $f_c = 100$ kHz
 Test 2 – Connect pins 5 and 6 to -5.0 volts
 Test 3 – Adjust potentiometer for carrier null @ 25° C

Figure 8. Carrier Suppression versus Frequency (Test 1)

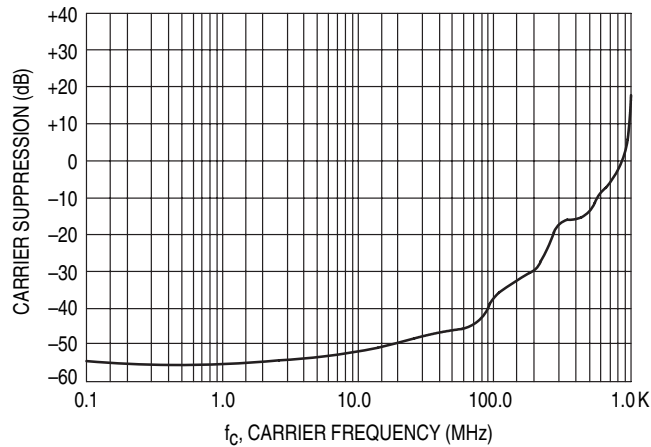


Figure 9. Carrier Suppression versus Frequency (Test 2)

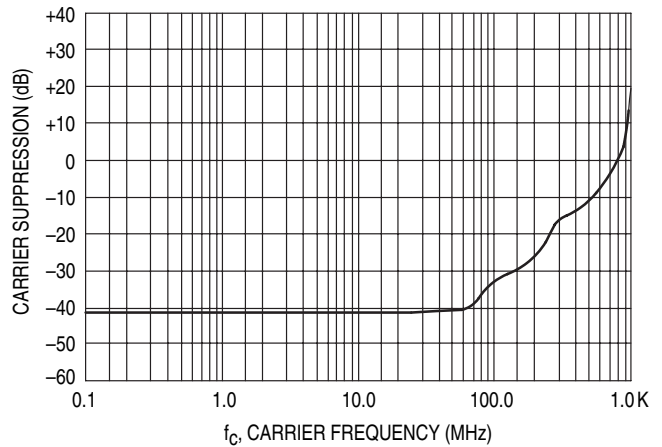


Figure 10. Carrier Suppression versus Temperature

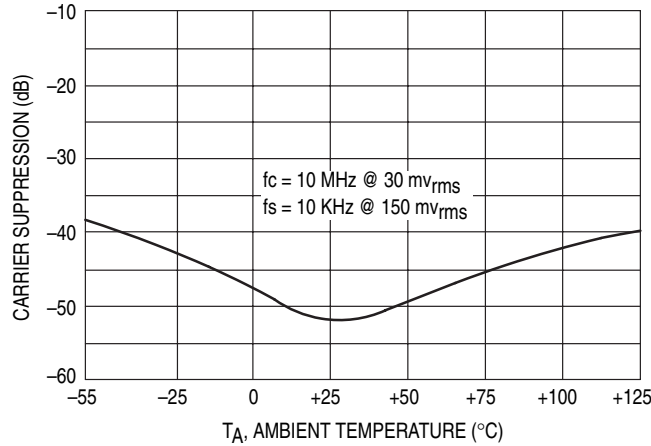


Figure 11a. Output Offset Current (I₀) versus Temperature

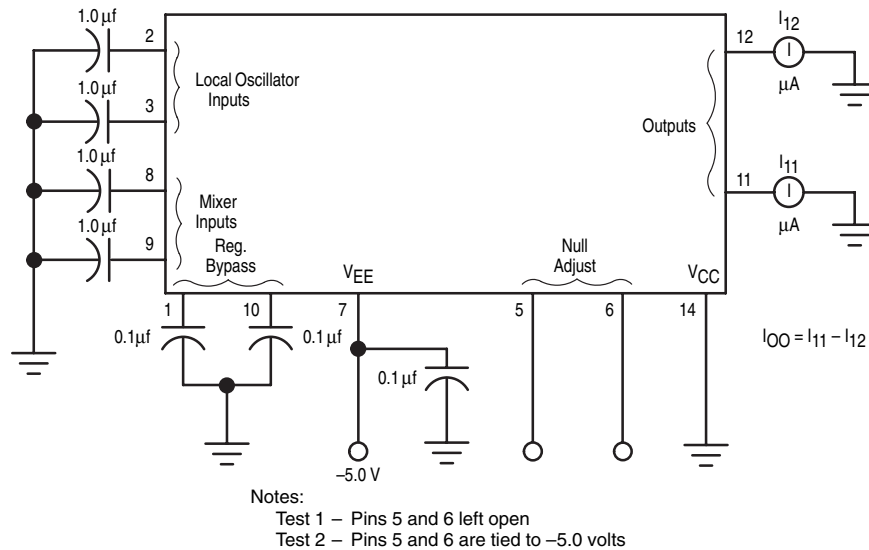


Figure 12. Output Offset Current versus Temperature

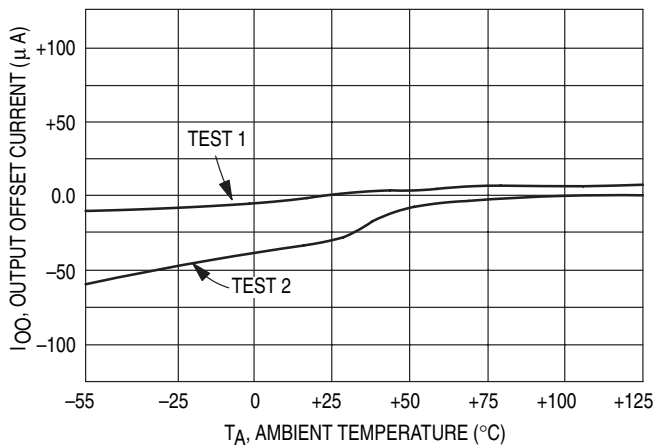
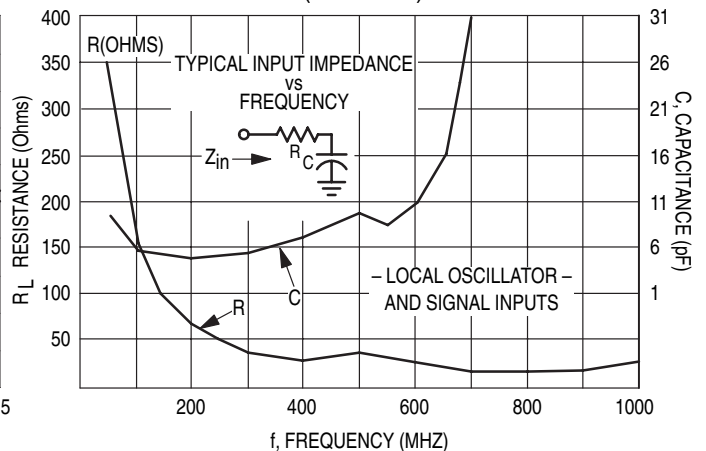


Figure 13. Typical Input Impedance versus Frequency (No Circuit)



AM modulator using ML12002

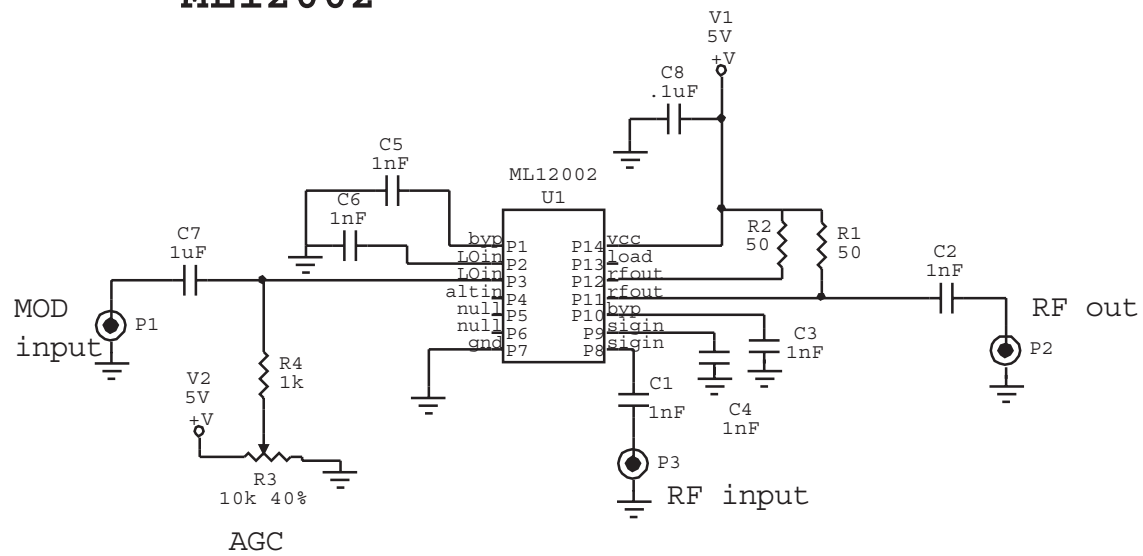
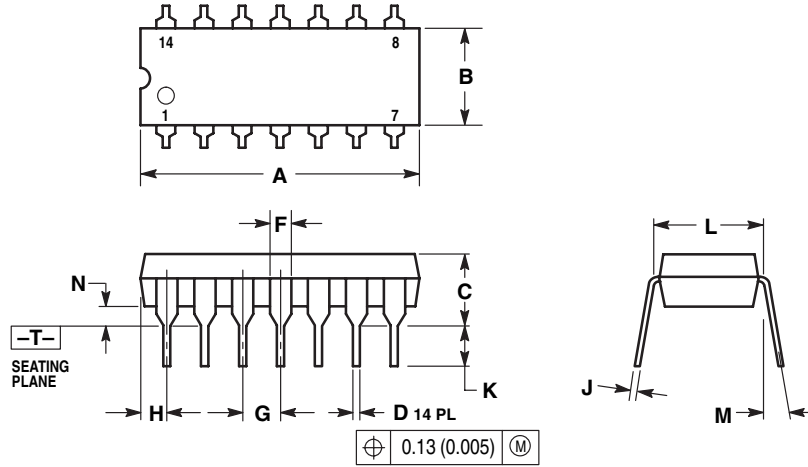


Figure 11b. Application Circuite Using ML12002 as a AM Modulator

OUTLINE DIMENSIONS

P DIP 14 = CP
 PLASTIC PACKAGE
 (ML12002CP)
 CASE 646-06
 ISSUE M

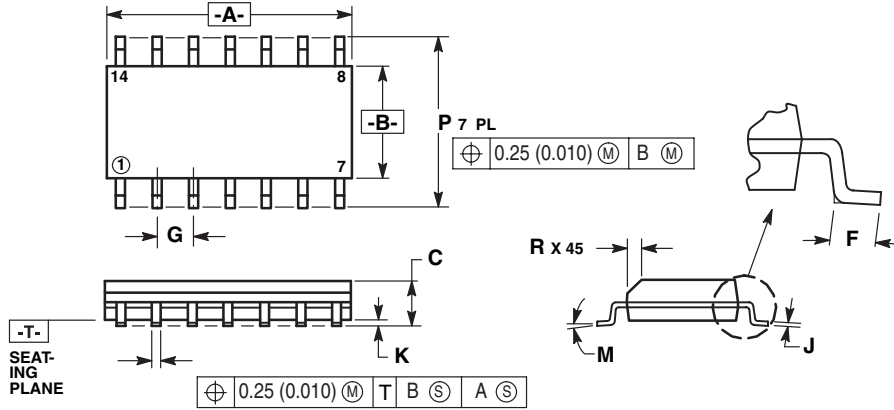


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	18.80
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	—		10°	
N	0.015	0.039	0.38	1.01

OUTLINE DIMENSIONS

SOG 14 = -5P
(ML12002-5P)
CASE 751A-03



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION
4. MAXIMUM HOLD PROTRUSION 0.15 (0.006) PER SIDE
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.334
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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