

## 5-TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

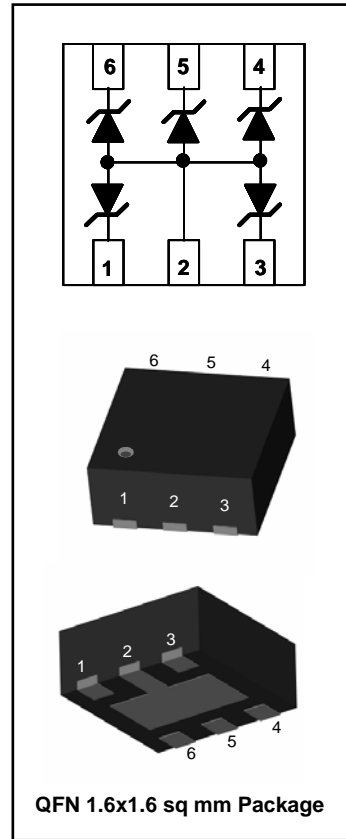
This 5-TVS array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry, operating at 3.3V and 5V Systems. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.

### SPECIFICATION FEATURES

- 15W Power Dissipation (8/20 $\mu$ s Waveform)
- Low Leakage Current, Maximum of 0.5 $\mu$ A @  $V_{WRM}$
- Very low Off-State Capacitance, Maximum of 10pF at 1MHz 0Vdc
- IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance
- 100% Tin plated finish (LEAD FREE) RoHS Compliant
- New SMT package QFN 1.6mm x 1.6mm; Max Height of 0.75mm
- Same Footprint compared to the SOT563

### APPLICATIONS

- Personal Digital Assistant (PDA)
- MP3 Players
- Portable Global positioning Systems Port
- Mobile Phones and Accessories
- Memory Card Port Protection



### MAXIMUM RATINGS (Per Device)

Rating	Symbol	Value	Units
Peak Pulse Power (8/20 $\mu$ s Waveform)	$P_{pp}$	15	W
ESD Voltage (HBM)	$V_{ESD}$	>25	kV
Operating Temperature Range	$T_J$	-55 to +150	$^{\circ}$ C
Storage Temperature Range	$T_{stg}$	-55 to +150	$^{\circ}$ V

### ELECTRICAL CHARACTERISTICS (Per Device) $T_J = 25^{\circ}$ C

### PJESD5V6LCQ5G

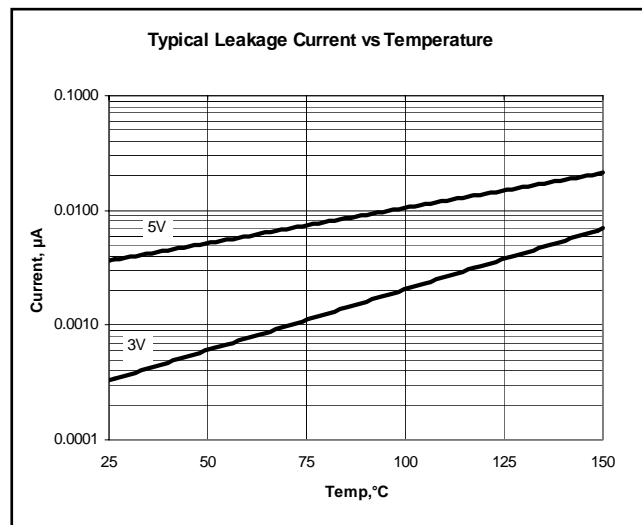
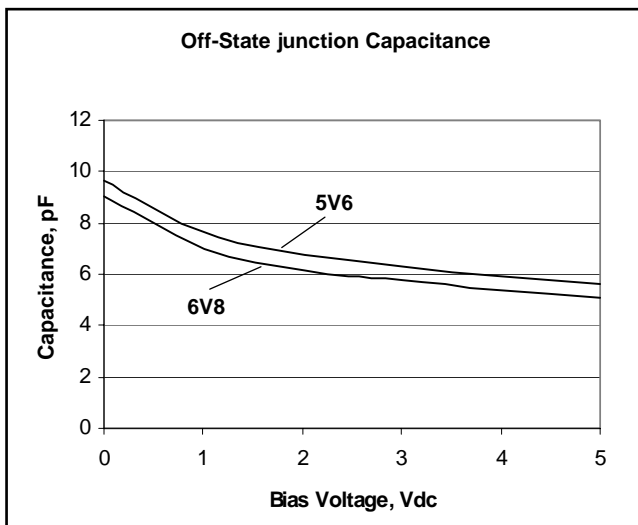
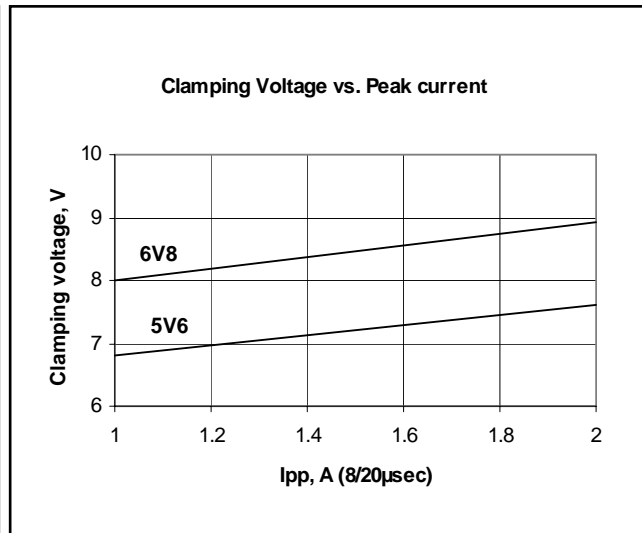
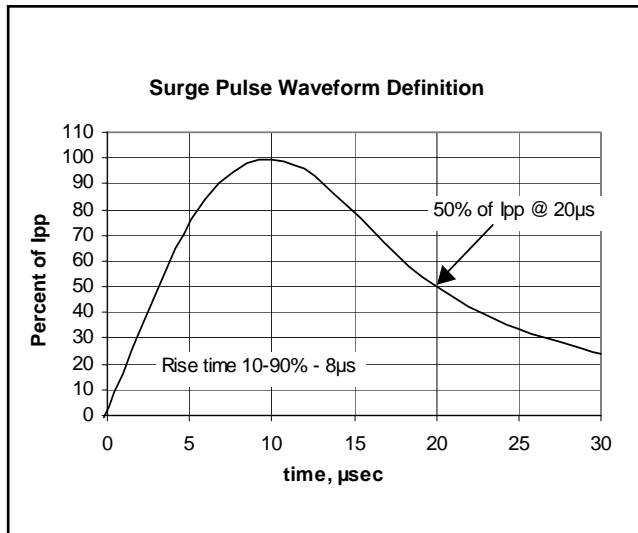
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				3.3	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	5.3	5.6	5.88	V
Reverse Leakage Current	$I_R$	$V_R = 3.3\text{V}$			0.5	$\mu$ A
Clamping Voltage (8/20 $\mu$ s)	$V_C$	$I_{pp} = 1\text{A}$			7.0	V
Clamping Voltage (8/20 $\mu$ s)	$V_C$	$I_{pp} = 2\text{A}$			8.0	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2		9.6	10	pF
Off State Junction Capacitance	$C_j$	3.3 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 2		6.2	8	pF

**ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C**

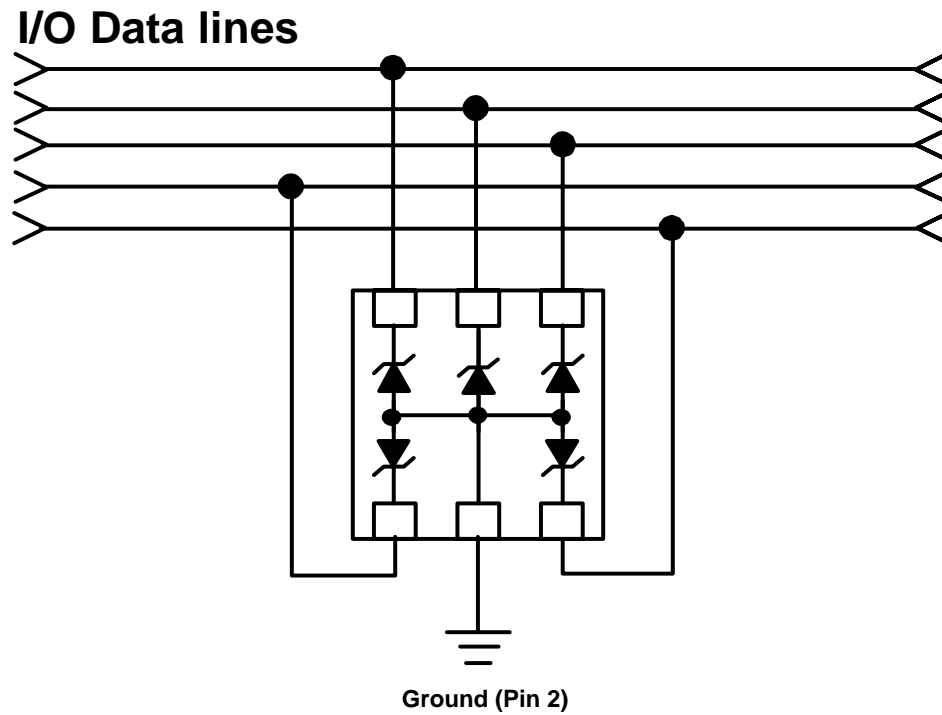
**PJESD6V8LCQ5G**

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				5.0	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1mA$	6.2	6.8	7.2	V
Reverse Leakage Current	$I_R$	$V_R = 5.0V$			0.5	$\mu A$
Clamping Voltage (8/20 $\mu s$ )	$V_c$	$I_{pp} = 1 A$			9	V
Clamping Voltage (8/20 $\mu s$ )	$V_c$	$I_{pp} = 2 A$			10	V
Off State Junction Capacitance	$C_j$	0 Vdc Bias f = 1MHz Between I/O pins and pin 2		9.1	10	pF
Off State Junction Capacitance	$C_j$	5 Vdc Bias f = 1MHz Between I/O pins and pin 2		5.0	6	pF

**TYPICAL CHARACTERISTICS 25°C unless otherwise noted**



**TYPICAL APPLICATION EXAMPLE**



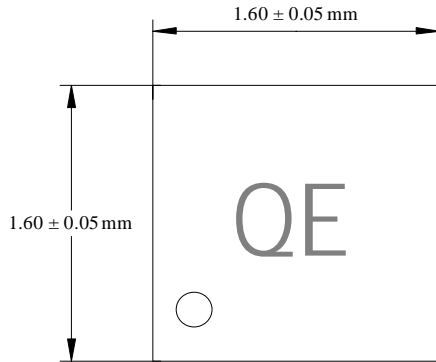
**Marking Code Information**

Device	Marking Code
PJESD5V6LCQ5G	QE
PJESD6V8LCQ5G	QG

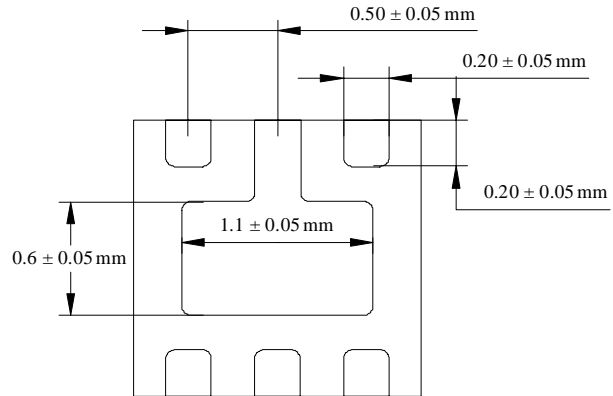


PACKAGE DIMENSIONS AND SUGGESTED BOND PAD LAYOUT

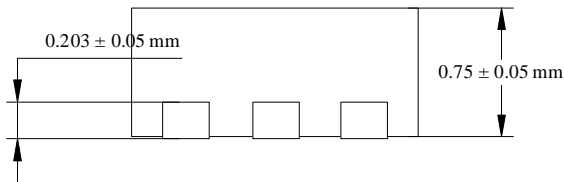
TOP VIEW



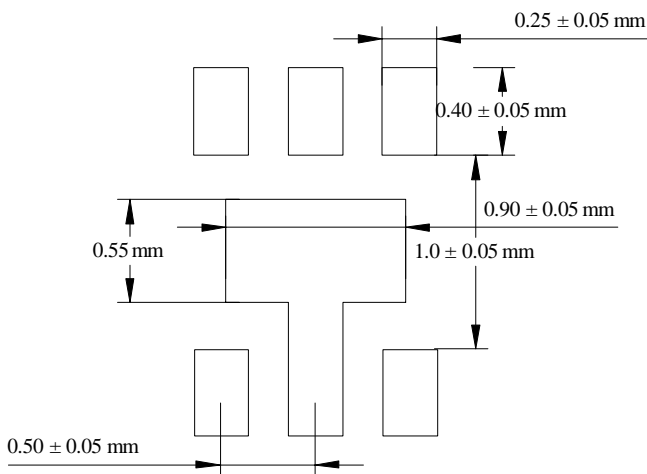
BOTTOM VIEW



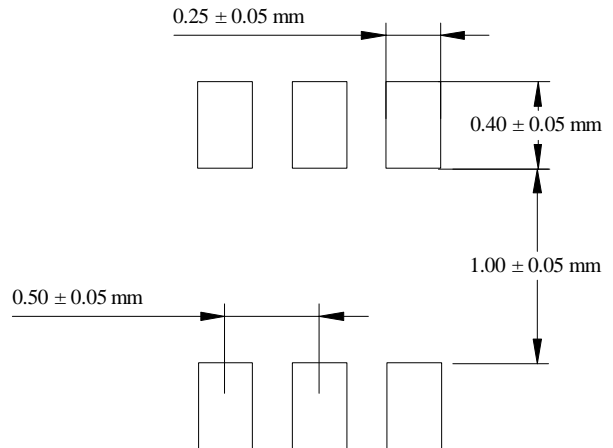
SIDE VIEW



PREFERRED



ALTERNATE



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