



Dual N-Channel 100-V (D-S) MOSFET

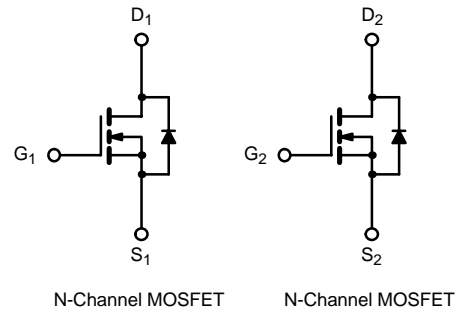
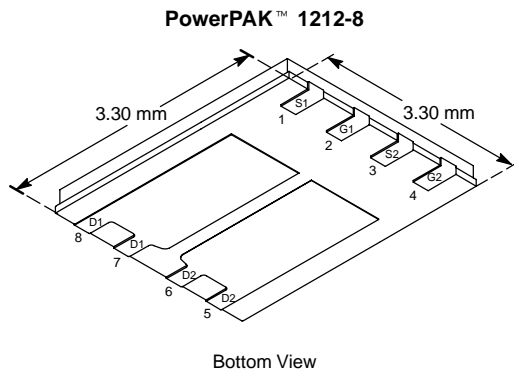
PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
100	0.195 @ V _{GS} = 10 V	2.5
	0.230 @ V _{GS} = 6 V	2.3

FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package, 1/3 the Space of An SO-8 While Thermally Comparable
- PWM Optimized

APPLICATIONS

- DC/DC Primary-Side Switch
- 48-V Battery Monitoring



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	100		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	2.5	1.8	A
		T _A = 85 °C	1.8	1.3	
Pulsed Drain Current	I _{DM}	10			
Avalanche Current	I _{AS}	5			
Single Avalanche Energy	E _{AS}	1.25		mJ	
Continuous Source Current (Diode Conduction) ^a	I _S	2.2	1.1	A	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.6	1.3	W
		T _A = 85 °C	1.4	0.69	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	38	48	°C/W
		Steady State	77	94	
Maximum Junction-to-Case (Drain)	R _{thJC}	4.3	5.4		

Notes

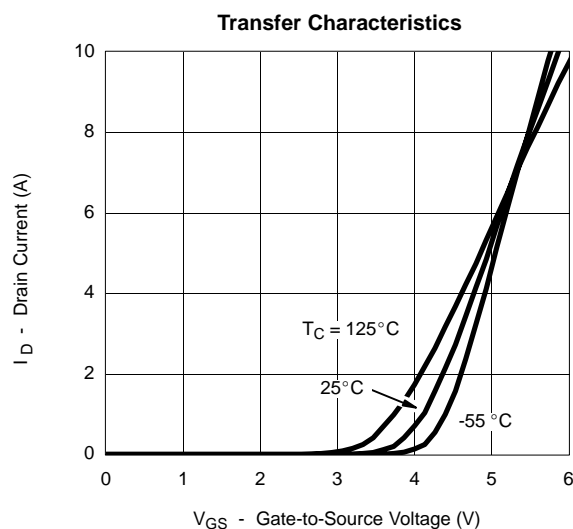
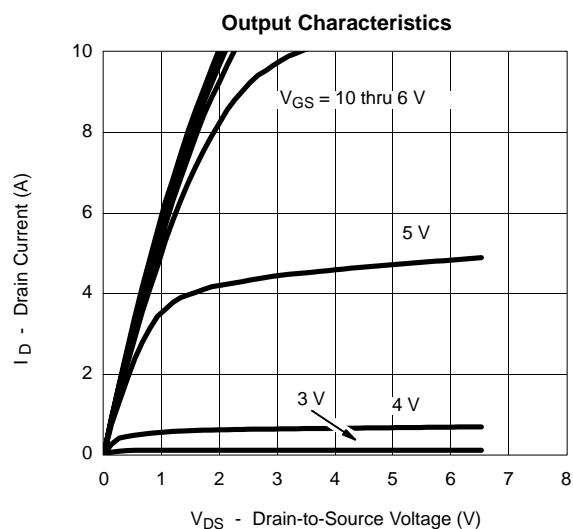
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 85 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	10			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 2.5 A		0.162	0.195	Ω
		V _{GS} = 6 V, I _D = 2.3 A		0.190	0.230	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 2.5 A		5.3		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.2 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 2.5 A		5.2	8	nC
Gate-Source Charge	Q _{gs}			1.1		
Gate-Drain Charge	Q _{gd}			1.9		
Gate Resistance	R _G			1.7		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _G = 6 Ω		7	15	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			8	15	
Fall Time	t _f			11	20	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 2.2 A, di/dt = 100 A/μs		40	80	

Notes

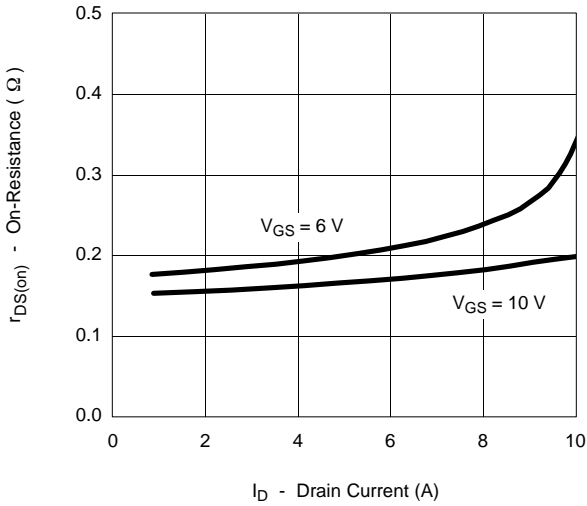
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

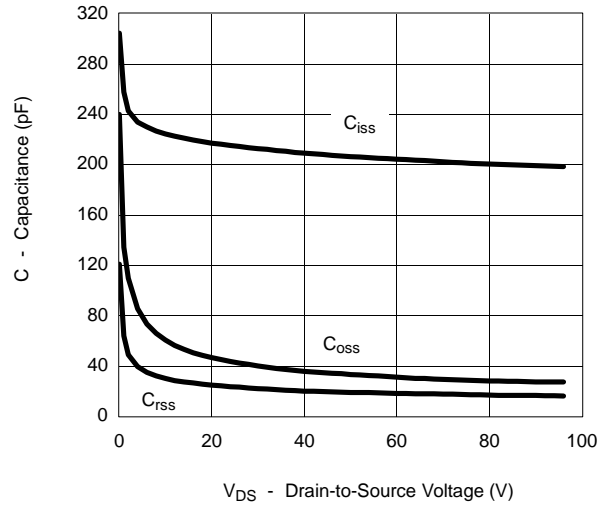


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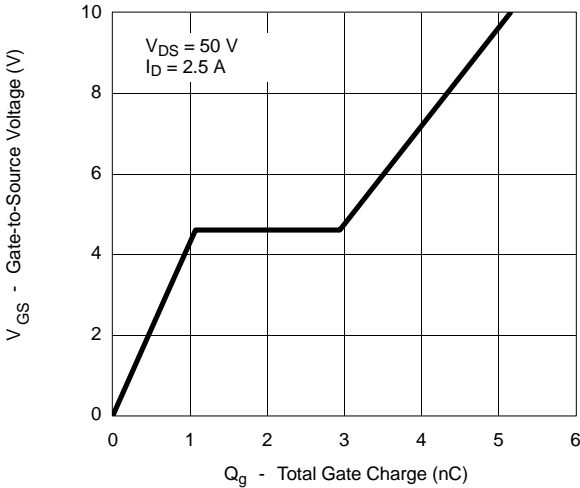
On-Resistance vs. Drain Current



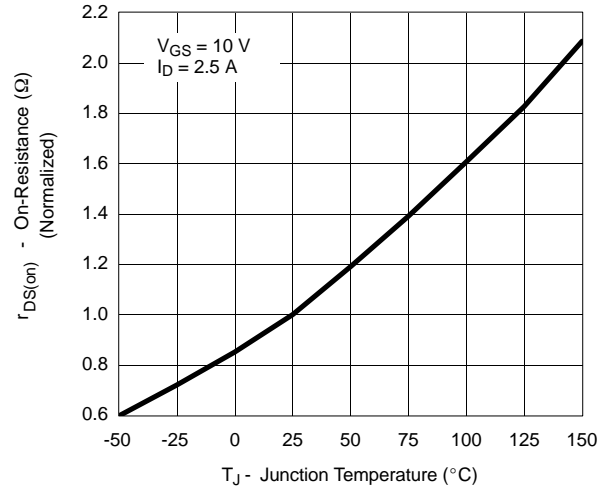
Capacitance



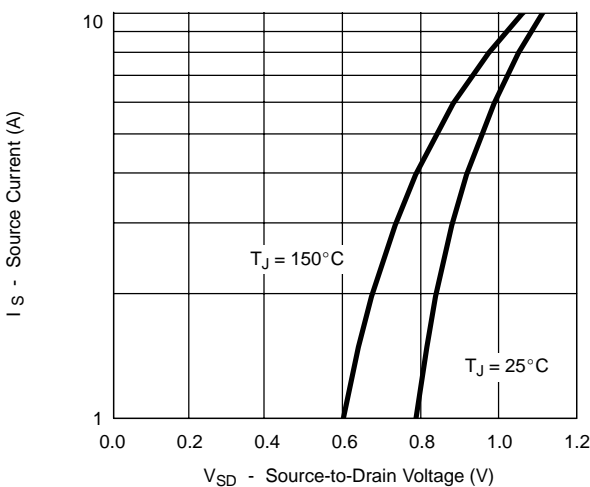
Gate Charge



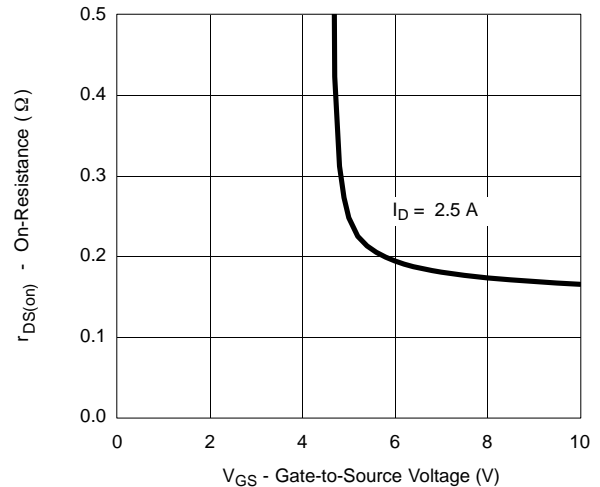
On-Resistance vs. Junction Temperature



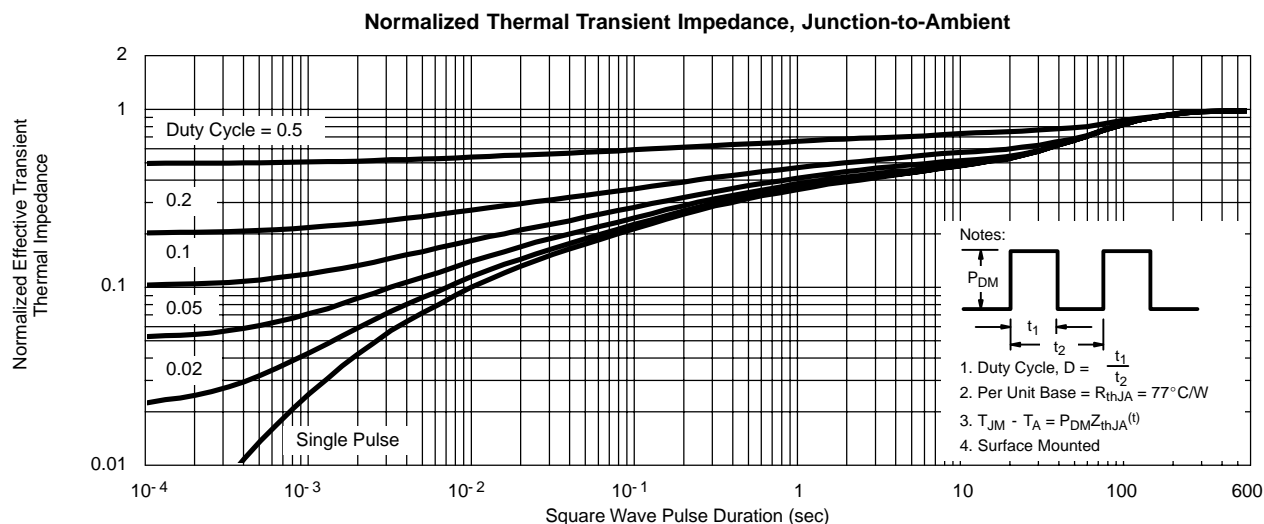
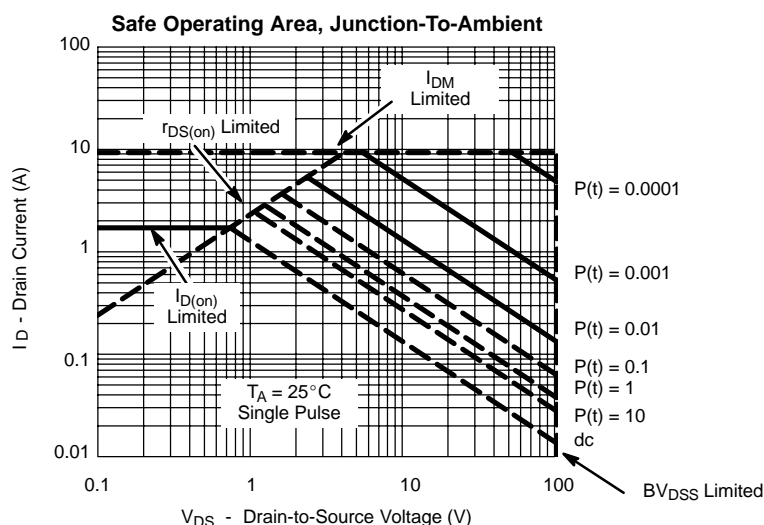
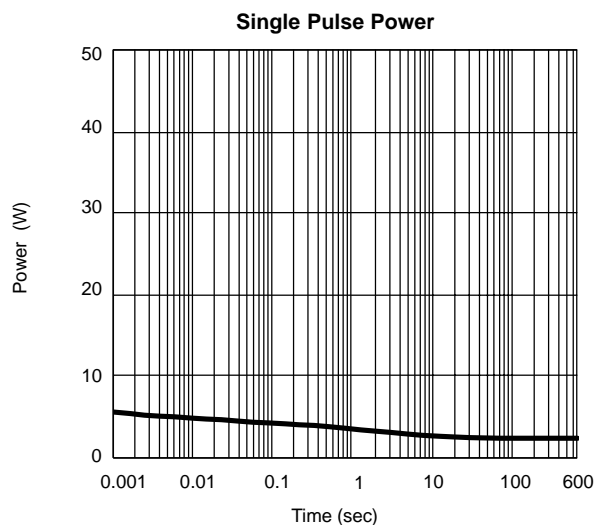
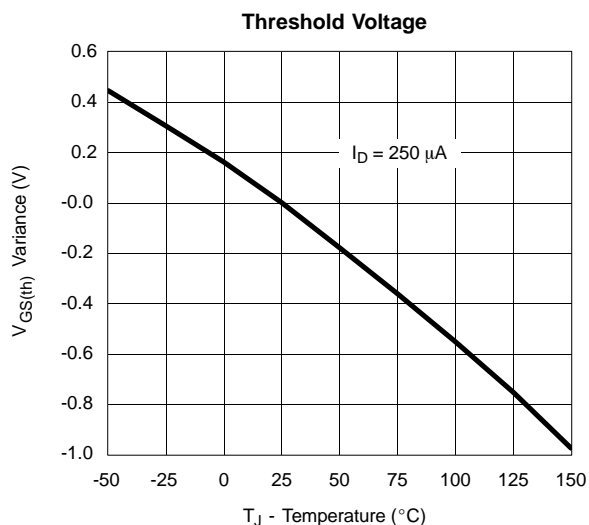
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

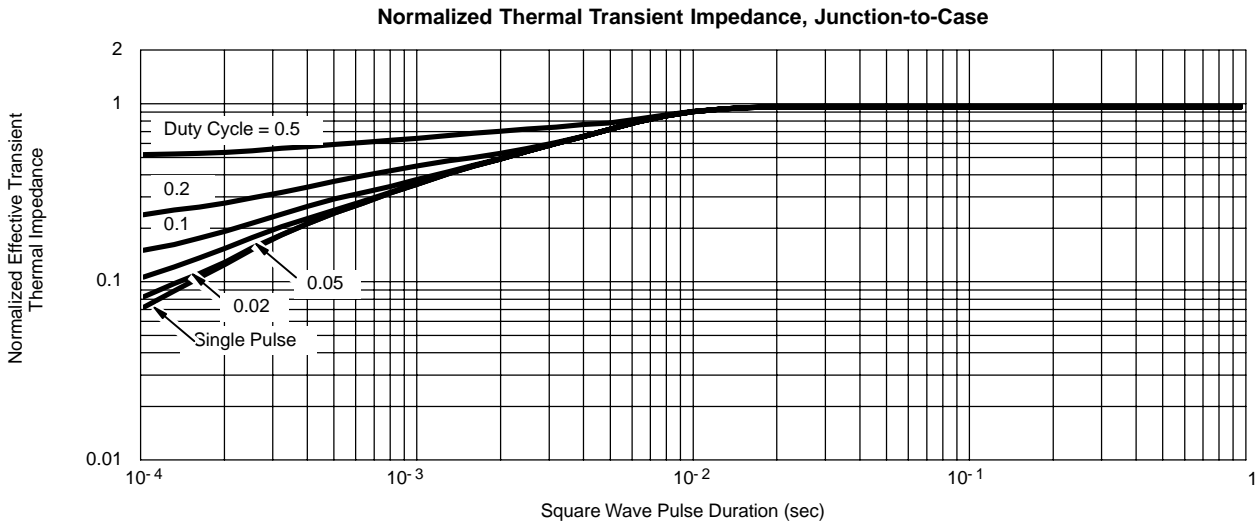


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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NOTE:

The minimum creepage between D1 and D2 for this 100-V device is 0.2 mm. Please see PowerPAK 1212-8 outline drawing, document # 71656, for more information.