8-bit MCU with Embedded EEPROM

1. Features

- Compatible with MCS-51
- Embedded 8K Bytes OTP ROM
- Embedded 1k bits EEPROM
- 256 x 8-bit Internal RAM
- 15 Programmable I/O Lines
- 2 16-bit Timer/Counter & 1 16-bit Timer
- 2 External Interrupt Input
- Programmable Serial UART Interface
- Low Power Idle & Power-down Modes
- Watch-dog Timer
- On-chip Crystal & RC Oscillator (Selected by Bonding Option)
- Internal Power-on Reset and External Reset Supported
- 32-pin LQFP Package
- 3.3V Operating Voltage

2. General Description

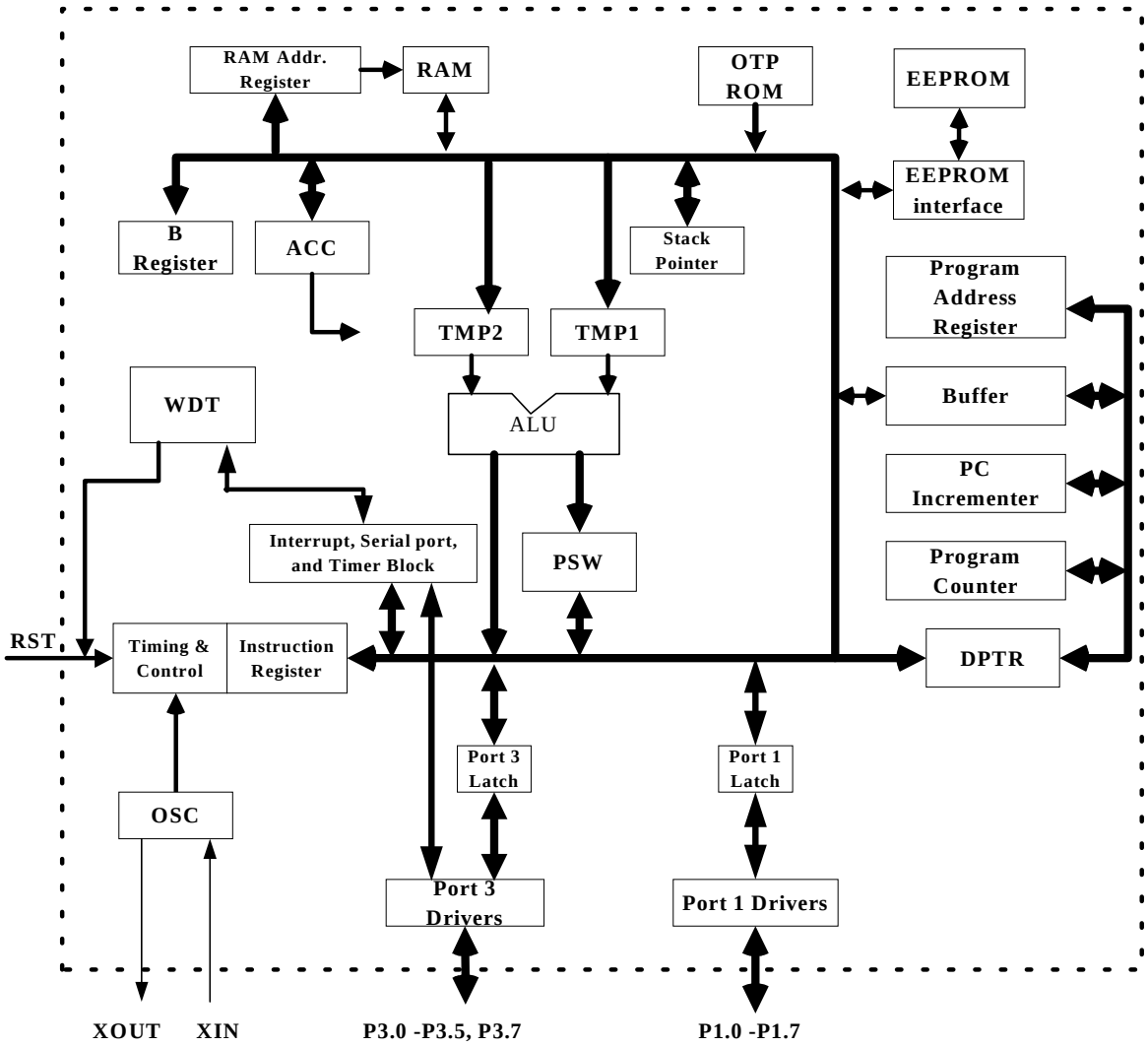
The T81L0010B is 8-bit microcontroller designed and developed with low power and high speed CMOS technology. It contains a 8K bytes OTP ROM, a 256 × 8 RAM, 1k bits EEPROM, 15 I/O lines, a watchdog timer, two 16-bit counter/timers, a seven source, two-priority level nested interrupt structure, a full duplex UART, and an on-chip oscillator and clock circuits.

In addition, the T81L0010B has two selectable modes of power reduction-idle mode and power-down mode. The idle mode freezes the CPU while allowing the RAM, timers, serial port, and interrupt system to continue functioning. The power-down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

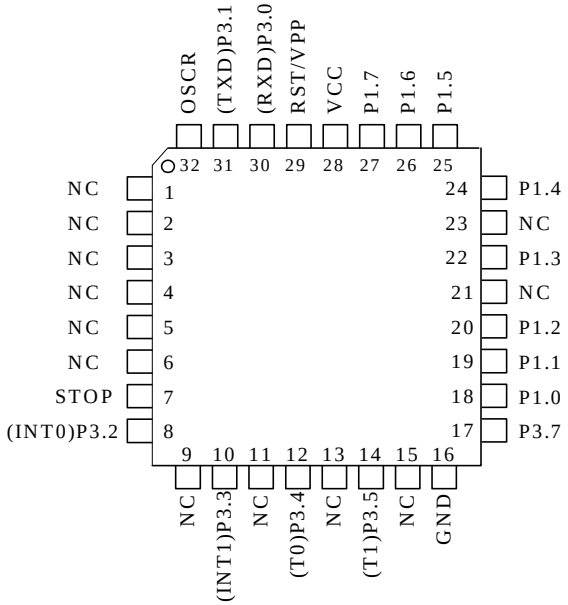
3. Order Information

Part number	Oscillator type	Package
T81L0010B-AL	RC	32-pin LQFP
T81L0010B-BL	Crystal	32-pin LQFP

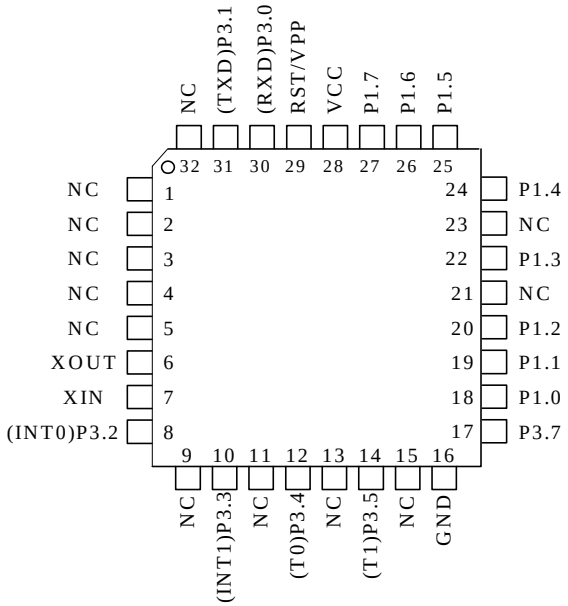
4. Block Diagram



5. Pin Configuration



LQFP-32 For RC Oscillator
T81L0010B-AL



LQFP-32 For Crystal Oscillator
T81L0010B-BL

6. Pin Description

Number (32-Pin)	Name	Type	Description
1	NC		No connect
2	NC		No connect
3	NC		No connect
4	NC		No connect
5	NC		No connect
6(AL)	NC		No connect
6(BL)	XOUT	I	Crystal oscillator output terminal.
7(AL)	STOP	O	Stop RC oscillator network.
7(BL)	XIN	O	Crystal oscillator input terminal.
8	P3.2/(INT0)	I/O	General-purpose I/O pin (Default) or External interrupt source 0.
9	NC		No connect
10	P3.3/(INT1)	I/O	General-purpose I/O pin (Default) or External interrupt source 1.
11	NC		No connect
12	P3.4/(T0)	I/O	General-purpose I/O pin (Default) or Timer 0 external input pin.
13	NC		No connect
14	P3.5/(T1)	I/O	General-purpose I/O pin (Default) or Timer 1 external input pin.
15	NC		No connect
16	GND		Ground
17	P3.7	I/O	General-purpose I/O pin
18	P1.0	I/O	General-purpose I/O pin
19	P1.1	I/O	General-purpose I/O pin
20	P1.2	I/O	General-purpose I/O pin
21	NC		No connect
22	P1.3	I/O	General-purpose I/O pin
23	NC		No connect
24	P1.4	I/O	General-purpose I/O pin
25	P1.5	I/O	General-purpose I/O pin
26	P1.6	I/O	General-purpose I/O pin
27	P1.7	I/O	General-purpose I/O pin
28	VCC		3.3V power supply.
29	RST/VPP	I	Reset signal input or programming supply voltage input.
30	P3.0/(RXD)	I/O	General-purpose I/O pin (Default) or Serial input port.
31	P3.1/(TXD)	I/O	General-purpose I/O pin (Default) or Serial output port.
32(AL)	OSCR	I	RC oscillator external resister connect pin.
32(BL)	NC		No connect

7. Temperature Limit Ratings

Parameter	Rating	Units
Operating temperature Range	-40 to +85	°C
Storage Temperature Range	-55 to +125	°C

8. Electrical Characteristics

D.C Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
VCC	Operating Voltage	25°C		3.0	3.3	3.6	V
ICC	Operating Current	No load, Vcc=2.5V, 4MHz		-	-	1.6	mA
		No load, Vcc=3.3V, 12MHz		-	-	6	mA
IPD	Power Down Current	Vcc=3.3V		-	0.1	1	uA
V_{IH}	Hi-Level input voltage	V_{out} >=$V_{VOH(MIN.)}$ V_{out} <=$V_{VOL(MIN.)}$		2.1	-	-	V
V_{IL}	Low-Level input voltage	V_{out} >=$V_{VOH(MIN.)}$ V_{out} <=$V_{VOL(MIN.)}$		-	-	0.6	V
V_{OH}	Hi-Level Output voltage	V_{CC}=MIN. V_I=V_{IH} or V_{IL}	I_{OH}=-7uA	2.9	-	-	V
			I_{OH}=-45uA	2.4			
			I_{OH}=-70uA	1.9			
V_{OL}	Low-Level Output voltage	V_{CC}=MIN. V_I=V_{IH} or V_{IL}	I_{OL}=12mA	-	-	0.2	V
			I_{OL}=25mA			0.4	
			I_{OL}=40mA			0.6	

A.C Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FSYS1	System Clock 1 (Crystal OSC)	VCC=3.3V	-	12	24	MHz
FSYS2	System Clock 2 (RC OSC)	VCC=3.3V	-	12	-	MHz
tRES	External Reset High Pulse Width		-	10	-	system cycle
	Power ON Start up Time		-	20	-	ms

9. Function Description

9.1. Special Function Register

F8H								
F0H	B							
E8H								
E0H	ACC							
D8H								
D0H	PSW							
C8H	T2CON	T2MOD			TL2	TH2		
C0H								
B8H	IP							
B0H	P3							
A8H	IE							
A0H	P2							
98H	SCON	SBUF						
90H	P1							
88H	TCON	TMOD	TL0	TL1	TH0	TH1		
80H	P0*	SP	DPL	DPH				PCON

***Note: P0:Internal still keeping, but for pad dominate, no external pin assignment**

Accumulator : ACC

ACC is the Accumulator register. The mnemonics for Accumulator-Specific instructions, however, refer to the Accumulator simply as A.

B Register : B

The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

Program Status Word : PSW

The PSW register contains program status information as detailed in

CY	AC	F0	RS1	RS0	OV	--	P

BIT SYMBOL FUNCTION

PSW.7 CY Carry flag.
PSW.6 AC Auxiliary Carry flag. (For BCD operations.)
PSW.5 F0 Flag 0. (Available to the user for general purposes.)
PSW.4 RS1 Register bank select control bit 1.
Set/cleared by software to determine working register bank. (See **Note.**)
PSW.3 RS0 Register bank select control bit 0.
Set/cleared by software to determine working register bank. (See **Note.**)
PSW.2 OV Overflow flag.
PSW.1 — User-definable flag.
PSW.0 P Parity flag.
Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the Accumulator, i.e., even parity.

NOTE: The contents of (RS1, RS0) enable the working register banks as follows:
(0,0)— Bank 0 (00H–07H)
(0,1)— Bank 1 (08H–0fH)
(1,0)— Bank 2 (10H–17H)
(1,1)— Bank 3 (18H–17H)

Stack Pointer : SP

The Stack Pointer register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in on-chip RAM, the Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at locations 08H.

Data Pointer (DPTR) : DPH & DPL

The Data Pointer (DPTR) consists of a high byte (DPH) and a low byte (DPL). Its intended function is to hold a 16-bit address. It may be manipulated as a 16-bit register or as two independent 8-bit registers.

Ports 1.0~1.7 & 3.0~3.5 & 3.7

All Ports are the SFR latches, respectively. Writing a one to a bit of a port SFR (P1 or P3) causes the corresponding port output pin to switch high. Writing a zero causes the port output pin to switch low. When used as an input, the external state of a port pin will be held in the port SFR (i.e., if the external state of a pin is low, the corresponding port SFR bit will contain a '0'; if it is high, the bit will contain a '1').

Serial Data Buffer : SBUF

The Serial Buffer is actually two separate registers, a transmit buffer and a receive buffer. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. (Moving a byte to SBUF is what initiates the transmission.) When data is moved from SBUF, it comes from the receive buffer.

Timer Registers : TH0, TL0, TH1, TL1,TH2,TL2

Register pairs (TH0, TL0) and (TH1, TL1) and (TH2, TL2) are 16-bit Counting registers for Timer/Counters 0 and Timer1and Timer2, respectively.

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Control Register : IP, IE, TMOD, TCON, SCON, PCON

Special Function Registers IP, IE, TMOD, TCON, SCON, and PCON contain control and status bits for the interrupt system, the Timer/Counters, and the serial port. They are described in later sections.

Standard Serial Interface

The serial port is full duplex, meaning it can transmit and receive simultaneously. It is also receive-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. (However, if the first byte still hasn't been read by the time reception of the second byte is complete, one of the bytes will be lost.) The serial port receive and transmit registers are both accessed at Special Function Register SBUF. Writing to SBUF loads the transmit register, and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

Mode 0: Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency.

Mode 1: 10 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), and a stop bit (1). On receive, the stop bit goes into RB8 in Special Function Register SCON. The baud rate is variable.

Mode 2: 11 bits are transmitted (through TxD) or received (through RxD): start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). On Transmit, the 9th data bit (TB8 in SCON) can be assigned the value of 0 or 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. On receive, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3: 11 bits are transmitted (through TxD) or received (through RxD): a start bit (0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable. In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = '0' and REN = '1'. Reception is initiated in the other modes by the incoming start bit if REN = '1'.

Multiprocessor Communications

Modes 2 and 3 have a special provision for multiprocessor communications. In these modes, 9 data bits are received. The 9th one goes into RB8. Then comes a stop bit. The port can be programmed such that when the stop bit is received, the serial port interrupt will be activated only if RB8 = '1'. This feature is enabled by setting bit SM2 in SCON. A way to use this feature in multiprocessor systems is as follows: When the master processor wants to transmit a block of data to one of several slaves, it first sends out an address byte which identifies the target slave. An address byte differs from a data byte in that the 9th bit is '1' in an address byte and '0' in a data byte. With SM2 = '1', no slave will be interrupted by a data byte. An address byte, however, will interrupt all slaves, so that each slave can examine the received byte and see if it is being addressed. The addressed slave will clear its SM2 bit and prepare to receive the data bytes that will be coming. The slaves that weren't being addressed leave their SM2s set and go on about their business, ignoring the coming data bytes.

SM2 has no effect in Mode 0, in Mode 1 can be used to check the validity of the stop bit. In Mode 1 reception, if SM2 = '1', the receive interrupt will not active unless a valid stop bit is received.

Serial Port Control Register

The serial port control and status register is the Special Function Register SCON, shown in Figure 11. This register contains not only the mode selection bits, but also the 9th data bit for transmit and receive (TB8 and RB8), and the serial port interrupt bits (TI and RI).

Baud Rates

The baud rate in Mode 0 is fixed: Mode 0 Baud Rate = Oscillator Frequency / 12. The baud rate in Mode 2 depends on the value of bit SMOD in Special Function Register PCON. If SMOD = '0' (which is the value on reset), the baud rate is 1/64 the oscillator frequency. If SMOD = '1', the baud rate is 1/32 the oscillator frequency.

Mode 2 Baud Rate =2^{SMOD}/64* (Oscillator Frequency)

In the T81L0010B, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate.

Using Timer 1 to Generate Baud Rates

When Timer 1 is used as the baud rate generator, the baud rates in Modes 1 and 3 are determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 Baud Rate =2^{SMOD}/32* (Timer 1 Overflow Rate)

The Timer 1 interrupt should be disabled in this application. The Timer 1 itself can be configured for either "timer" or "counter" operation, and in any of its 3 running modes. In the most typical applications, it is configured for "timer" operation, in the auto-reload mode (high nibble of TMOD = 0010B). In that case the baud rate is given by the formula:

Mode 1, 3 Baud Rate =2^{SMOD}*(Oscillator Frequency)/ 32/12 / [256 _ (TH1)]

One can achieve very low baud rates with Timer 1 by leaving the Timer 1 interrupt enabled, and configuring the Timer to run as a 16-bit timer (high nibble of TMOD = 0001B), and using the Timer 1 interrupt to do a 16-bit software reload.

MSB **LSB**

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Where SM0, SM1 specify the serial port mode, as follows:

SM0	SM1	Mode	Description	Baud Rate
0	**0**	**0**	shift register	f_{OSC} / 12
0	**1**	**1**	8-bit UART	Variable
1	**0**	**2**	9-bit UART	UART F_{OSC} /64 or F_{OSC} /32
1	**1**	**3**	9-bit UART	Variable

Interrupt Enable Register : IE

MSB **LSB**

EA	wdt	ET2	ES	ET1	EX1	ET0	EX0

EA IE.7 Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

wdt IE.6 Watchdog timer refresh flag.

ET2 IE.5 Enable or disable the Timer 2 overflow interrupt.

ES IE.4 Enable or disable the serial port interrupt.

ET1 IE.3 Enable or disable the Timer 1 overflow interrupt.

EX1 IE.2 Enable or disable External Interrupt 1.

ET0 IE.1 Enable or disable the Timer 0 overflow interrupt.

EX0 IE.0 Enable or disable External Interrupt 0.

9.2. External Register Table (for LVR, EEPROM, High/ Normal Driving)

Register Address		Name	Comments
A15…A5-A0	Hex		
100… 0010 1011	802bH	PWMC2	LVR (Low Voltage Reset)*
100… 0011 0000	8030H	Port3 HDS	Port3 I/O high driving set**
100… 0011 0010	8032H	Port1 HDS	Port1 I/O high driving set**
100… 00101000	8028H	SPICON	EEPROM control & setup
100… 0010 1001	8029H	OPCODE	EEPROM opcode
100… 0010 1110	802eH	DATAW_H	EEPROM write high byte
100… 0010 1111	802fH	DATAW_L	EEPROM write low byte
100… 0010 1100	802cH	DATAR_H	EEPROM read high byte
100… 0010 1101	802dH	DATAR_L	EEPROM read low byte

Note :

***** LVR (Low Voltage Reset) address : 802bH, read/write

MSB **LSB**

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
LVR[7]	LVR[6]	Reserved					

LVR[7] : if LVR[7] write '1', low voltage reset function enable.
default is '0', low voltage reset function disable.

LVR[6] : if LVR[6] write '1'= 2.1V reset. if LVR[6] write '0'= 2.8V reset.
default is '0'= 2.8V reset.

** Port I/O high driving set
if write '0' = set I/O to high driving current mode.
if write '1' = set I/O to normal driving current mode.
default is set '1'.

Port 3 high driving address : 8030H

MSB **LSB**

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Port3.7		Port3.5	Port3.4	Port3.3	Port3.2	Port3.1	Port3.0

Port 1 high driving address : 8032H

MSB **LSB**

Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
Port1.7	Port1.6	Port1.5	Port1.4	Port1.3	Port1.2	Port1.1	Port1.0

9.3. EEPROM Interface

The EEPROM interface timing is fully compatible with 93C46. To access or send data from/to T81L0010B , 6 registers are going to be controlled.

EEPROM Register Control

SPICON	Default	--	--	--	--	--	B2: R/W	B1: R/W	B0: R/W
	00H	--	--	--	--	--	Epdiv1	Epdiv0	Epst
OPCODE									W
	00H	-	-	-	-	-	-	-	
DATAW_H									
DATAW_L	00H								
DATAR_H									
DATAW_L	00H								

SPICON:

MSB							**LSB**
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
					Epdiv1	Epdiv0	Epst

Epst: start EEPROM timing. “1” to start and will be auto cleared after timing finish.
Epdiv[1..0]: divide input clock into EEPROM system clock.
10: divide by 64
01: divide by 32
else: divide by 16

OPCODE

MSB							**LSB**
Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
OP Code		address					

Instruction Set	**OP Code**	**Address**	**Input Data**
Read	**10**	**A5-A0**	
WEN (Write Enable)	**00**	**11xxxx**	
Write	**01**	**A5-A0**	**D15-D0**
WRALL (Write All Registers)	**00**	**01xxxx**	**D15-D0**
WDS (Write Disable)	**00**	**00xxxx**	
Erase	**11**	**A5-A0**	
ERAL	**00**	**10xxxx**	

9.4. I/O Ports

Port1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. Port 1 output buffers can sink/source four external TTL device inputs. When port 1 pins are written as 1's, these pins are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. Port 3 output buffers can sink/source four external TTL device inputs. When port 3 pins are written as 1's, these pins are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current because of the internal pull-ups.

Port 3 also serves the functions of various special features, as listed below:

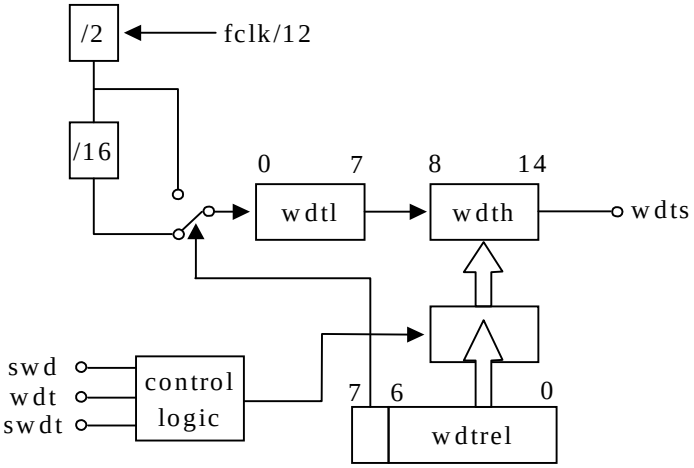
P3.0 RXD (serial input port)
P3.1 TXD (serial output port)
P3.2 INT0 (external interrupt 0)
P3.3 INT1 (external interrupt 1)
P3.4 T0 (timer 0 external input)
P3.5 T1 (timer 1 external input)
P3.7 General purpose I/O only

Watchdog Timer

The watchdog timer is a 16-bit counter that is incremented once every 24 or 384 clock cycles. After an external reset the watchdog timer is disabled and all registers are set to zeros.

Watchdog Timer structure

The watchdog consists of 16-bit counter wdt, reload register wdtrel, prescalers by 2 and by 16 and control logic.



Watchdog block diagram

Start procedure

There are two ways to start the watchdog. One method, called hardware automatic start, is based on examining the level of signal swd during active internal rst signal. When this condition is met, the watchdog will start running automatically with default settings (all registers set to zeros).When this criterion is not met during active internal rst signal, a programmer can start the watchdog later. It will occur when signal swd becomes active. Once the watchdog is started it cannot be stopped unless internal rst signal becomes active. When wdt registers enters the state 7CFFh , asynchronous wdts signal will become active. The signal wdts sets the bit 6 in ip0 register and requests reset state. The wdts is cleared either by rst signal or change of the state of the wdt timer.

Refreshing the watchdog timer

The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active. This requirement imposes obligation on the programmer to issue two followed instructions. The first instruction sets wdt and the second one swdt. The maximum allowed delay between settings of the wdt and swdt is 12 clock cycles. While this period has expired and swdt has not been set, wdt is automatically reset, otherwise the watchdog timer is reloaded with the content of the wdtrel register and wdt is automatically reset.

Special Function Registers

a) Interrupt Enable 0 register (ien0)

The ien0 register (address : A8)

MSB							LSB
eal	wdt	et2	es0	et1	ex1	et0	ex0

The ien0 bit functions

Bit	Symbol	Function
ien0.6	wdt	Watchdog timer refresh flag. Set to initiate a refresh of the watchdog timer. Must be set directly before swdt is set to prevent an unintentional refresh of the watchdog timer. The wdt is reset by hardware 12 instruction cycles after it has been set.

Note: other bits are not used to watchdog control

The ien0 bit functions

b) Interrupt Enable 1 register (ien1)

The ien1 register (Address : B8)

MSB							LSB
-	swdt	pt2	ps	pt1	px1	pt0	px0

The ien1 bit functions

Bit	Symbol	Function
Ien1.6	swdt	Watchdog timer start refresh flag. Set to active/refresh the watchdog timer. When directly set after setting wdt, a watchdog timer refresh is performed. Bit swdt is reset by hardware 12 instruction cycles after it has been set.

Pay attention that when write ien1.6, it write the swdt bit, when read ien1.6, we will read out the wdts bit. Ie. Watch dog timer status flag. Set by hardware when the watchdog timer was started.

C) Watchdog Timer Reload register (wdtrel)

The wdtrel register (Address : 86)

MSB							LSB
7	6	5	4	3	2	1	0

The wdtrel bit functions

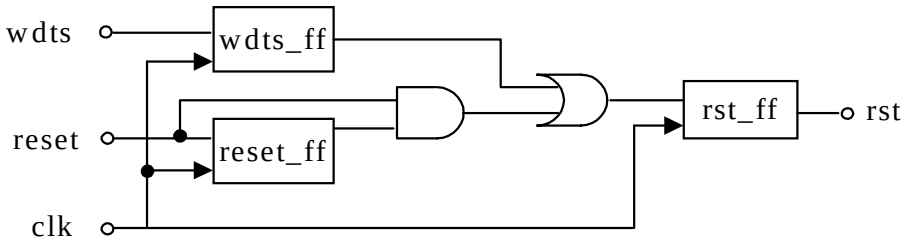
Bit	Symbol	Function
wdtrel.7	7	Prescaler select bit. When set, the watchdog is clocked through an additional divide-by-16 prescaler
wdtrel.6 t0 wdtrel.0	6-0	Seven bit reload value for the high-byte of the watchdog timer. This value is loaded to the wdt when a refresh is triggered by a consecutive setting of bits wdt and swdt

The wdtrel register can be loaded and read any time

WDT Reset

A high on reset pin or watchdog reset request for two clock cycles while the oscillator is running resets the device.

Diagram



Reset timing

a) External hardware reset

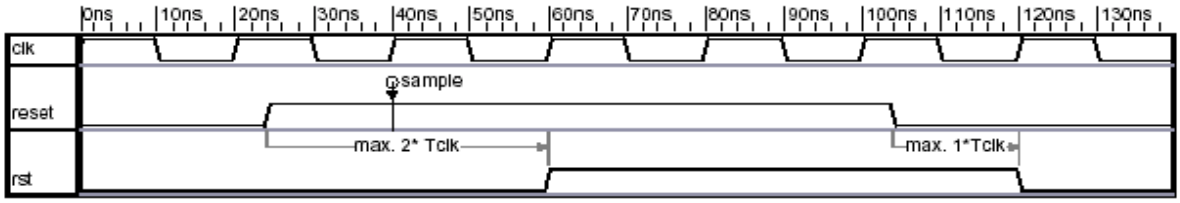


Figure External reset timing

**Note:
clk: external clock input
Tclk: clock period
reset: external reset input
rst: internally generated reset signal

b) Watchdog timer reset

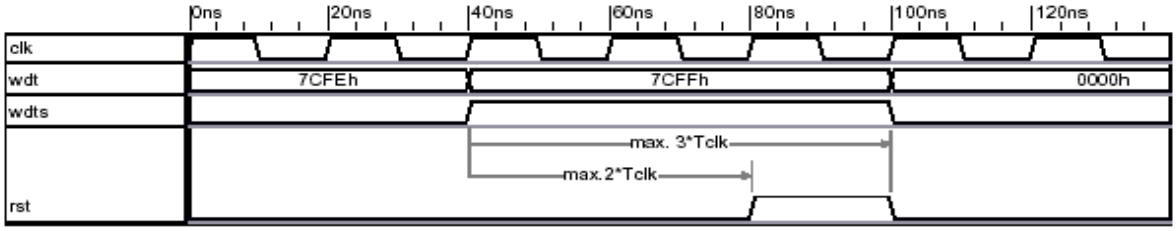
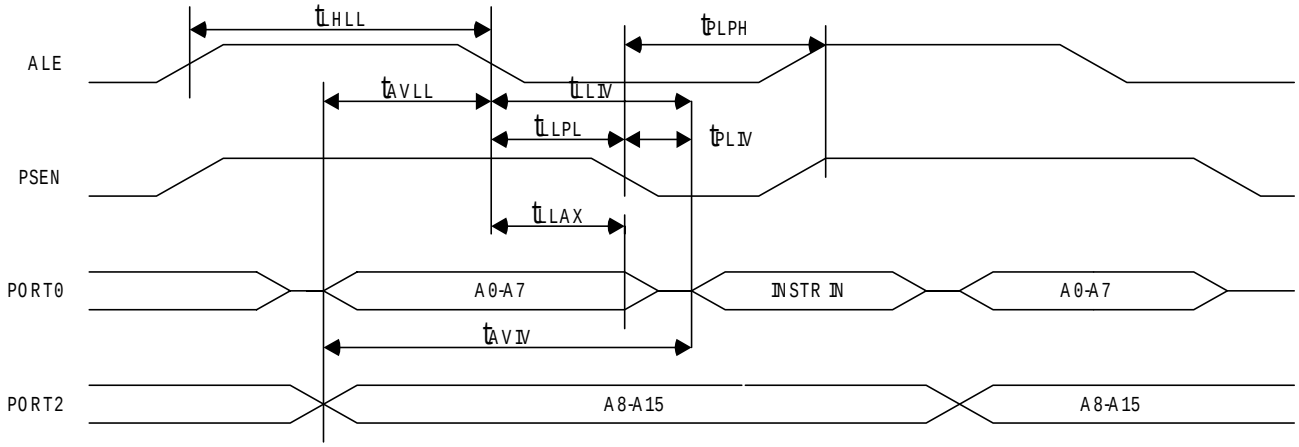


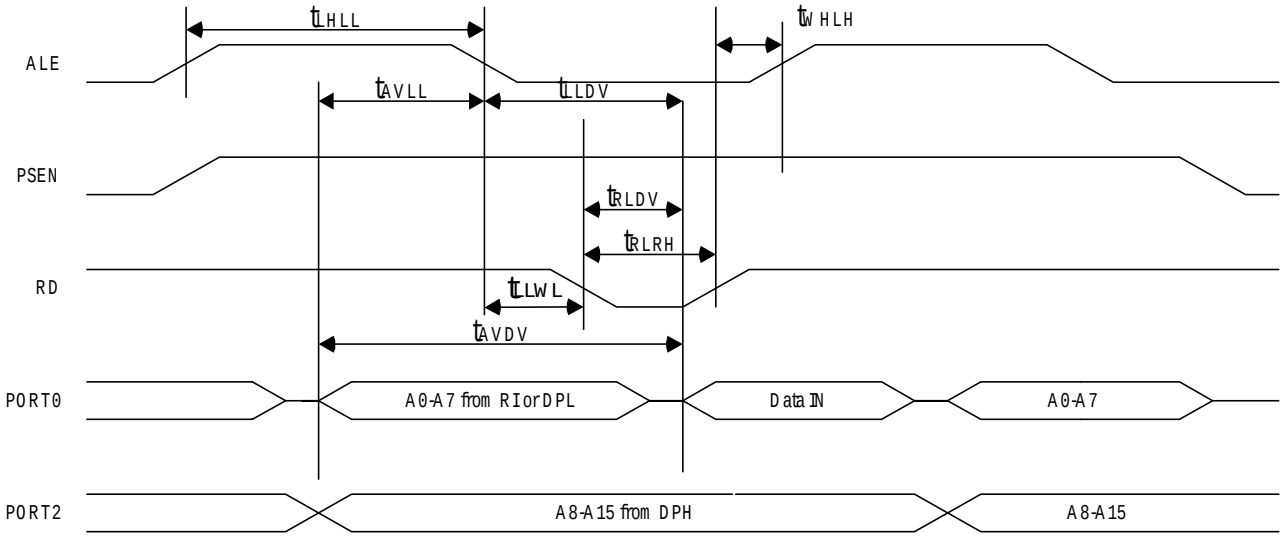
Figure Watchdog reset timing

**Note:
clk: external clock input
Tclk: clock period
wdt: watchdog timer registers
wdts: watchdog timer status flag
reset: external reset input
rst: internally generated reset signal

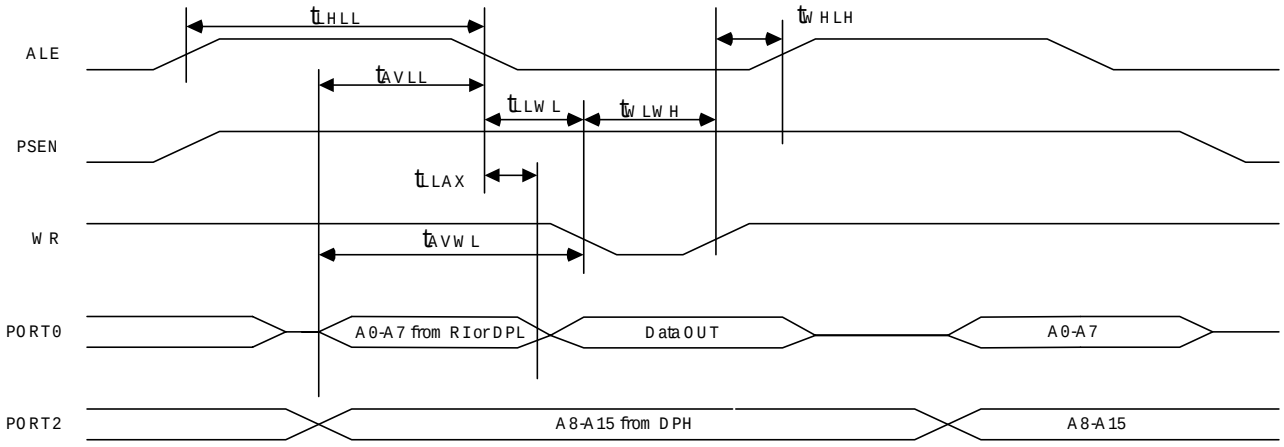
10. Timing Diagram



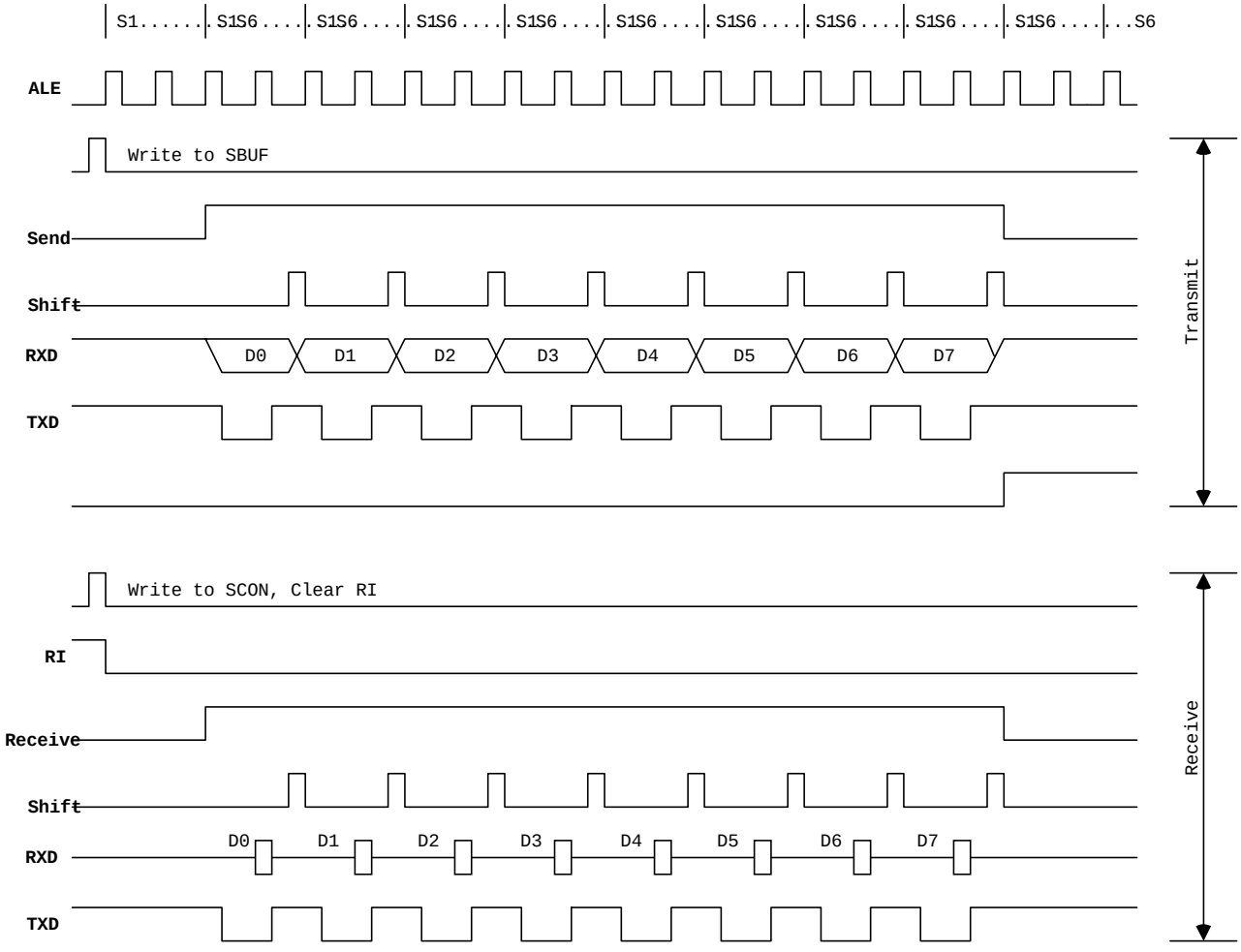
External Program Memory Read Cycle



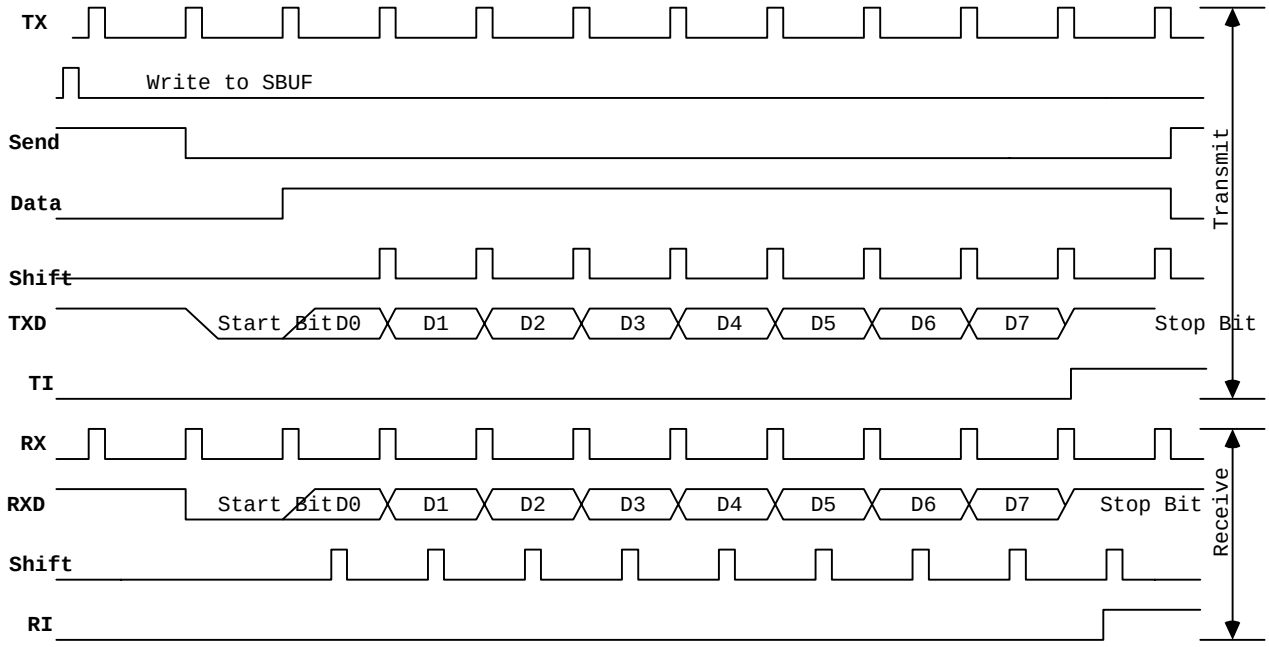
External Data Memory Read Cycle



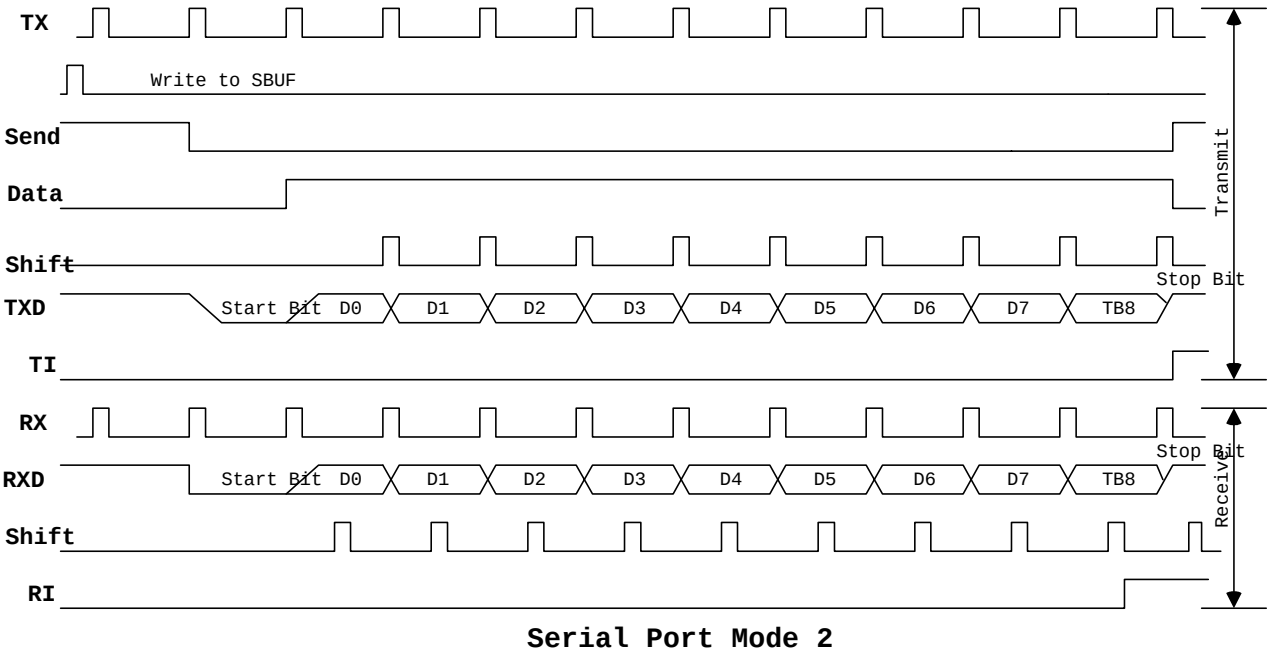
External Data Memory Write Cycle



Serial Port Mode 0



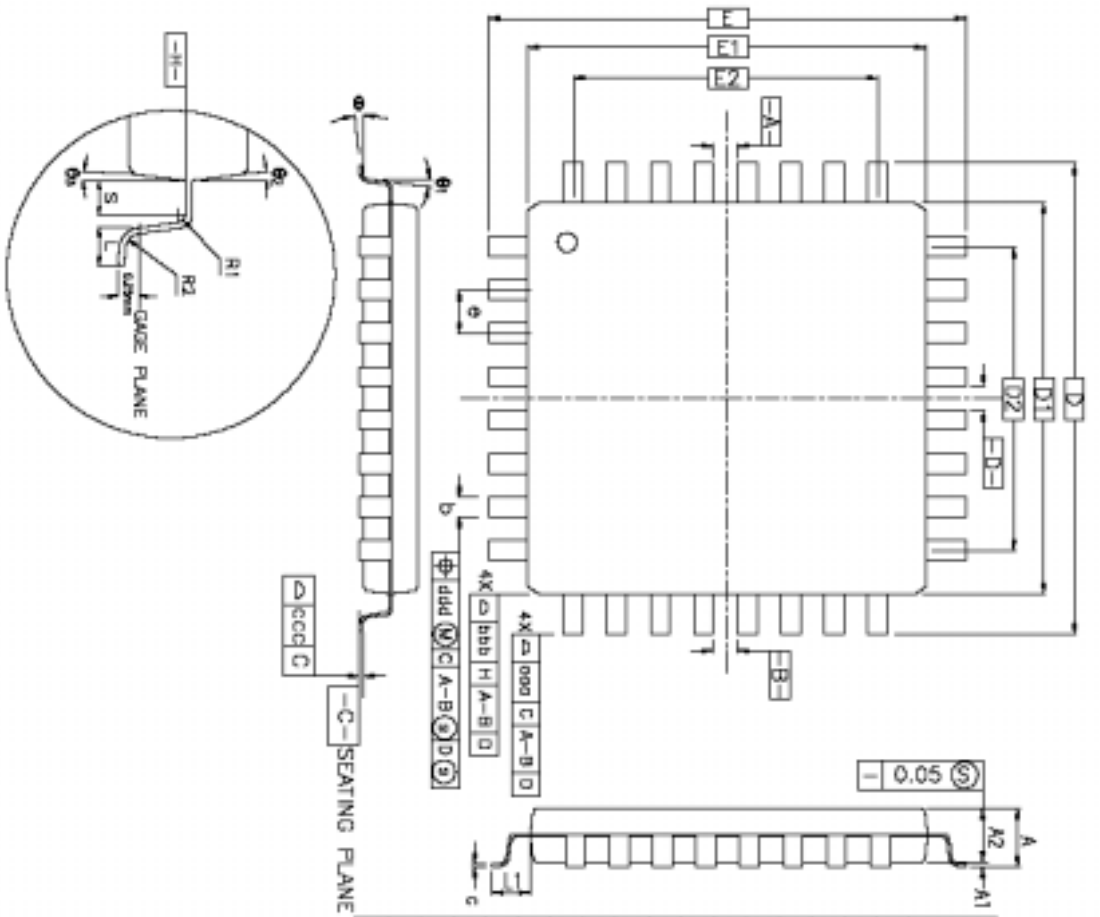
Serial Port Mode 1



Serial Port Mode 2

PACKAGE DIMENSIONS

- LQFP-32 Package



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 44L WERE BASE ON THOSE OF 48L SINCE THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.