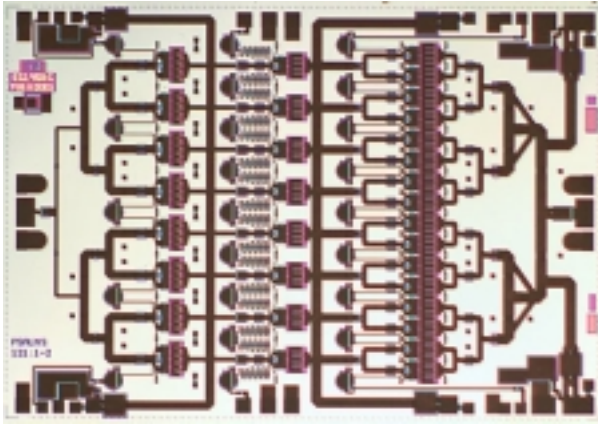


28-31 GHz Ka Band HPA



Key Features

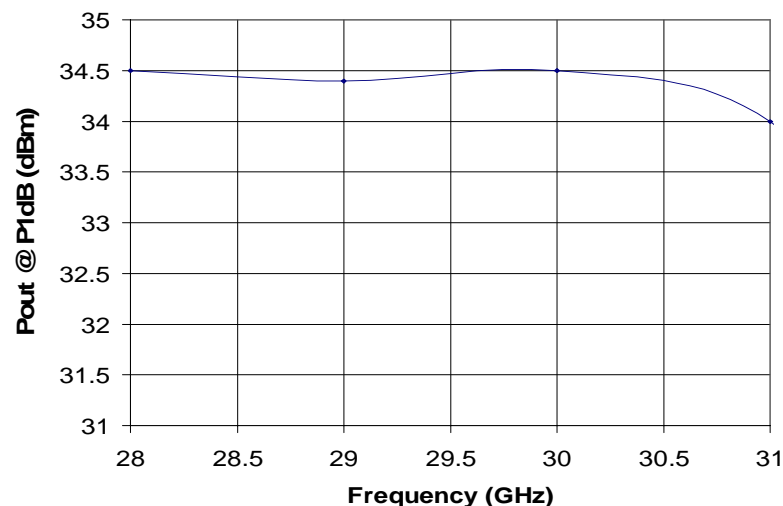
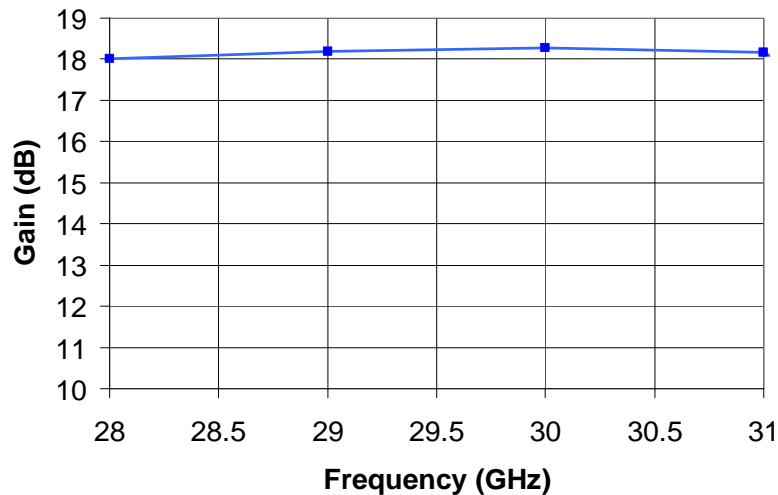
- 0.25 um pHEMT Technology
- 18 dB Nominal Gain
- 34.5 dBm Nominal P1dB
- 40 dBm OTOI Typical
- Bias 6 V @ 2.1 A

Primary Applications

- Satellite Ground Terminal
- Point-to-Point Radio

Chip Dimensions 4.290 mm x 3.019 mm

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 2.1\text{ A}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

TABLE I
 MAXIMUM RATINGS

Symbol	Parameter <u>5/</u>	Value	Notes
V ⁺	Positive Supply Voltage	8 V	<u>4/</u>
V ⁻	Negative Supply Voltage Range	-5V TO 0V	
I ⁺	Positive Supply Current (Quiescent)	3.0 A	<u>4/</u>
I _G	Gate Supply Current	62 mA	
P _{IN}	Input Continuous Wave Power	24 dBm	
P _D	Power Dissipation	18.4 W	<u>3/ 4/</u>
T _{CH}	Operating Channel Temperature	150 °C	<u>1/ 2/</u>
T _M	Mounting Temperature (30 Seconds)	320 °C	
T _{STG}	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 7.4 E+6 to 4.6 E+5 hours.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
- 5/ These ratings represent the maximum operable values for this device.

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TABLE II
DC PROBE TEST
(TA = 25 °C ± 5 °C)

Symbol	Parameter	Minimum	Maximum	Unit
$I_{DSS(Q35)*}$	Saturated Drain Current	15	70.5	mA
$G_{m(Q35)*}$	Transconductance	33	79.5	mS
V_P	Pinch-off Voltage	-1.5	-0.5	V
$BV_{GS(Q35)*}$	Breakdown Voltage Gate-Source	-30	-11	V
$BV_{GD(Q35)*}$	Breakdown Voltage Gate-Drain	-30	-11	V

* Q35 is a 150 um Test FET

TABLE III
AUTOPROBE FET PARAMETER MEASUREMENT CONDITIONS

FET Parameters	Test Conditions
I_{DSS} : Maximum drain current (I_{DS}) with gate voltage (V_{GS}) at zero volts.	$V_{GS} = 0.0$ V, drain voltage (V_{DS}) is swept from 0.5 V up to a maximum of 3.5 V in search of the maximum value of I_{DS} ; voltage for I_{DSS} is recorded as VDSP.
G_m : Transconductance; $\frac{(I_{DSS} - I_{DS1})}{V_{G1}}$	For all material types, V_{DS} is swept between 0.5 V and VDSP in search of the maximum value of I_{DS} . This maximum I_{DS} is recorded as I_{DS1} . For Intermediate and Power material, I_{DS1} is measured at $V_{GS} = V_{G1} = -0.5$ V. For Low Noise, HFET and pHEMT material, $V_{GS} = V_{G1} = -0.25$ V. For LNBECOLC, use $V_{GS} = V_{G1} = -0.10$ V.
V_P : Pinch-Off Voltage; V_{GS} for $I_{DS} = 0.5$ mA/mm of gate width.	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.5 mA/mm.
V_{BVGD} : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I_{BD}) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V_{GD}) measured is V_{BVGD} and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V_{BVGS} : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I_{BS}) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V_{GS}) measured is V_{BVGS} and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

TABLE IV
 RF WAFER CHARACTERIZATION TEST
 ($T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$)
 ($V_d = 6\text{V}$, $I_d = 2.048\text{A} \pm 5\%$)

Parameter	Unit	Min	Typical	Max
Frequency	GHz	28		31
Output P1dB	dBm	33.5	34.5	
Small Signal Gain	dB	16	18	
Input Return Loss	dB		-6	
Output Return Loss	dB		-6	
Output TOI	dBm		40	

TABLE V
 THERMAL INFORMATION*

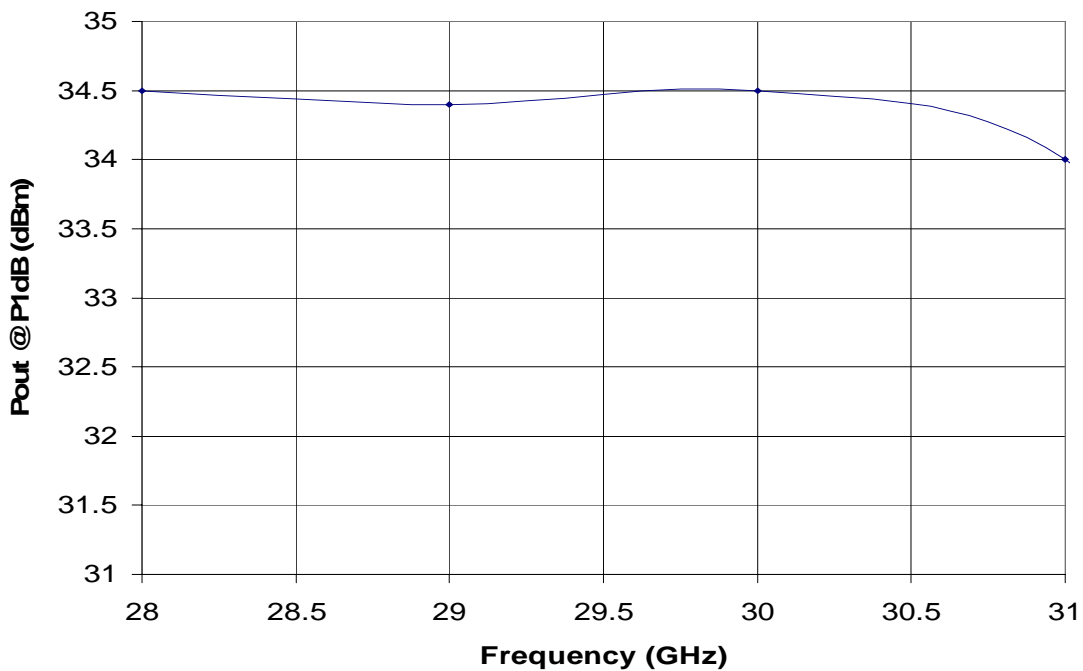
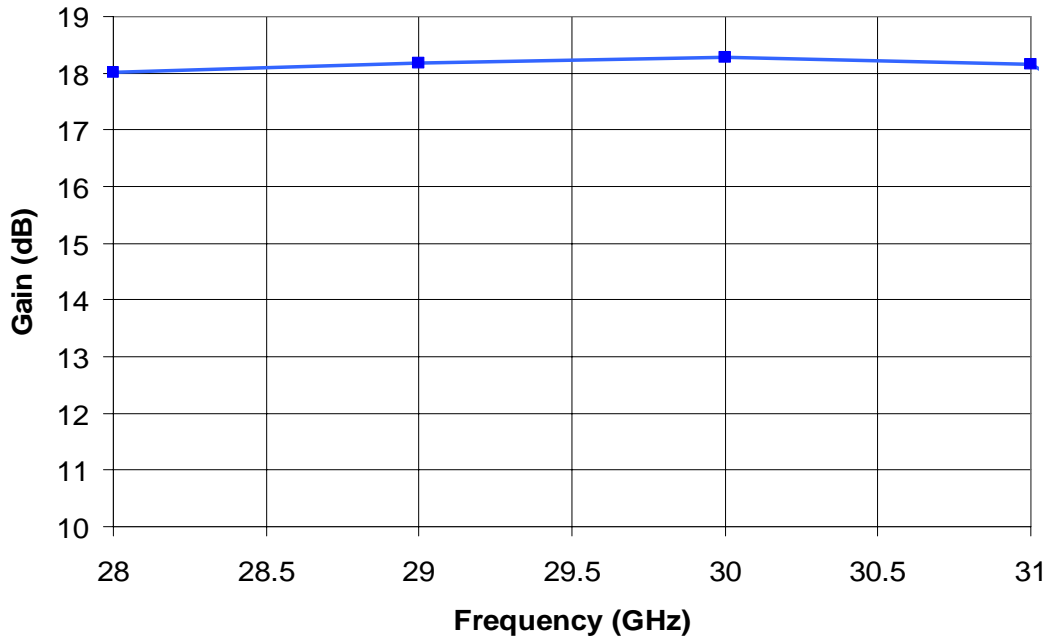
Parameter	Test Conditions	T_{CH} ($^\circ\text{C}$)	$R_{\theta JC}$ ($^\circ\text{C}/\text{W}$)	T_M (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	$V_d = 6\text{V}$ $I_D = 2.048\text{A}$ $P_{diss} = 12.288\text{W}$	127.65	4.69	7.4E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

* This information is a result of a thermal model analysis.

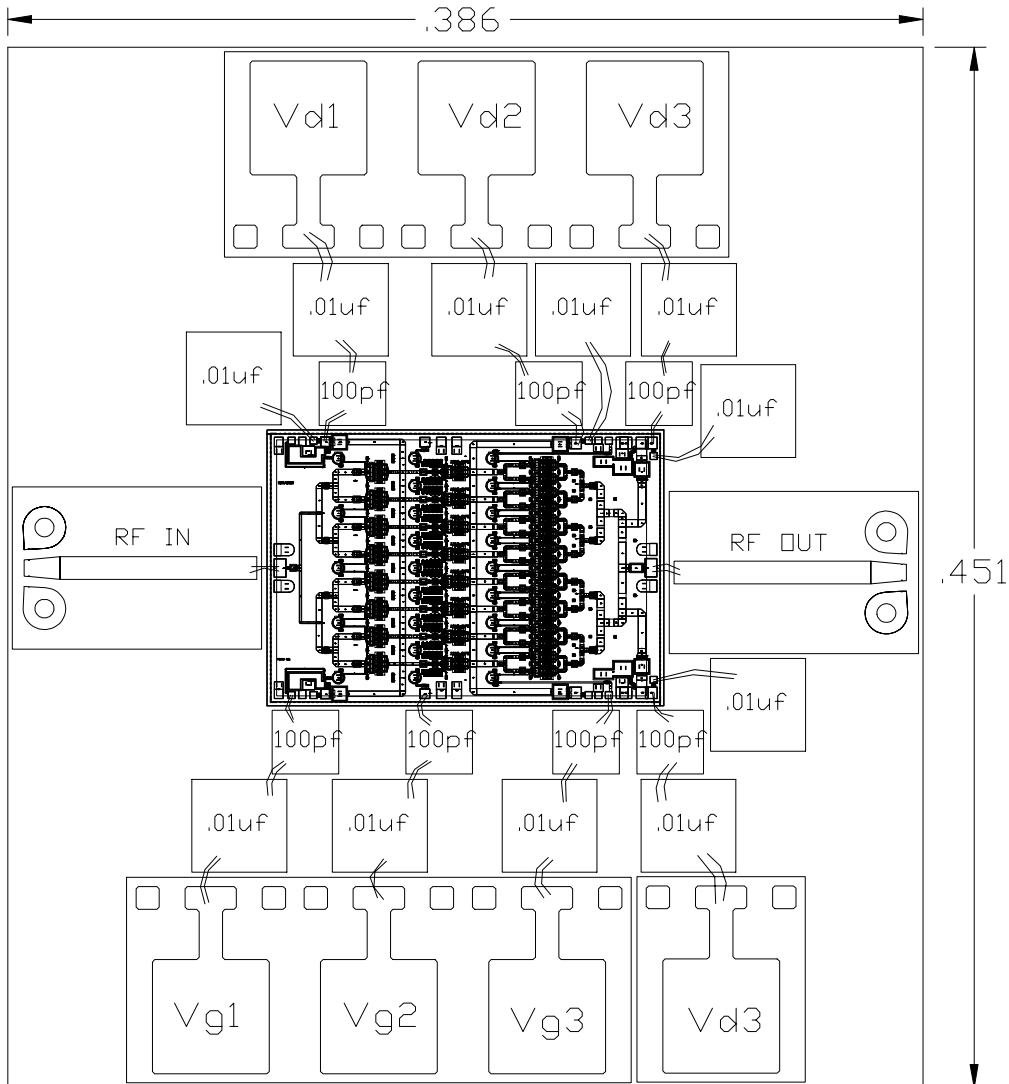
Preliminary Measured Data

Bias Conditions: $V_d = 6\text{ V}$, $I_d = 2.1\text{ A}$



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Chip Assembly & Bonding Diagram

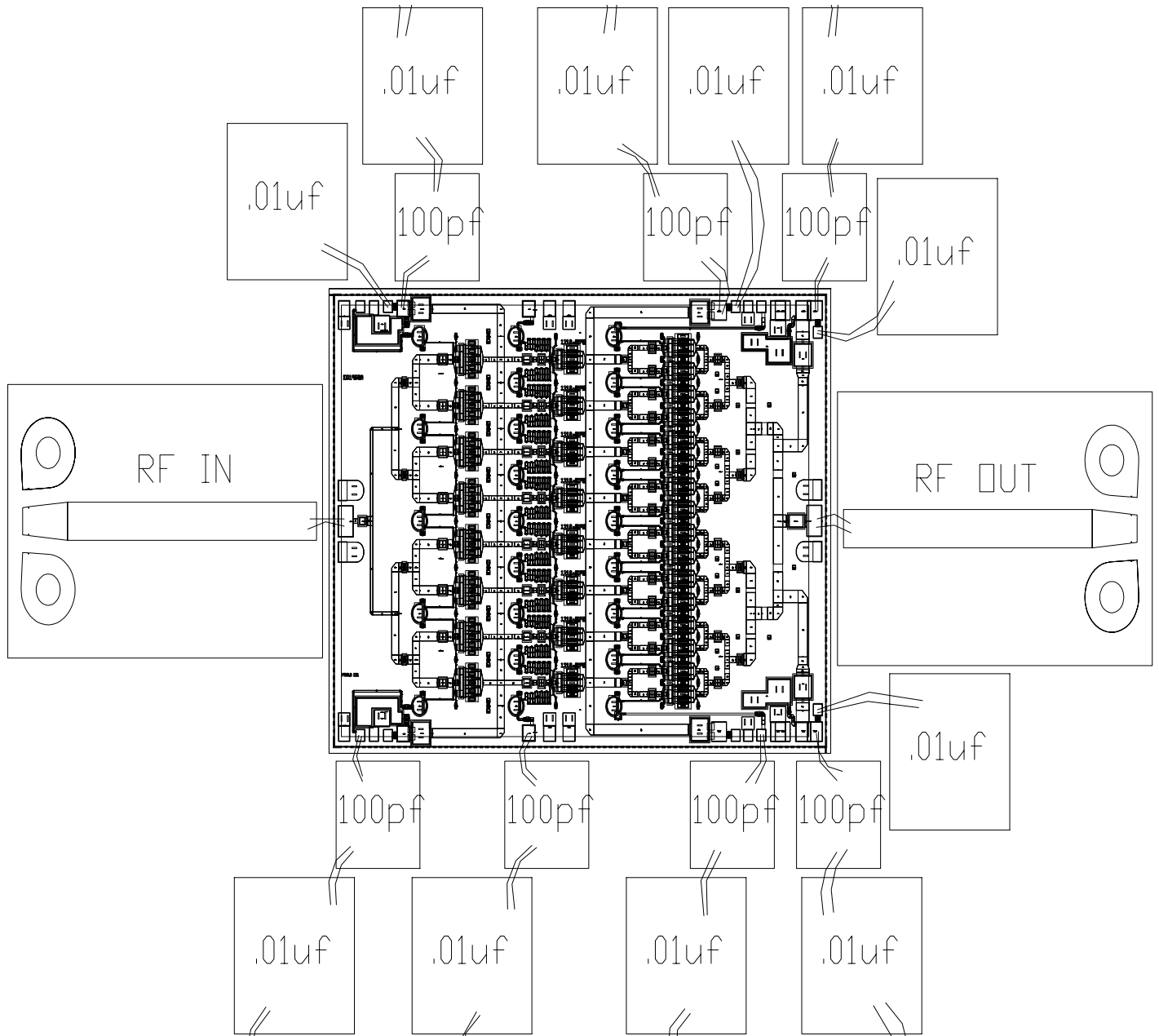


Note: Please refer to page 8 for a magnified view of the chip assembly and bonding diagram

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

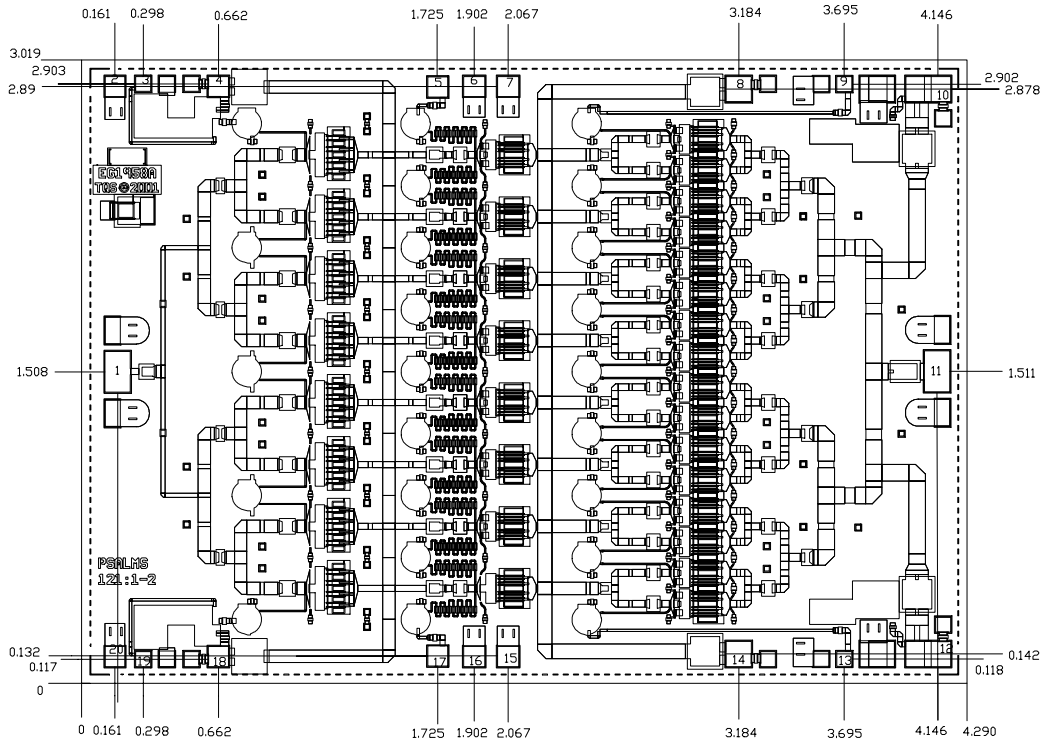
Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Chip Assembly and Bonding Diagram



Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.

Mechanical Drawing



Units: Millimeters (inches)

Thickness: 0.0508 (0.002) (reference only)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size +/- 0.0508 (0.002)

Bond pad #1	<RF Input>	0.130 x 0.205 (0.0051 x 0.0081)
Bond pad #11	<RF Output>	0.130 x 0.205 (0.0051 x 0.0081)
Bond pad #2, 20	<GND>	0.102 x 0.105 (0.004 x 0.0041)
Bond pad #3, 19	<VG1>	0.085 x 0.085 (0.0033 x 0.0033)
Bond pad #4, 18	<VD1>	0.105 x 0.105 (0.0041 x 0.0042)
Bond pad #5, 17	<VG2>	0.110 x 0.110 (0.0043 x 0.0043)
Bond pad #6, 7, 15, 16	<GND>	0.110 x 0.105 (0.0043 x 0.0042)
Bond pad #8, 14	<VD2>	0.130 x 0.130 (0.0051 x 0.0051)
Bond pad #9, 13	<VG3>	0.085 x 0.085 (0.0033 x 0.0033)
Bond pad #10, 12	<VD3>	0.130 x 0.130 (0.0051 x 0.0051)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Note: Devices designated as EPU are typically early in their characterization process prior to finalizing all electrical and process specifications. Specifications are subject to change without notice.