TOSHIBA Diode Silicon Epitaxial Planar Type

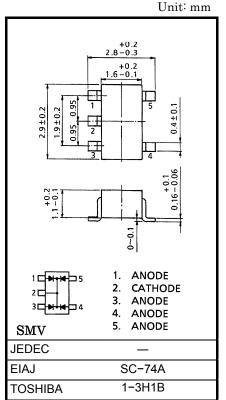
# **1SS309**

#### Ultra High Speed Switching Applications

- Small package : SC-74A
- Low forward voltage  $: V_{F(3)} = 0.90V (typ.)$
- Fast reverse recovery time: t<sub>rr</sub> = 1.6ns (typ.)
- Small total capacitance  $: C_T = 0.9 pF (typ.)$

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	
Maximum (peak) reverse voltage	V <sub>RM</sub>	85	V	
Reverse voltage	V <sub>R</sub>	80	V	
Maximum (peak) forward current	I <sub>FM</sub>	300 (*)	mA	
Average forward current	Ι <sub>Ο</sub>	100 (*)	mA	
Surge current (10ms)	I <sub>FSM</sub>	2 (*)	A	
Power dissipation	Р	200	mW	
Junction temperature	Тј	125	°C	
Storage temperature	T <sub>stg</sub>	-55~125	°C	



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating

Weight: 0.014g

temperature/current/voltage, etc.) are within the absolute maximum ratings.

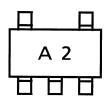
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(\*) Unit rating. Total rating = unit rating × 1.5

## Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit	
Forward voltage	V <sub>F (1)</sub>	_	I <sub>F</sub> = 1mA		0.60	_		
	V <sub>F (2)</sub>	-	I <sub>F</sub> = 10mA	_	0.72	_	V	
	V <sub>F (3)</sub>	-	I <sub>F</sub> = 100mA	_	0.90	1.20		
Reverse current	I <sub>R (1)</sub>	-	V <sub>R</sub> = 30V	_	_	0.1		
	I <sub>R (2)</sub>	-	V <sub>R</sub> = 80V	_	_	0.5	μA	
Total capacitance	CT	_	V <sub>R</sub> = 0, f = 1MHz		0.9	3.0	pF	
Reverse recovery time	t <sub>rr</sub>	_	I <sub>F</sub> = 10mA, Fig.1		1.6	4.0	ns	

#### Marking



# TOSHIBA

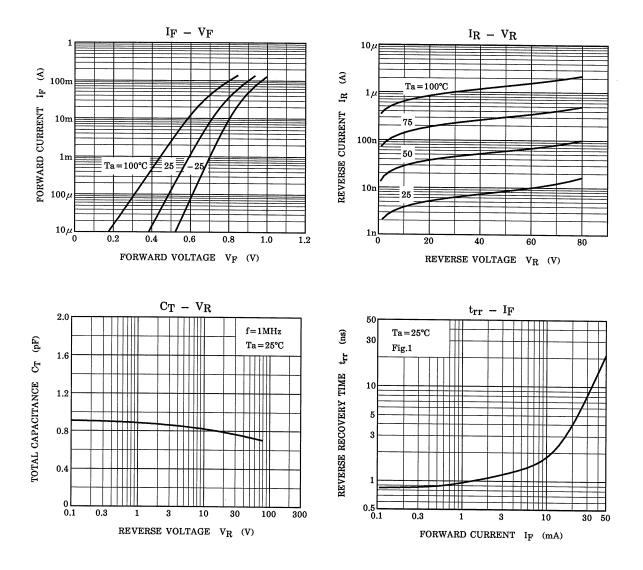
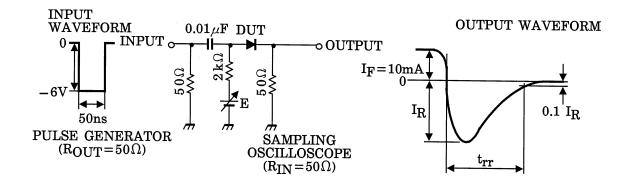


Fig.1 Reverse Recovery Time (trr) Test Circuit



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20070701-EN GENERAL

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