

6N137

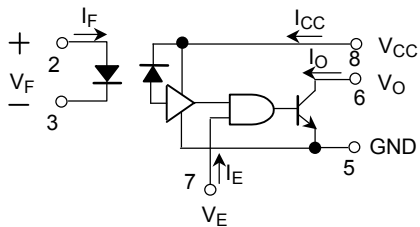
Digital Logic Isolation
 Tele-Communication
 Analog Data Equipment Control

The TOSHIBA 6N137 consist of a high emitting diode and a one chip photo IC. This unit is 8-lead DIP package.

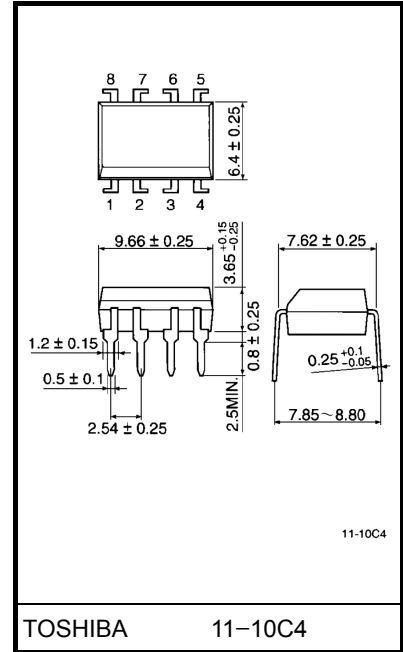
- LSTTL / TTL compatible: 5V Supply
- Ultra high speed: 10MBd
- Guaranteed performance over temperature: 0°C to 70°C
- High isolation voltage: 2500Vrms min.
- UL recognized: UL1577, file no. E67349

Truth Table

| Input | Enable | Output |
|-------|--------|--------|
| H | H | L |
| L | H | H |
| H | L | H |
| L | L | H |

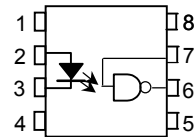


Unit in mm



Weight: 0.54g

Pin Configurations (top view)



- 1 : N.C.
- 2 : Anode
- 3 : Cathode
- 4 : N.C.
- 5 : GND
- 6 : Output(Open collector)
- 7 : Enable
- 8 : VCC

Absolute Maximum Ratings

| Characteristic | | Symbol | Rating | Unit |
|---|--|-----------|---------|------|
| LED | Forward current | I_F | 20 | mA |
| | Pulse forward current (Note 1) | I_{FP} | 40 | mA |
| | Reverse voltage | V_R | 5 | V |
| Detector | Output current | I_O | 50 | mA |
| | Output voltage | V_O | 7 | V |
| | Supply voltage (1 minute maximum) | V_{CC} | 7 | V |
| | Enable input voltage (not to exceed V_{CC} by more than 500mV) | V_{EH} | 5.5 | V |
| | Output collector power dissipation | P_O | 85 | mW |
| Operating temperature range | | T_{opr} | 0~70 | °C |
| Storage temperature range | | T_{stg} | -55~125 | °C |
| Lead solder temperature (10 s) (Note 2) | | T_{sol} | 260 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note 1) 50% duty cycle, 1ms pulse width.

(Note 2) Soldering portion of lead: Up to 2mm from the body of the device.

Recommended Operating Conditions

| Characteristic | Symbol | Min. | Max. | Unit |
|--|----------|------|----------|---------|
| Input current, low level each channel | I_{FL} | 0 | 250 | μ A |
| Input current, high level each channel | I_{FH} | 7 | 20 | mA |
| High level enable voltage | V_{EH} | 2.0 | V_{CC} | V |
| Low level enable voltage (output high) | V_{EL} | 0 | 0.8 | V |
| Supply voltage, output* | V_{CC} | 4.5 | 5.5 | V |
| Fan out (TTL load) | N | — | 8 | — |
| Operating temperature | T_a | 0 | 70 | °C |

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

*This item denotes operating ranges, not meaning of recommended operating conditions.

Precaution

Please be careful of the followings.

A ceramic capacitor(0.1 μ F)should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1cm.

Electrical Characteristics
Over Recommended Temperature (Ta = 0~70°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min. | (**)Typ. | Max. | Unit |
|--|------------------|---|------|------------------|------|------|
| High level output current | I _{OH} | V _{CC} =5.5V, V _O =5.5V I _F =250μA, V _E = 2.0V | — | 1 | 250 | μA |
| Low level output voltage | V _{OL} | V _{CC} =5.5V, I _F =5mA V _{EH} =2.0V I _{OL} (sinking)=13mA | — | 0.4 | 0.6 | V |
| High level enable current | I _{EH} | V _{CC} =5.5V, V _E =2.0V | — | -1.0 | — | mA |
| Low level enable current | I _{EL} | V _{CC} =5.5V, V _E =0.5V | — | -1.6 | -2.0 | mA |
| High level supply current | I _{CCH} | V _{CC} =5.5V, I _F =0, V _E =0.5V | — | 7 | 15 | mA |
| Low level supply current | I _{CCL} | V _{CC} =5.5V, I _F =10mA V _E =0.5V | — | 12 | 18 | mA |
| Resistance (input-output) (Note 3) | R _{I-O} | V _{I-O} =500V, Ta=25°C R.H.≤60% | — | 10 ¹² | — | Ω |
| Capacitance (input-output) (Note 3) | C _{I-O} | f=1MHz, Ta=25°C | — | 0.6 | — | pF |
| Input forward voltage | V _F | I _F =10mA, Ta=25°C | — | 1.65 | 1.75 | V |
| Input reverse breakdown voltage | BV _R | I _R =10μA, Ta=25°C | 5 | — | — | V |
| Input capacitance | C _{IN} | V _F =0, f=1MHz | — | 45 | — | pF |
| Current transfer ratio | CTR | I _F =5.0mA, R _L =100Ω | — | 1000 | — | % |

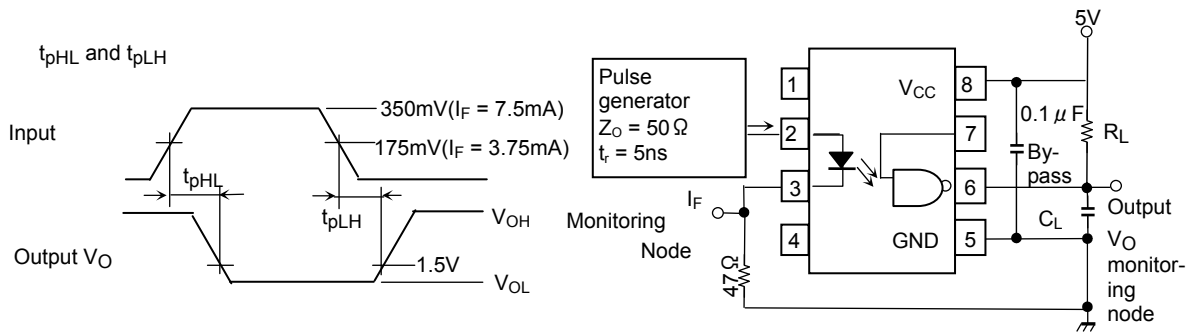
(**) All typical values are at V_{CC}=5V, Ta=25°C

(Note 3) Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (Ta = 25°C, VCC = 5V)

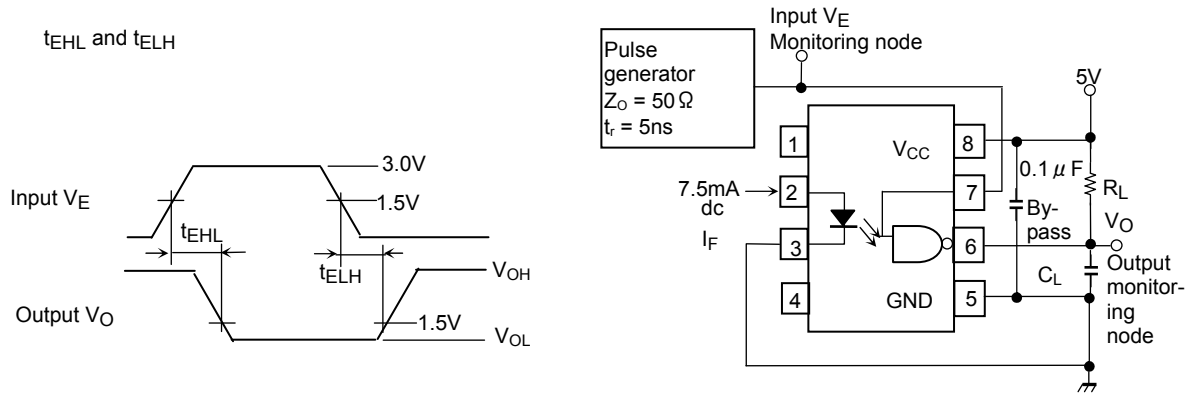
| Characteristic | Symbol | Test Circuit | Test Condition | Min. | Typ. | Max. | Unit |
|--|---------------|--------------|---|------|------|------|-------------|
| Propagation delay time to high output level | t_{pLH} | 1 | $R_L=350\Omega$, $C_L=15pF$ $I_F=7.5mA$ | — | 60 | 75 | ns |
| Propagation delay time to low output level | t_{pHL} | 1 | $R_L=350\Omega$, $C_L=15pF$ $I_F=7.5mA$ | — | 60 | 75 | ns |
| Output rise–fall time (10–90%) | t_r , t_f | — | $R_L=350\Omega$, $C_L=15pF$ $I_F=7.5mA$ | — | 30 | — | ns |
| Propagation delay time of enable from V_{EH} to V_{EL} | t_{ELH} | 2 | $R_L=350\Omega$, $C_L=15pF$ $I_F=7.5mA$ $V_{EH}=3.0V$ $V_{EL}=0.5V$ | — | 25 | — | ns |
| Propagation delay time of enable from V_{EL} to V_{EH} | t_{EHL} | 2 | $R_L=350\Omega$, $C_L=15pF$ $I_F=7.5mA$ $V_{EH}=3.0V$ $V_{EL}=0.5V$ | — | 25 | — | ns |
| Common mode transient immunity at logic high output level | CM_H | 3 | $V_{CM}=10V$ $R_L=350\Omega$ $V_{O(min.)}=2V$ $I_F=0mA$ | — | 200 | — | V / μs |
| Common mode transient immunity at logic low output level | CM_L | 3 | $V_{CM}=10V$ $R_L=350\Omega$ $V_{O(max.)}=0.8V$ $I_F=5mA$ | — | -500 | — | V / μs |

Test Circuit 1.



· C_L is approximately 15pF which includes probe and stray wiring capacitance.

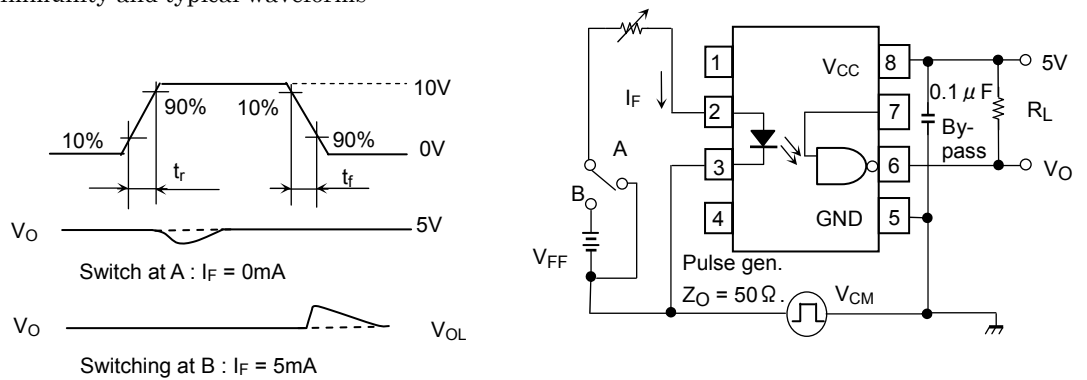
Test Circuit 2.

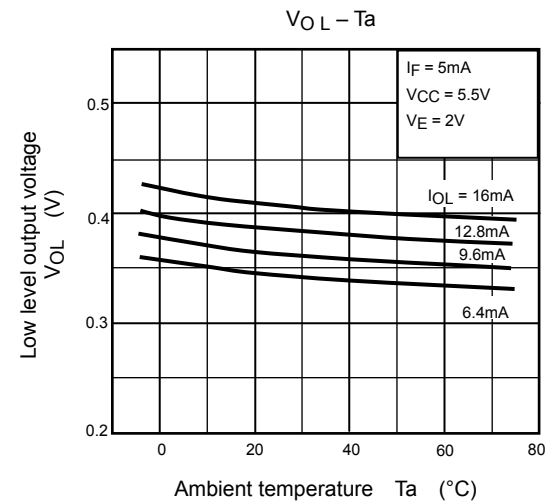
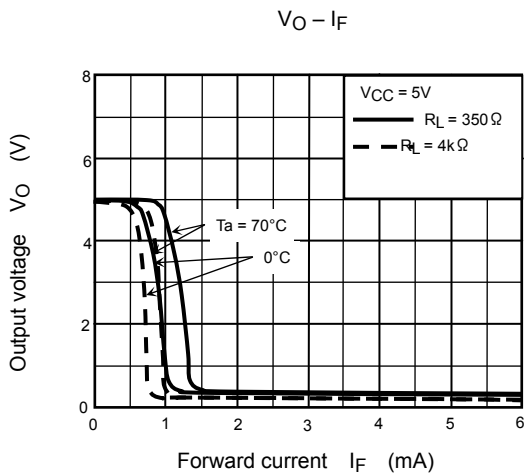
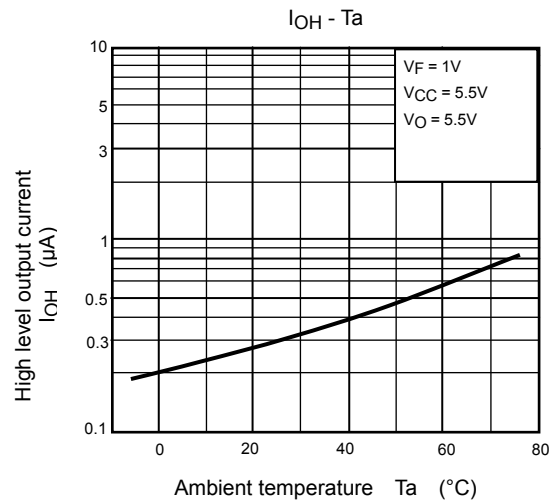
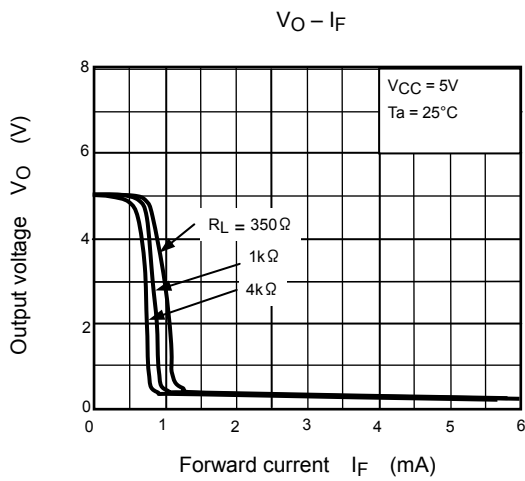
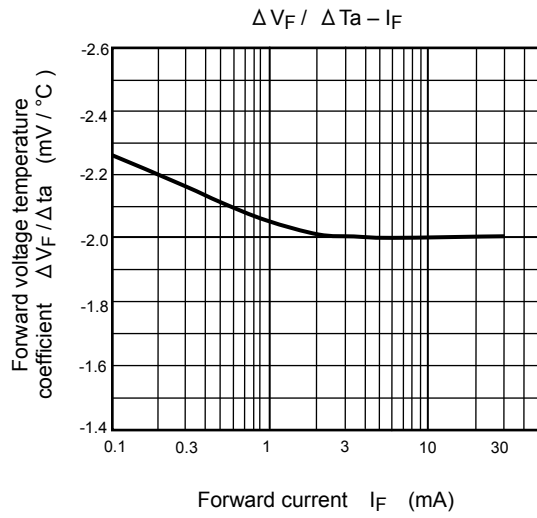
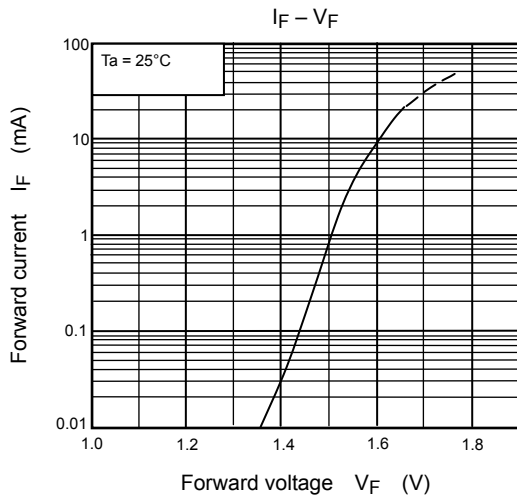


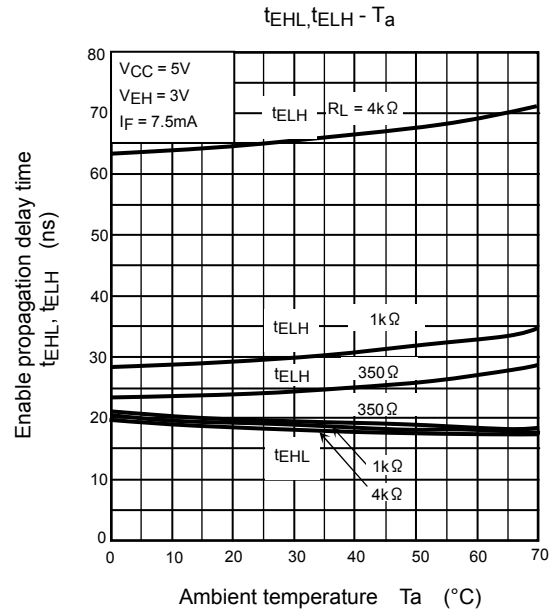
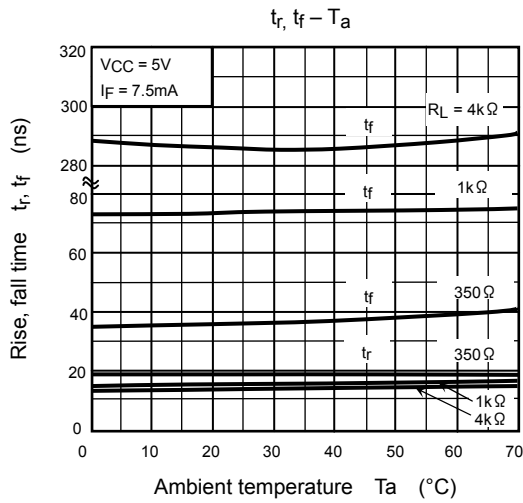
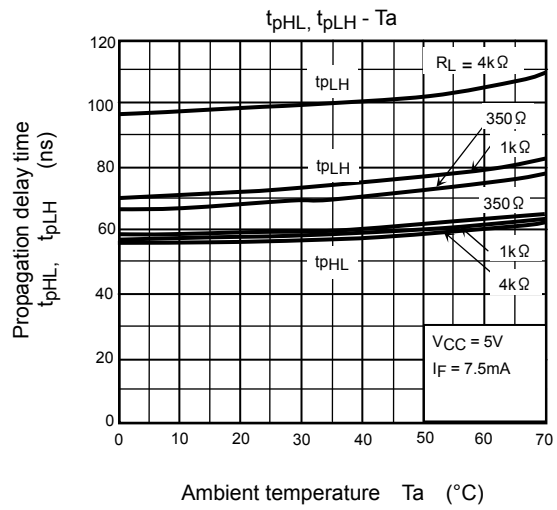
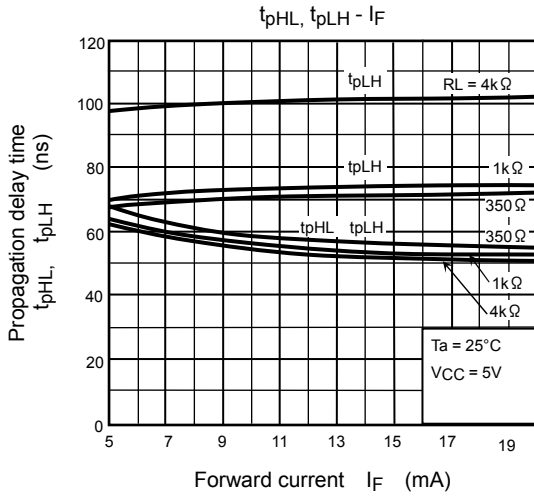
· C_L is approximately 15pF which includes prove and stray wiring capacitance.

Test Circuit 3.

Transient immunity and typical waveforms







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20070701-EN

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