► EC motor control

system evaluation chip E910.46

FEATURES

- ► High voltage supply in the range VS = 6.0 V to 58 V
- ► Drive of up to 6 external n-channel Power FETs (3 high side- and 3 low side switches)
- ► Programmability of functions and parameters by SPI µP interface
- ► Self adjusting driver timing and power FET protection
- ► High power efficiency
- ► Low RF emission due to the field programmable driver technology
- ► Three current measurement amplifiers and programmable over current protection
- ► On chip and external over temperature detection and protection
- ► Programmable analog measurement channels (temperature and motor currents)
- ► Position detection by BEMF
- ► Sleep / Wake up mode system
- ► 5V or 3.3V interface to control device
- ► Developmentkits available (programmable board and software with PC Interface)
- ► −40°C to +125°C operating temperature
- ► PLCC68 package

APPLICATION

- ► EC or DC motor drive / regulation
- ► Fan cooler
- ► Air-conditioning
- ► Pumps

DESCRIPTION

The IC is a PWM EC brushless motor driver/controller to implement a motor regulator together with n-channel power FET B6-configuration and a µC The programmability of parameters (e.g. threshold values of over current, over temperature, motor failures, EMC conditions, etc.) can be used to drive motors in a widely different range. These programmability features and the driver channel control inputs and allow this chip to act in general motor regulator applications, too. The special programmable switching technology (pendingpatent) enables an excellent EMC behavior.

The device works in typical motor regulator systems as physical interface between a µC or a special controller hardware and the power FET-motor load configuration. The user has the complete control over the logical behaviour by software implementation in the µC. In this way all control/regulation strategies of the motor can be realised by software development.

BLOCK DIAGRAM

PINNING

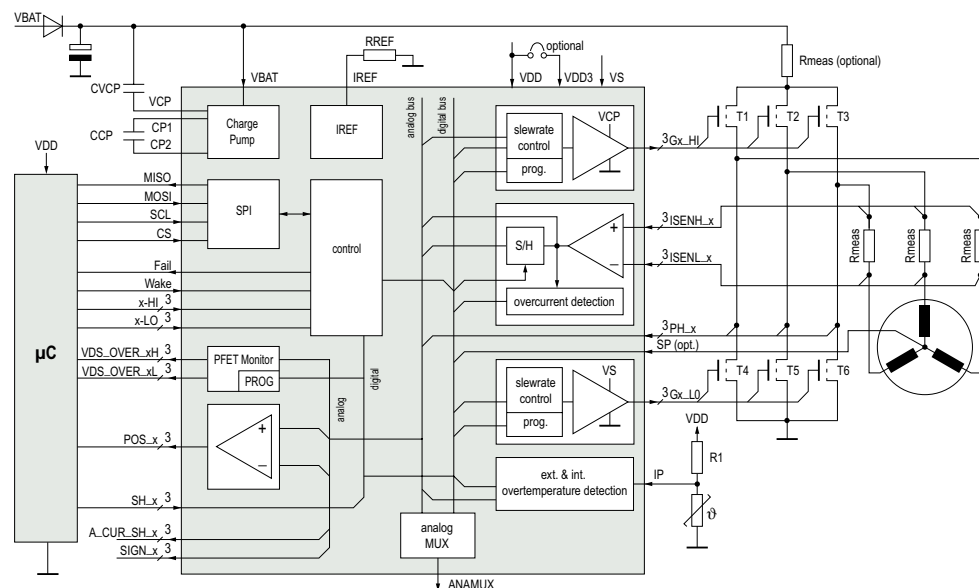| Pin	Name	Description
1	ISENH_A	Positive current measurement input, channel A
2	ISENL_A	Negative current measurement input, channel A
3	DGND	Digital ground
4	VDD	5V supply
5-7	A_CUR_SH_[C-A]	Current measurement output, channel [A-C], S&H
8	TP	Temperature sensor input
9	ANAMUX	Analog MUX output
10	IREF	Reference current output
11-13	SH_[A-C]	Sample and hold control input, channel [A-C]
14-16	SIGN[A-C]	Sign of current output, channel [A-C]
17	VDD3	3.3 V or 5 V supply of control interface
18	VSSA	Analog ground
19	CS	Enable signal of SPI
20	SCL	Clock of SPI
21	MOSI	Data input of SPI
22	MISO	Data output of SPI
23	FAIL	Failure signal, high active
24	WAKE	Wake up signal, low active
25-27	POS_[A-C]	Position signal of BEMF detection, channel [A-C]
28-29	VDS_OVER_A[H,L]	VDS detection, high/low side switch, channel A
30-31	VDS_OVER_B[H,L]	VDS detection, high/low side switch, channel B
32-33	VDS_OVER_C[H,L]	VDS detection, high/low side switch, channel C
34	VDD3	3.3V or 5V supply of control interface
35	AGND	Analog ground
36-38	[A-C]_HI	Ctrl input of HS switch, channel [A-C], high active
39-41	[A-C]_LO	Ctrl input of LS switch, channel [A-C], high active
42	VS	12V supply
43	PGND	Power ground
44,46	GC_LO, GB_LO	Driver output, gate LS FET, channel c/b
48	GA_LO	Driver output, gate LS power FET, channel A

PACKAGE
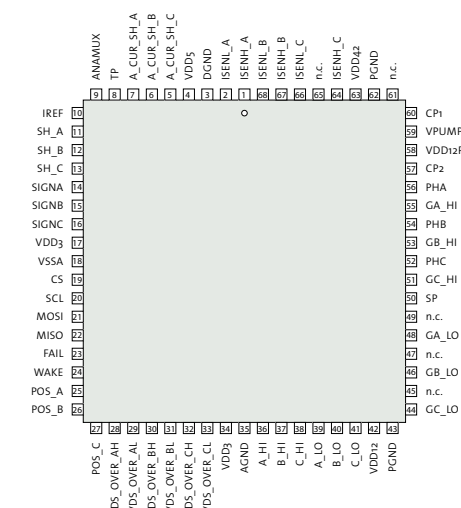
AVAILABILITY

Samples	available
Series	tbd.

Pin	Name	Description
50	SP	Star point connection
51	GC_HI	Driver output, gate HS power FET, channel C
52,54, 56	PHC, PHB, PHA	Phase C-A
53	GB_HI	Driver output, gate HS power FET, channel B
55	GA_HI	Driver output, gate HS power FET, channel A
57	CP2	Switch capacitor connection 2 of charge pump
58,63	VBAT, VS	12V supply, high voltage supply
59	VPUMP	Pumped voltage, storage capacitor connection
60	CP1	Switch capacitor connection 1 of charge pump
62	PGND	Power ground
64,66	ISENH_C, ISENL_C	Pos/Neg current measurement input, channel C
67-68	ISENH_B, ISENL_B	Pos/Neg current measurement input, channel B