

DRAM MODULE

MT12D436
MT24D836

FEATURES

- JEDEC- and industry-standard pinout in a 72-pin, single in-line memory module (SIMM)
- 16MB (4 Meg x 36) and 32MB (8 Meg x 36) parity versions
- High-performance CMOS silicon-gate process
- Single 5V $\pm 10\%$ power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR) and HIDDEN
- 2,048-cycle refresh distributed across 32ms
- FAST PAGE MODE (FPM) access cycle
- Multiple RAS# lines allow x18 or x36 widths

OPTIONS

- Timing
60ns access
- Packages
72-pin SIMM
72-pin SIMM (gold)
72-pin SIMM low profile (1.00")
72-pin SIMM (gold) low profile (1.00")

MARKING

-6

M

G

DM

DG

KEY TIMING PARAMETERS

| SPEED | t _{RC} | t _{RAC} | t _{PC} | t _{AA} | t _{CAC} | t _{RP} |
|-------|-----------------|------------------|-----------------|-----------------|------------------|-----------------|
| -6 | 110ns | 60ns | 35ns | 30ns | 15ns | 40ns |

PART NUMBERS

| PART NUMBER | CONFIGURATION | PLATING | HEIGHT |
|---------------|---------------|----------|--------|
| MT12D436G-xx | 4 Meg x 36 | Gold | 1.190" |
| MT12D436M-xx | 4 Meg x 36 | Tin/Lead | 1.190" |
| MT12D436DG-xx | 4 Meg x 36 | Gold | 1.000" |
| MT12D436DM-xx | 4 Meg x 36 | Tin/Lead | 1.000" |
| MT24D836G-xx | 8 Meg x 36 | Gold | 1.190" |
| MT24D836M-xx | 8 Meg x 36 | Tin/Lead | 1.190" |

xx = speed

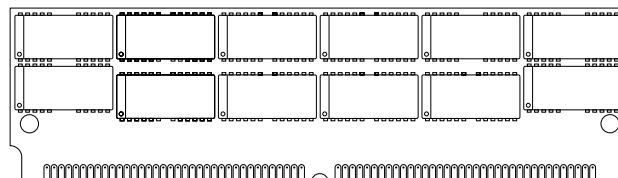
GENERAL DESCRIPTION

The MT12D436 and MT24D836 are randomly accessed 16MB and 32MB solid-state memories organized in a x36 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 22 address bits, which are entered 11 bits (A0-A10) at a time. RAS# is used to latch the first 11 bits and CAS# the latter 11 bits. A READ or WRITE

PIN ASSIGNMENT (Front View)

72-Pin SIMM

- (DD-5) 4 Meg x 36 (shown)
- (DD-6) 8 Meg x 36
- (DD-7) 4 Meg x 36 Low Profile



| PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL | PIN | SYMBOL |
|-----|--------|-----|-----------|-----|-----------|-----|--------|
| 1 | Vss | 19 | A10 | 37 | DQ18 | 55 | DQ13 |
| 2 | DQ1 | 20 | DQ5 | 38 | DQ36 | 56 | DQ31 |
| 3 | DQ19 | 21 | DQ23 | 39 | Vss | 57 | DQ14 |
| 4 | DQ2 | 22 | DQ6 | 40 | CAS0# | 58 | DQ32 |
| 5 | DQ20 | 23 | DQ24 | 41 | CAS2# | 59 | Vcc |
| 6 | DQ3 | 24 | DQ7 | 42 | CAS3# | 60 | DQ33 |
| 7 | DQ21 | 25 | DQ25 | 43 | CAS1# | 61 | DQ15 |
| 8 | DQ4 | 26 | DQ8 | 44 | RAS0# | 62 | DQ34 |
| 9 | DQ22 | 27 | DQ26 | 45 | NC/RAS1#* | 63 | DQ16 |
| 10 | Vcc | 28 | A7 | 46 | NC | 64 | DQ35 |
| 11 | NC | 29 | NC (A11) | 47 | WE# | 65 | DQ17 |
| 12 | A0 | 30 | Vcc | 48 | NC | 66 | NC |
| 13 | A1 | 31 | A8 | 49 | DQ10 | 67 | PRD1 |
| 14 | A2 | 32 | A9 | 50 | DQ28 | 68 | PRD2 |
| 15 | A3 | 33 | NC/RAS3#* | 51 | DQ11 | 69 | PRD3 |
| 16 | A4 | 34 | RAS2# | 52 | DQ29 | 70 | PRD4 |
| 17 | A5 | 35 | DQ27 | 53 | DQ12 | 71 | NC |
| 18 | A6 | 36 | DQ9 | 54 | DQ30 | 72 | Vss |

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

cycle is selected with the WE# input. A logic HIGH on WE# dictates READ mode, while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of CAS#. Since WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined (A0-A10) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

REFRESH

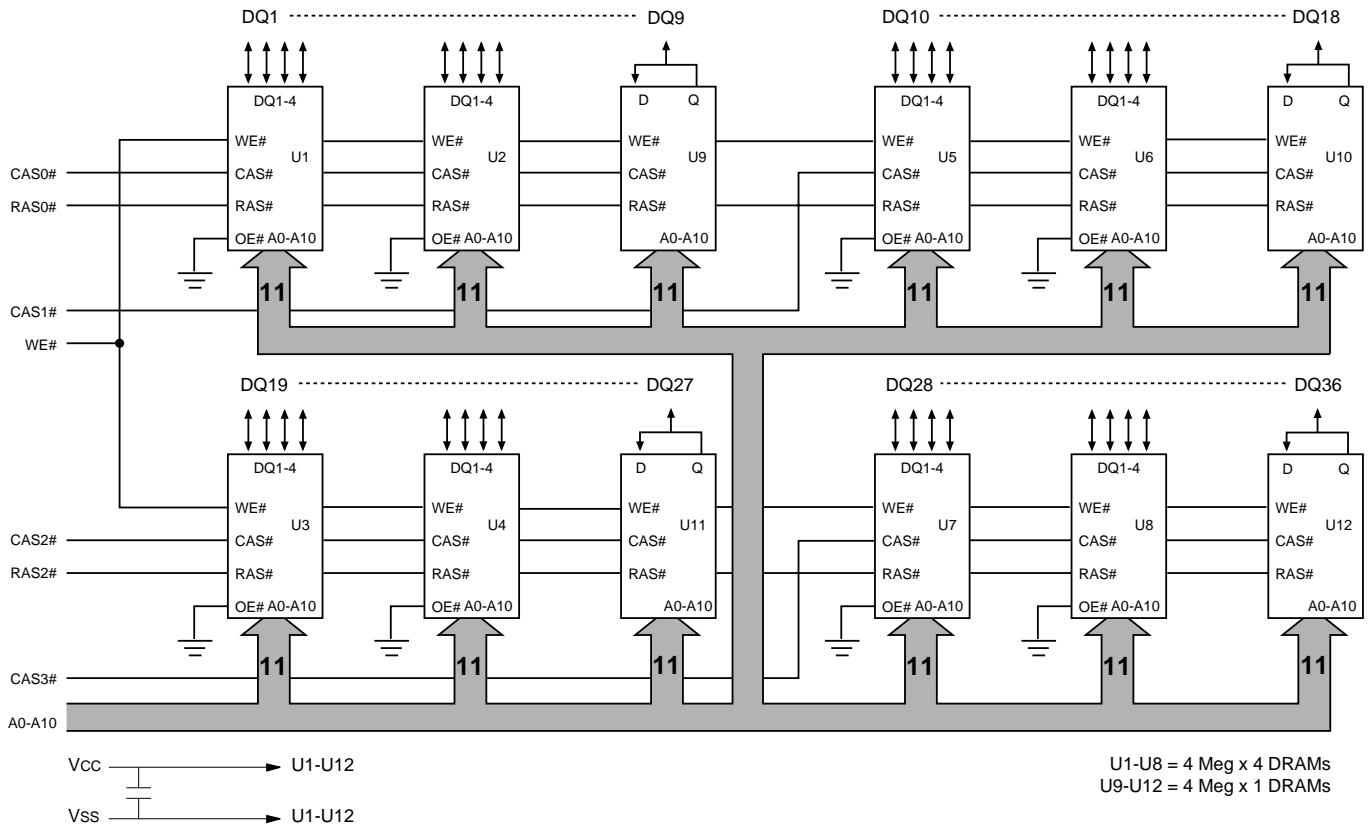
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during

the RAS# HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS# ONLY, CBR or HIDDEN) so that all 2,048 combinations of RAS# addresses (A0-A10) are executed at least every 32ms, regardless of sequence. The CBR REFRESH cycle will invoke the refresh counter for automatic RAS# addressing.

x18 CONFIGURATION

For x18 applications, the corresponding DQ and CAS# pins must be connected together (DQ1 to DQ19, DQ2 to DQ20 and so forth, and CAS0# to CAS2# and CAS1# to CAS3#). Each RAS# is then a bank select for the x18 memory organization.

FUNCTIONAL BLOCK DIAGRAM MT12D436 (16MB)

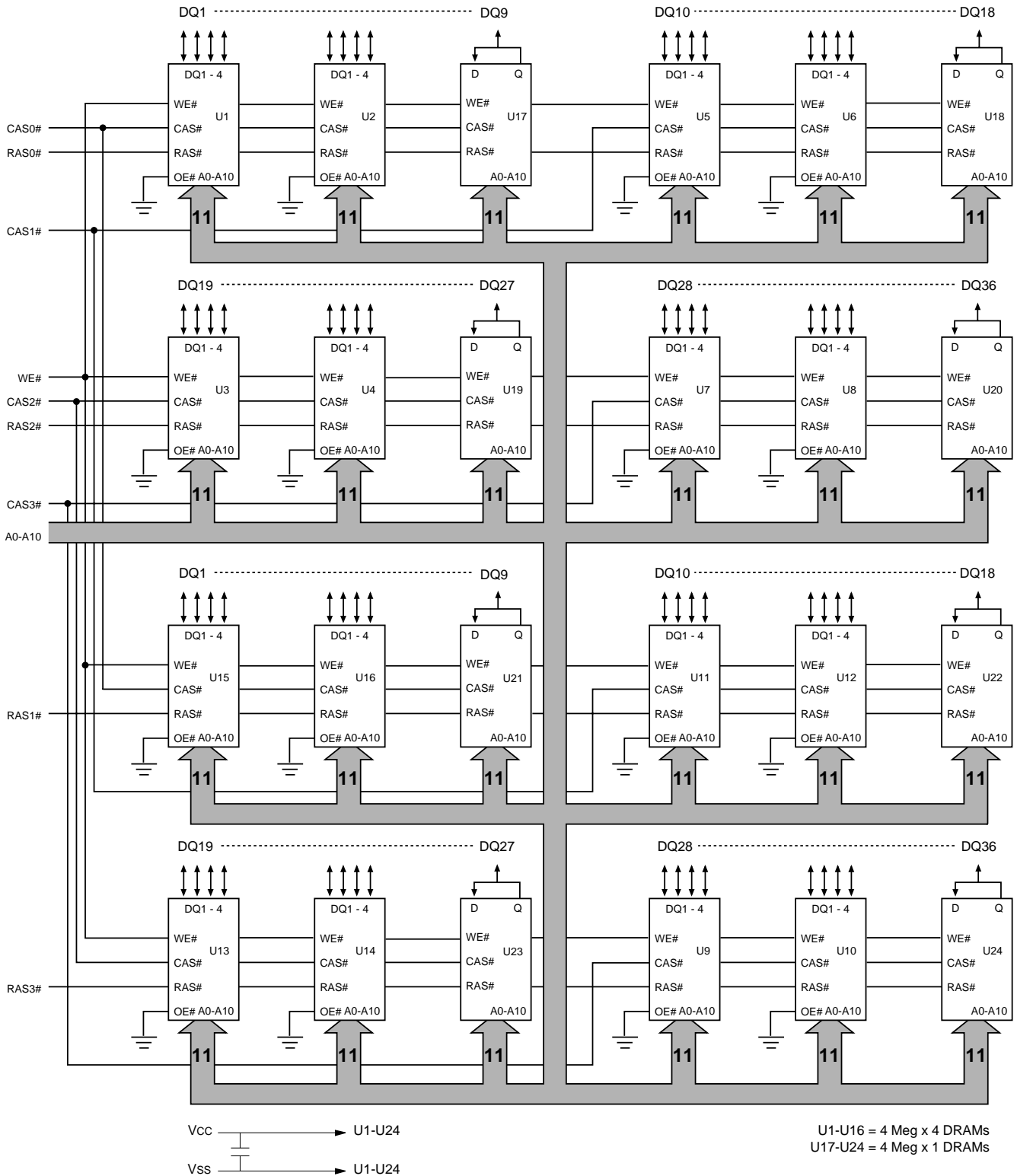


OBSOLETE



4, 8 MEG x 36
PARITY DRAM SIMMs

**FUNCTIONAL BLOCK DIAGRAM
MT24D836 (32MB)**



TRUTH TABLE

| FUNCTION | | RAS# | CAS# | WE# | ADDRESSES | | DATA-IN/OUT |
|-------------------------------|-----------|-------|------|-----|----------------|----------------|-------------|
| | | | | | t _R | t _C | DQ1-DQ36 |
| Standby | | H | H→X | X | X | X | High-Z |
| READ | | L | L | H | ROW | COL | Data-Out |
| EARLY WRITE | | L | L | L | ROW | COL | Data-In |
| FAST-PAGE-MODE READ | 1st Cycle | L | H→L | H | ROW | COL | Data-Out |
| | 2nd Cycle | L | H→L | H | n/a | COL | Data-Out |
| FAST-PAGE-MODE EARLY-WRITE | 1st Cycle | L | H→L | L | ROW | COL | Data-In |
| | 2nd Cycle | L | H→L | L | n/a | COL | Data-In |
| RAS#-ONLY REFRESH | | L | H | X | ROW | n/a | High-Z |
| HIDDEN REFRESH | READ | L→H→L | L | H | ROW | COL | Data-Out |
| | WRITE | L→H→L | L | L | ROW | COL | Data-In |
| CBR REFRESH | | H→L | L | H | X | X | High-Z |

**JEDEC-DEFINED
PRESENCE-DETECT – MT12D436 (16MB)**

| SYMBOL | PIN | -6 |
|--------|-----|-----------------|
| PRD1 | 67 | V _{ss} |
| PRD2 | 68 | NC |
| PRD3 | 69 | NC |
| PRD4 | 70 | NC |

**JEDEC-DEFINED
PRESENCE-DETECT – MT24D836 (32MB)**

| SYMBOL | PIN | -6 |
|--------|-----|-----------------|
| PRD1 | 67 | NC |
| PRD2 | 68 | V _{ss} |
| PRD3 | 69 | NC |
| PRD4 | 70 | NC |

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} -1V to +7V
 Operating Temperature, T_A (ambient) 0°C to +70°C
 Storage Temperature (plastic) -55°C to +125°C
 Power Dissipation 12W
 Short Circuit Output Current 50mA

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +5V ±10%)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES | |
|---|-----------------|-----------------|-----|-------|-------|----|
| Supply Voltage | V _{CC} | 4.5 | 5.5 | V | | |
| Input High (Logic 1) Voltage, all inputs | V _{IH} | 2.4 | 5.5 | V | | |
| Input Low (Logic 0) Voltage, all inputs | V _{IL} | -1.0 | 0.8 | V | | |
| INPUT LEAKAGE CURRENT Any input 0V ≤ V _{IN} ≤ 5.5V (All other pins not under test = 0V) | RAS0#-RAS3# | I _{I1} | -12 | 12 | μA | |
| | A0-A10, WE# | I _{I2} | -48 | 48 | μA | 23 |
| | CAS0#-CAS3# | I _{I3} | -12 | 12 | μA | 23 |
| OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V _{OUT} ≤ 5.5V) | DQ1-DQ36 | I _{OZ} | -10 | 10 | μA | 23 |
| OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA) Output Low Voltage (I _{OUT} = 4.2mA) | V _{OH} | 2.4 | | V | | |
| | V _{OL} | | 0.4 | V | | |

| PARAMETER/CONDITION | SYMBOL | SIZE | MAX | UNITS | NOTES |
|--|------------------|--------------|----------------|-------|-------|
| | | | -6 | | |
| STANDBY CURRENT: (TTL) (RAS# = CAS# = V _{IH}) | I _{CC1} | 16MB 32MB | 22 44 | mA | |
| STANDBY CURRENT: (CMOS) (RAS# = CAS# = other inputs = V _{CC} -0.2V) | I _{CC2} | 16MB 32MB | 16 32 | mA | |
| OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN]) | I _{CC3} | 16MB 32MB | 1,400 1,422 | mA | 3, 22 |
| OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V _{IL} , CAS#, address cycling: t _{PC} = t _{PC} [MIN]) | I _{CC4} | 16MB 32MB | 1,040 1,062 | mA | 3, 22 |
| REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V _{IH} : t _{RC} = t _{RC} [MIN]) | I _{CC5} | 16MB 32MB | 1,400 1,422 | mA | 3, 22 |
| REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: t _{RC} = t _{RC} [MIN]) | I _{CC6} | 16MB 32MB | 1,400 1,422 | mA | 3, 4 |

CAPACITANCE

| PARAMETER | SYMBOL | MAX | | UNITS | NOTES |
|--|------------------|------|------|-------|-------|
| | | 16MB | 32MB | | |
| Input Capacitance: A0-A10 | C _{I1} | 70 | 140 | pF | 2 |
| Input Capacitance: WE# | C _{I2} | 94 | 188 | pF | 2 |
| Input Capacitance: RAS0#, RAS1#, RAS2#, RAS3# | C _{I3} | 50 | 50 | pF | 2 |
| Input Capacitance: CAS0#, CAS1#, CAS2#, CAS3# | C _{I4} | 25 | 50 | pF | 2 |
| Input/Output Capacitance: DQ1-DQ8, DQ10-DQ17, DQ19-DQ26, DQ28-DQ35 | C _{IO1} | 10 | 18 | pF | 2 |
| Input/Output Capacitance: DQ9, DQ18, DQ27, DQ36 | C _{IO2} | 16 | 28 | pF | 2 |

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

| AC CHARACTERISTICS | | -6 | | | |
|---|---------------------|-----|---------|-------|--------|
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
| Access time from column address | t ¹ AA | | 30 | ns | |
| Column-address hold time (referenced to RAS#) | t ¹ AR | 45 | | ns | |
| Column-address setup time | t ¹ ASC | 0 | | ns | |
| Row-address setup time | t ¹ ASR | 0 | | ns | |
| Access time from CAS# | t ¹ CAC | | 15 | ns | |
| Column-address hold time | t ¹ CAH | 10 | | ns | |
| CAS# pulse width | t ¹ CAS | 15 | 10,000 | ns | |
| CAS# hold time (CBR REFRESH) | t ¹ CHR | 15 | | ns | 4 |
| CAS# to output in Low-Z | t ¹ CLZ | 3 | | ns | 21 |
| CAS# precharge time | t ¹ CP | 10 | | ns | 13 |
| Access time from CAS# precharge | t ¹ CPA | | 35 | ns | |
| CAS# to RAS# precharge time | t ¹ CRP | 10 | | ns | |
| CAS# hold time | t ¹ CSH | 60 | | ns | |
| CAS# setup time (CBR REFRESH) | t ¹ CSR | 10 | | ns | 4 |
| Write command to CAS# lead time | t ¹ CWL | 15 | | ns | |
| Data-in hold time | t ¹ DH | 10 | | ns | 18 |
| Data-in setup time | t ¹ DS | 0 | | ns | 18 |
| Output buffer turn-off delay | t ¹ OFF | 3 | 15 | ns | 17, 21 |
| FAST-PAGE-MODE READ or WRITE cycle time | t ¹ PC | 35 | | ns | |
| Access time from RAS# | t ¹ RAC | | 60 | ns | |
| RAS# to column-address delay time | t ¹ RAD | 15 | | ns | 15 |
| Row-address hold time | t ¹ RAH | 10 | | ns | |
| RAS# pulse width | t ¹ RAS | 60 | 10,000 | ns | |
| RAS# pulse width (FAST PAGE MODE) | t ¹ RASP | 60 | 125,000 | ns | |
| Random READ or WRITE cycle time | t ¹ RC | 110 | | ns | |
| RAS# to CAS# delay time | t ¹ RCD | 20 | | ns | 14 |
| Read command hold time (referenced to CAS#) | t ¹ RCH | 0 | | ns | 16 |
| Read command setup time | t ¹ RCS | 0 | | ns | |
| Refresh period (2,048 cycles) | t ¹ REF | | 32 | ms | |
| RAS# precharge time | t ¹ RP | 40 | | ns | |
| RAS# to CAS# precharge time | t ¹ RPC | 0 | | ns | |

OBSOLETE



4, 8 MEG x 36 PARITY DRAM SIMMs

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{cc} = +5V \pm 10\%$)

| AC CHARACTERISTICS | | -6 | | | |
|--|-----------|-----|-----|-------|-------|
| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
| Read command hold time (referenced to RAS#) | t_{RRH} | 0 | | ns | 16 |
| RAS# hold time | t_{RSH} | 15 | | ns | |
| Write command to RAS# lead time | t_{RWL} | 15 | | ns | |
| Transition time (rise or fall) | t_T | 2 | 50 | ns | |
| Write command hold time | t_{WCH} | 10 | | ns | |
| Write command hold time (referenced to RAS#) | t_{WCR} | 45 | | ns | |
| WE# command setup time | t_{WCS} | 0 | | ns | |
| Write command pulse width | t_{WP} | 10 | | ns | |
| WE# hold time (CBR REFRESH) | t_{WRH} | 10 | | ns | |
| WE# setup time (CBR REFRESH) | t_{WRP} | 10 | | ns | |

NOTES

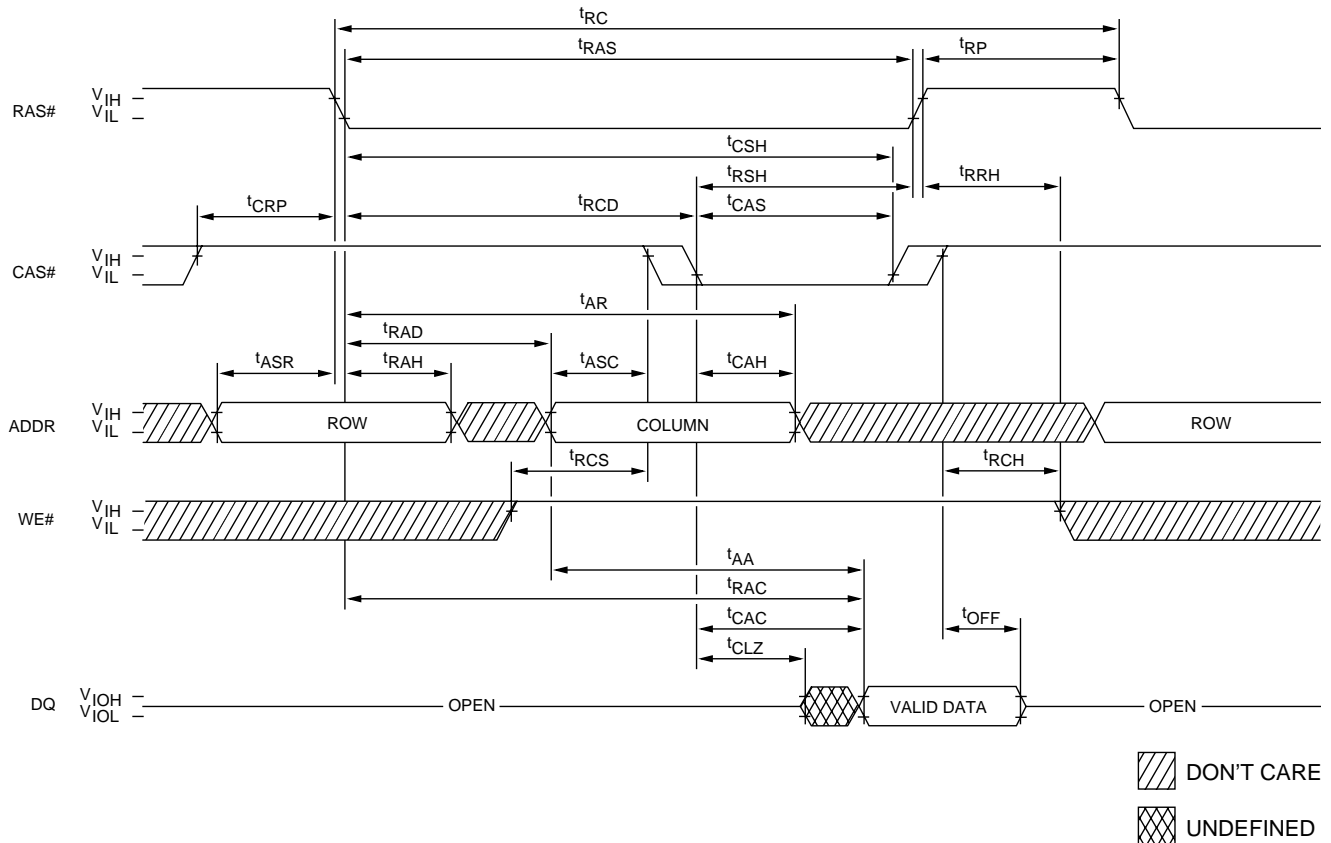
1. All voltages referenced to V_{SS} .
2. This parameter is sampled. Capacitance is measured using MIL-STD-883C, Method 3012.1 (1 MHz AC, $V_{CC} = 4.5V$, DC bias = 2.4V at 15mV RMS).
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. 16MB module values will be half of those shown.

OBSOLETE



4, 8 MEG x 36
PARITY DRAM SIMMs

READ CYCLE

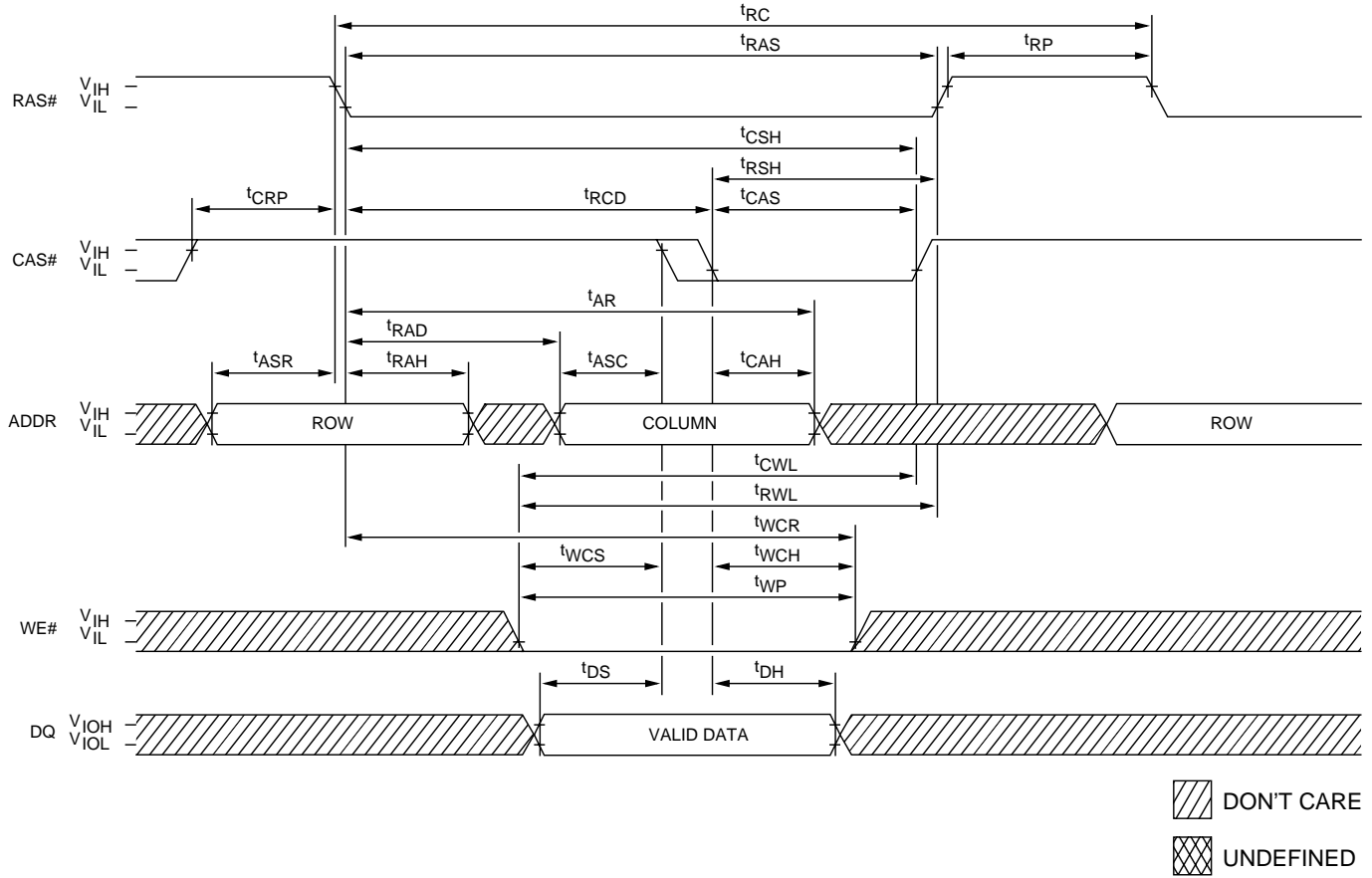


TIMING PARAMETERS

| SYMBOL | -6 | | UNITS |
|-----------|-----|--------|-------|
| | MIN | MAX | |
| t_{AA} | | 30 | ns |
| t_{AR} | 45 | | ns |
| t_{ASC} | 0 | | ns |
| t_{ASR} | 0 | | ns |
| t_{CAC} | | 15 | ns |
| t_{CAH} | 10 | | ns |
| t_{CAS} | 15 | 10,000 | ns |
| t_{CLZ} | 3 | | ns |
| t_{CRP} | 10 | | ns |
| t_{CSH} | 60 | | ns |
| t_{OFF} | 3 | 15 | ns |

| SYMBOL | -6 | | UNITS |
|-----------|-----|--------|-------|
| | MIN | MAX | |
| t_{RAC} | | 60 | ns |
| t_{RAD} | 15 | | ns |
| t_{RAH} | 10 | | ns |
| t_{RAS} | 60 | 10,000 | ns |
| t_{RC} | 110 | | ns |
| t_{RCD} | 20 | | ns |
| t_{RCH} | 0 | | ns |
| t_{RCS} | 0 | | ns |
| t_{RP} | 40 | | ns |
| t_{RRH} | 0 | | ns |
| t_{RSH} | 15 | | ns |

EARLY WRITE CYCLE

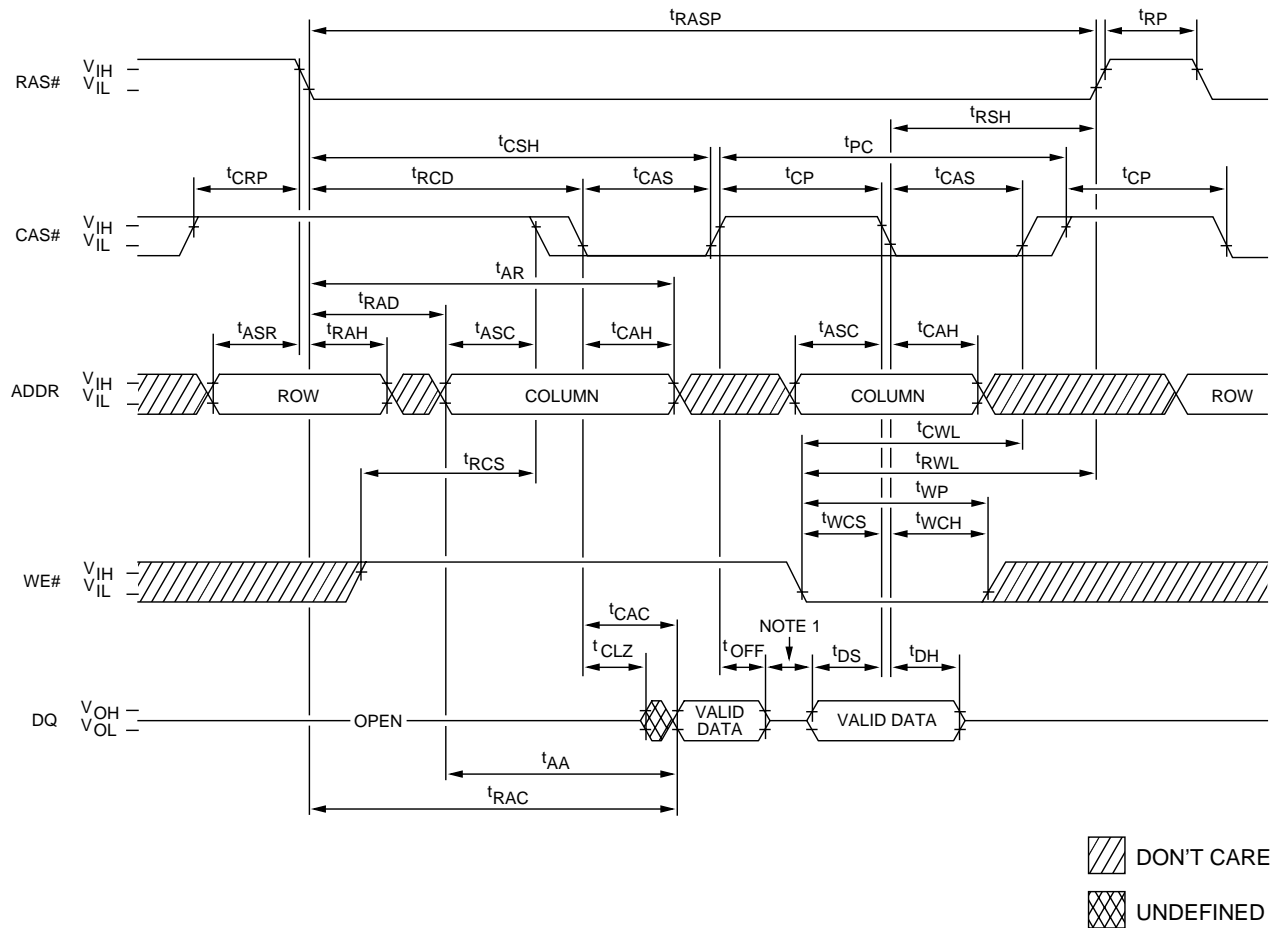


TIMING PARAMETERS

| SYMBOL | -6 | | UNITS |
|-----------|-----|--------|-------|
| | MIN | MAX | |
| t_{AR} | 45 | | ns |
| t_{ASC} | 0 | | ns |
| t_{ASR} | 0 | | ns |
| t_{CAH} | 10 | | ns |
| t_{CAS} | 15 | 10,000 | ns |
| t_{CRP} | 10 | | ns |
| t_{CSH} | 60 | | ns |
| t_{CWL} | 15 | | ns |
| t_{DH} | 10 | | ns |
| t_{DS} | 0 | | ns |
| t_{RAD} | 15 | | ns |

| SYMBOL | -6 | | UNITS |
|-----------|-----|--------|-------|
| | MIN | MAX | |
| t_{RAH} | 10 | | ns |
| t_{RAS} | 60 | 10,000 | ns |
| t_{RC} | 110 | | ns |
| t_{RCD} | 20 | | ns |
| t_{RP} | 40 | | ns |
| t_{RSH} | 15 | | ns |
| t_{RWL} | 15 | | ns |
| t_{WCH} | 10 | | ns |
| t_{WCR} | 45 | | ns |
| t_{WCS} | 0 | | ns |
| t_{WP} | 10 | | ns |

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



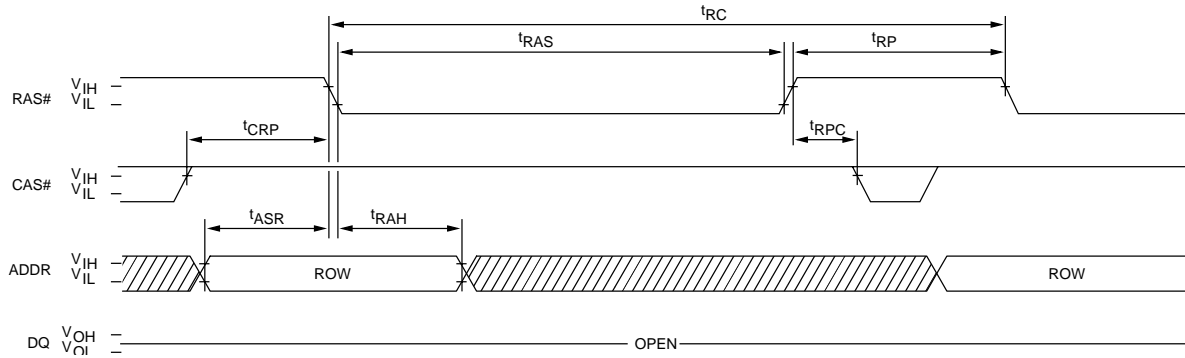
TIMING PARAMETERS

| SYMBOL | -6 | | UNITS |
|--------|-----|--------|-------|
| | MIN | MAX | |
| tAA | | 30 | ns |
| tAR | 45 | | ns |
| tASC | 0 | | ns |
| tASR | 0 | | ns |
| tCAC | | 15 | ns |
| tCAH | 10 | | ns |
| tCAS | 15 | 10,000 | ns |
| tCLZ | 3 | | ns |
| tCP | 10 | | ns |
| tCRP | 10 | | ns |
| tCSH | 60 | | ns |
| tCWL | 15 | | ns |
| tDH | 10 | | ns |
| tDS | 0 | | ns |

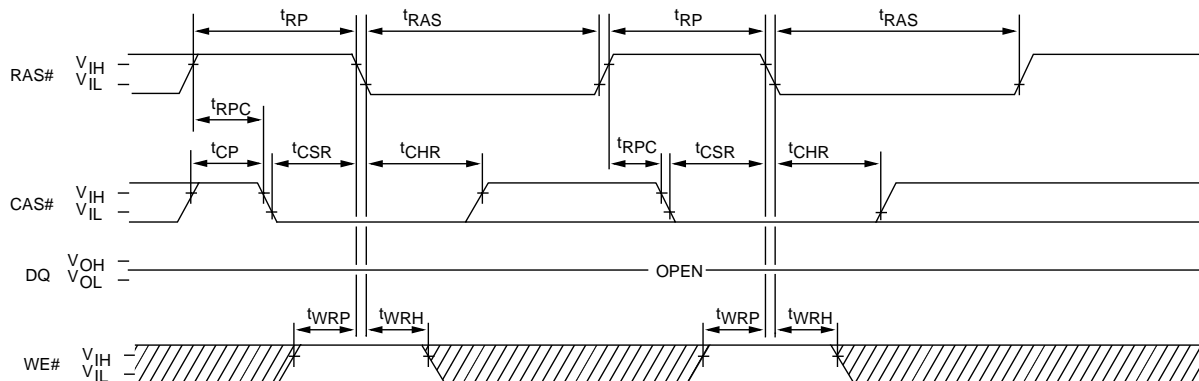
| SYMBOL | -6 | | UNITS |
|--------|-----|---------|-------|
| | MIN | MAX | |
| tOFF | 3 | 15 | ns |
| tPC | 35 | | ns |
| tRAC | | 60 | ns |
| tRAD | 15 | | ns |
| tRAH | 10 | | ns |
| tRASP | 60 | 125,000 | ns |
| tRCD | 20 | | ns |
| tRCS | 0 | | ns |
| tRP | 40 | | ns |
| tRSH | 15 | | ns |
| tRWL | 15 | | ns |
| tWCH | 10 | | ns |
| tWCS | 0 | | ns |
| tWP | 10 | | ns |

NOTE: 1. Do not drive data prior to tristate.

**RAS#-ONLY REFRESH CYCLE
(WE# = DON'T CARE)**



**CBR REFRESH CYCLE
(Addresses = DON'T CARE)**



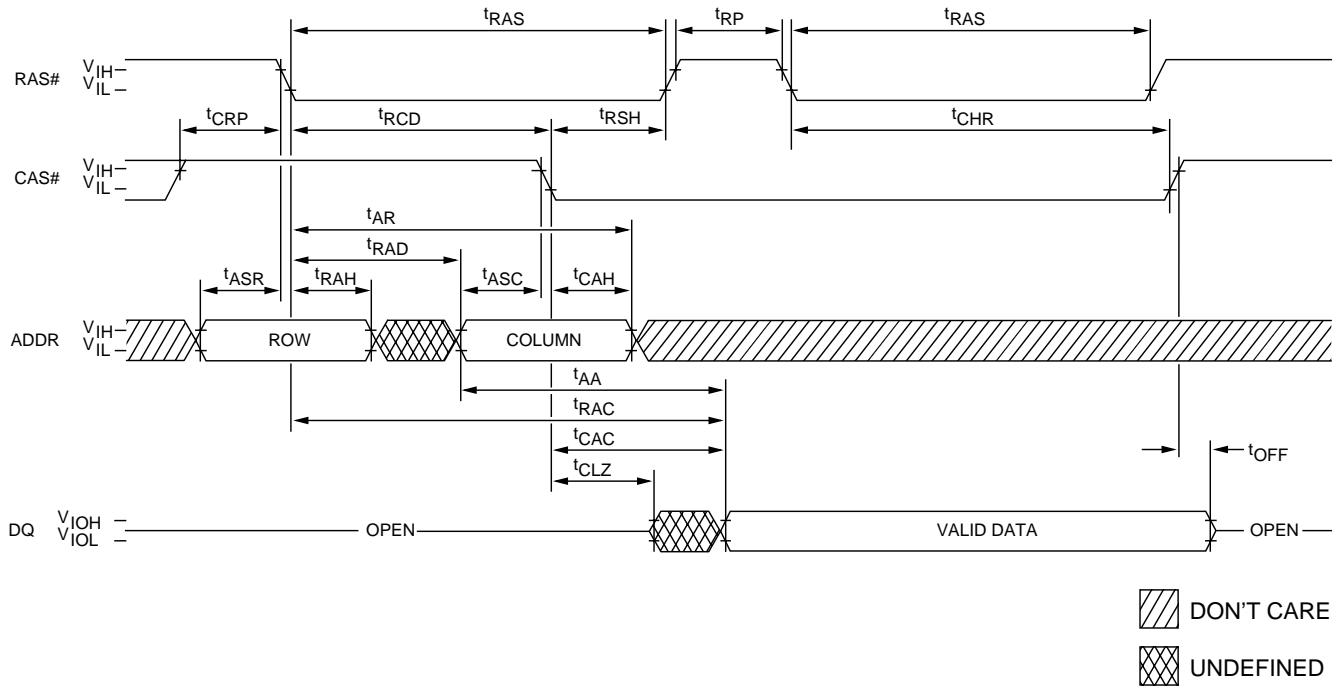
DON'T CARE
 UNDEFINED

TIMING PARAMETERS

| SYMBOL | -6 | | UNITS |
|------------------|-----|-----|-------|
| | MIN | MAX | |
| t _{ASR} | 0 | | ns |
| t _{CHR} | 15 | | ns |
| t _{CP} | 10 | | ns |
| t _{CRP} | 10 | | ns |
| t _{CSR} | 10 | | ns |
| t _{RAH} | 10 | | ns |

| SYMBOL | -6 | | UNITS |
|------------------|-----|--------|-------|
| | MIN | MAX | |
| t _{RAS} | 60 | 10,000 | ns |
| t _{RC} | 110 | | ns |
| t _{RP} | 40 | | ns |
| t _{RPC} | 0 | | ns |
| t _{WRH} | 10 | | ns |
| t _{WRP} | 10 | | ns |

HIDDEN REFRESH CYCLE²⁰
(WE# = HIGH)



TIMING PARAMETERS

| SYMBOL | -6 | | UNITS |
|------------------|-----|-----|-------|
| | MIN | MAX | |
| t _{AA} | | 30 | ns |
| t _{AR} | 45 | | ns |
| t _{ASC} | 0 | | ns |
| t _{ASR} | 0 | | ns |
| t _{CAC} | | 15 | ns |
| t _{CAH} | 10 | | ns |
| t _{CHR} | 15 | | ns |
| t _{CLZ} | 3 | | ns |
| t _{CRP} | 10 | | ns |

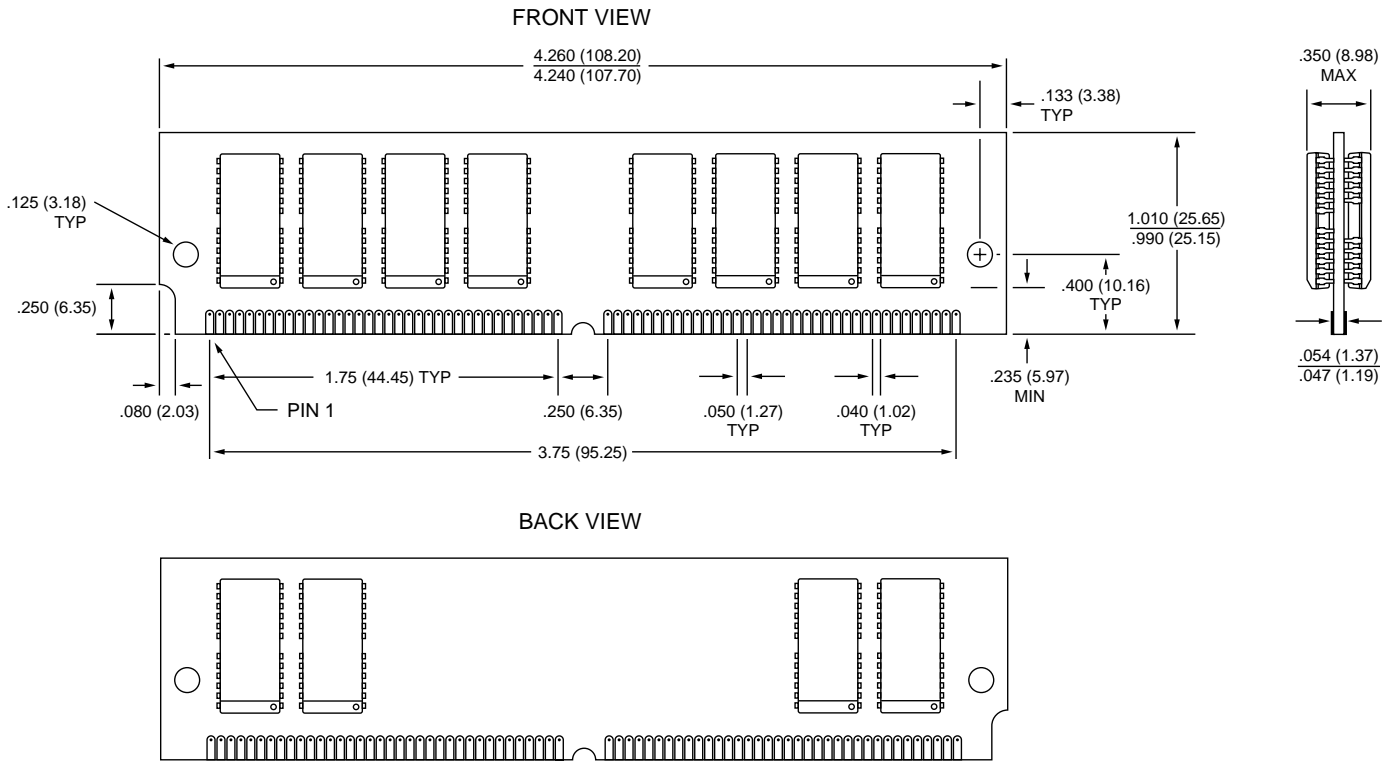
| SYMBOL | -6 | | UNITS |
|------------------|-----|--------|-------|
| | MIN | MAX | |
| t _{OFF} | 3 | 15 | ns |
| t _{RAC} | | 60 | ns |
| t _{RAD} | 15 | | ns |
| t _{RAH} | 10 | | ns |
| t _{RAS} | 60 | 10,000 | ns |
| t _{RCD} | 20 | | ns |
| t _{RP} | 40 | | ns |
| t _{RSH} | 15 | | ns |

OBSOLETE



4, 8 MEG x 36
PARITY DRAM SIMMs

72-Pin SIMM (32MB)



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.



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