SC1403
Mobile Multi-Output PWM Controller with Lossless Current Sense

Description

The SC1403 is a multiple-output power supply controller designed to power battery operated systems. The SC1403 provides synchronous buck converter control for two (3.3V and 5V) power supplies. An efficiency of 95% can be achieved for the two supplies. The SC1403 uses Semtech's proprietary Virtual Current Sense™ technology along with external error amplifier compensation to achieve enhanced stability and DC accuracy over a wide range of output filter components while maintaining fixed frequency operation. Lossless current sensing can be used to eliminate current sense resistors and reduce cost. The SC1403 also provides a 5V linear regulator for system housekeeping. The 5V linear regulator is derived from the battery; for improved efficiency, the output is switched to the 5V output when available.

Control functions include power-up sequencing, soft start, power-good signaling, and frequency synchronization. Line and load regulation is to +/-1%. The internal oscillator can be set to 200kHz, 300kHz, or synchronized to an external clock. The mosfet drivers provide >1A peak drive current for fast mosfet switching.

The SC1403 includes a PSAVE# input to select pulse skipping mode for high efficiency at light load, or fixed frequency mode for low noise operation.

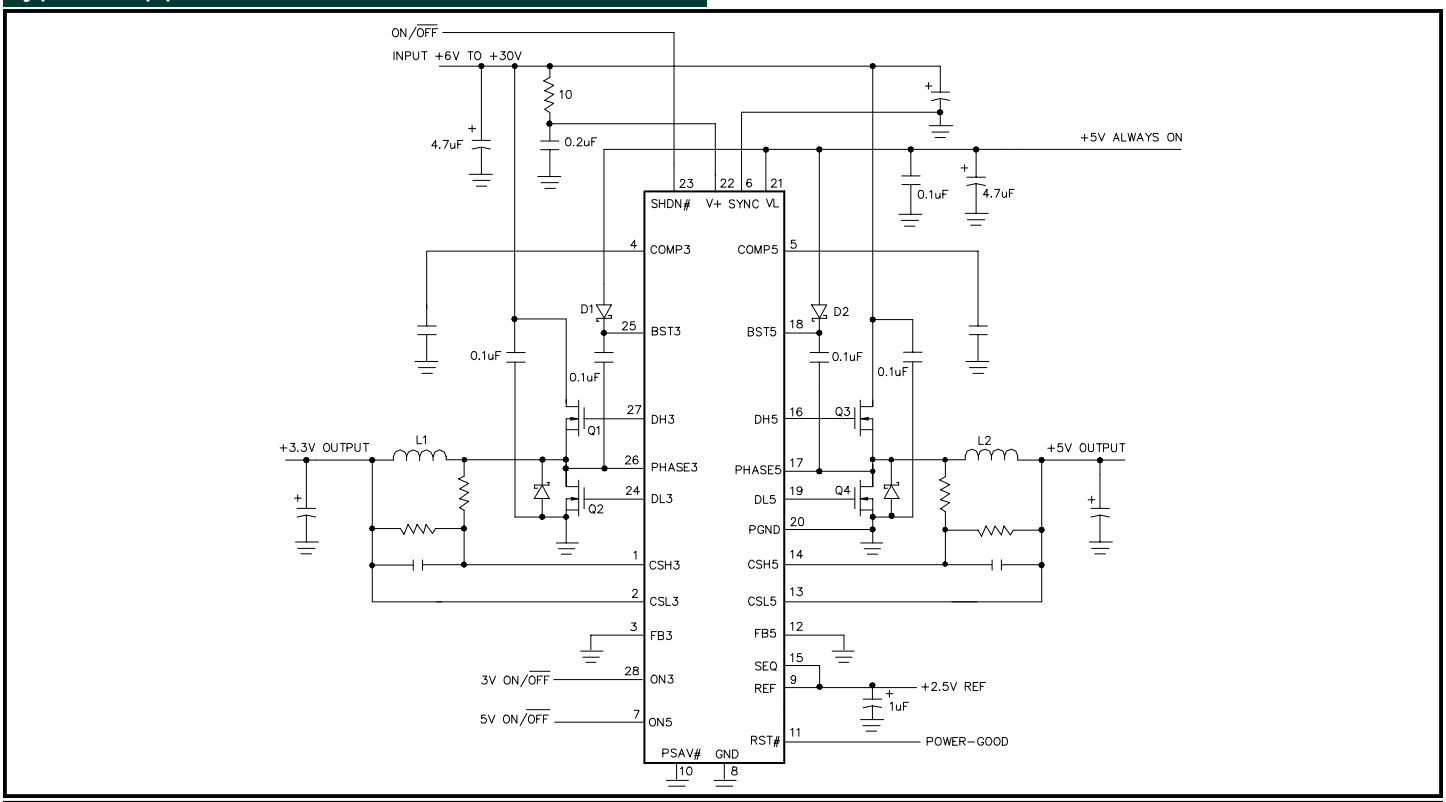
Features

- 3.3V and 5V dual synchronous outputs, resistor programmable to 2.5V
- Fixed frequency or PSAVE operation for maximum efficiency over wide load range
- 5V / 50mA linear regulator
- Virtual Current Sense™ for enhanced stability
- Lossless current limiting
- Out of phase switching reduces input capacitance
- External compensation supports wide range of output filter components
- Programmable power-up sequence
- Power Good output
- Output overvoltage and overcurrent protection with output undervoltage shutdown
- 6µA typical shutdown current
- 6mW typical quiescent power

Applications

- Notebook and subnotebook computers
- Tablet PCs
- Embedded applications

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

PARAMETER	DESCRIPTION	MAXIMUM	UNITS
VDD, V+, PHASE3, PHASE5 to GND	Supply and Phase Voltages	-0.3 to +30	V
PHASE3, PHASE5 to GND	Phase Voltages	-2.0 (transient - 100 nsec)	V
BST3, BST5, DH3, DH5 to GND	Boost voltages	-0.3 to +36	V
PGND to GND	Power Ground to Signal Ground	± 0.3	V
VL to GND	Logic Supply	-0.3 to +6	V
BST3 to PHASE3; BST5 to PHASE5;	High-side Gate Drive Supply	-0.3 to +6	V
DH3 to PHASE3; DH5 to PHASE5	High-side Gate Drive Outputs	-0.3 to (+BSTx + 0.3)	V
DL3, DL5 to GND CSL5, CSH5, CSL3, CSH3 to GND	Low-side Gate Drive Outputs and Current Sense inputs	-0.3 to +(VL + 0.3)	V
REF, SYNC, SEQ, PSAVE#, ON5, RESET#, VL, FB3, FB5, COMP3, COMP5 to GND	Logic inputs/outputs	-0.3 to +(VL + 0.3)	V
ON3, SHDN# to GND		-0.3 to +(V+ + 0.3V)	V
VL, REF Short to GND		Continuous	
REF Current		+5	mA
VL Current		+50	mA
T_J	Junction Temperature Range	+150	°C
Package Thermal Resistance	junction to ambient	76	°C/Watt
T_S	Storage Temperature Range	-65 to +200	°C
T_L	Lead Temperature	+300 °C, 10 second max.	°C

Electrical Characteristics

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
MAIN SMPS CONTROLLERS					
Input Voltage Range		6.0		30.0	V
FB3, FB5 range - Adjustable Mode	V+ = 6.0 to 30V, CSLx = FBx, Output Load = 0A to current limit	2.45	2.5	2.55	V
3.3V Output - Fixed Mode	V+ = 6.0 to 30V, FB3 = 0V, 3V Load = 0A to current limit	3.23	3.3	3.37	V
5V Output - Fixed Mode	V+ = 6.0 to 30V, FB5 = 0V, 5V Load = 0A to current limit	4.9	5.0	5.1	V
Output Voltage Adjust Range	Either SMPS	REF		5.5	V
Adjustable Mode Threshold	Measured at FB3/FB5	0.5	0.8	1.1	V
Load Regulation	Either SMPS, 0A to current limit		-0.4		%
Line Regulation	Either SMPS, 6.0V < V+ <30; PSAVE# = V_L		0.05		

Electrical Characteristics (Cont.)

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Thresholds (2)	CSH_X - CSL_X (positive current) CSH_X - CSL_X (negative current)	40	55 -50	70	mV
Zero Crossing Threshold	CSH_X - CSL_X PSAVE# = 0V, not tested		5		mV
Soft-Start Ramp Time	From enable to 95% full current limit, with respect to f_{OSC}		512		clks
Oscillator Frequency	SYNC = VL SYNC = 0V	220 170	300 200	380 230	kHz
Maximum Duty Factor	SYNC = VL SYNC = 0V	92 94	94 96		%
SYNC Input High Pulse	Not tested		300		ns
SYNC Input Low Pulse Width	Not tested		300		
SYNC Rise/Fall Time	Not tested		200		
SYNC Input Frequency Range			240 - 350		kHz
CSH3, CSH5 Input Leakage Current	CSH3 = 3.3V, CSH5 = 5.0V		3	10	µA
ERROR AMP					
DC Loop Gain	From internal feedback node to COMP3/COMP5		18		V/V
Gain Bandwidth Product			8		MHz
Output Resistance	COMP3, COMP5		25		Kohms
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	SHDN# = V+; 6V < V+ <30V, 0mA < I_{LOAD} < 30mA, ON3 = ON5 = 0V	4.6		5.25	V
VL Undervoltage Lockout Fault Threshold	Falling edge, hysteresis = 0.7V	3.5	3.7	4.1	
VL Switchover Lockout	Switchover at startup - rising edge		4.5		
REF Output Voltage	No external load	2.45	2.5	2.55	
REF Load Regulation	0µA < I_{LOAD} < 50µA			12.5	mV
	0mA < I_{LOAD} < 5mA			50	

Electrical Characteristics (Cont.)

Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A =-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
REF Sink Current	10mV rise in REF		10		µA
REF Fault Lockout Voltage	Falling edge	1.8		2.2	V
V+ Operating Supply Current	VL switched over to VOUT5, both SMPS on, lLoad3 = 0A, lLoad5 = 0A		10	50	µA
V+ Standby Supply Current	V+ = 6V to 30V, SMPS off, includes current into SHDN#		300		
V+ Shutdown Supply Current	V+ = 6V to 30V, SHDN# = 0V	-1	3	15	
Quiescent Power Consumption	SMPS enabled, FB3 = FB5 = 0V, No Load on SMPS		6		mW
FAULT DETECTION					
Overvoltage Trip Threshold	With respect to unloaded output voltage	7	11	15	%
Overvoltage-Fault Propagation Delay	Output driven 2% above overvoltage trip V_{TH}		1.5		µs
Output Undervoltage Threshold	With respect to unloaded output voltage	65	75	85	%
Output Undervoltage Lockout Time	From each SMPS enabled, with respect to f_{OSC}	5000	6144	7000	clks
Thermal Shutdown Threshold	Typical hysteresis = +10°C		150		°C
RESET#					
RESET# Trip Threshold	With respect to unloaded output voltage, falling edge; typical hysteresis = 1%	-12	-9	-5	%
RESET# Propagation Delay	Falling edge, output driven 2% below RESET# trip threshold		1.5		µs
RESET# Delay Time	With respect to f_{OSC}	27,000	32,000	37,000	clks
INPUTS AND OUTPUTS					
Feedback Input Leakage Current	FB3, FB5 = 2.6V	-1		1	µA
Logic Input Low Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)			0.6	V
Logic Input High Voltage	ON3, PSAVE#, ON5, SHDN#, SYNC (SEQ = REF)	2.4			V

Electrical Characteristics (Cont.)

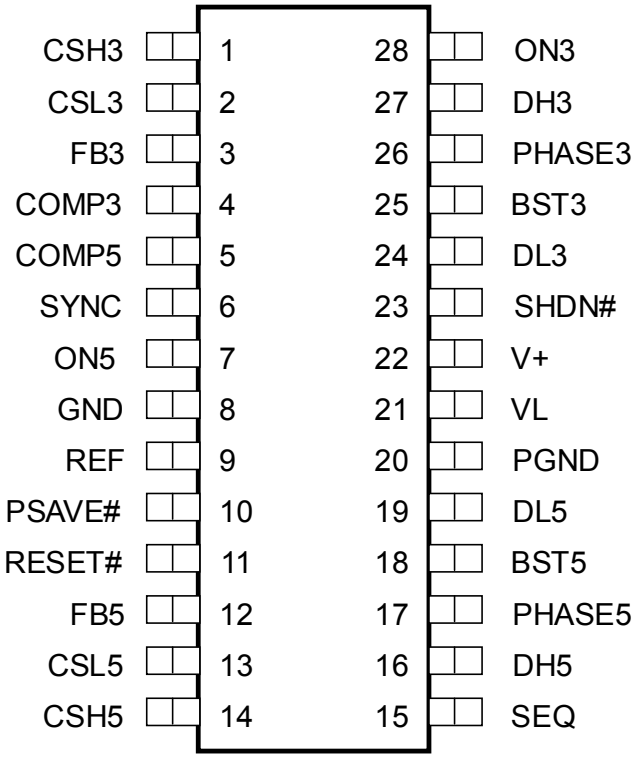
Unless otherwise noted: V+ = 15V, both PWMs on, SYNC = 0V, VL load = 0mA, REF load = 0mA, PSAVE# = 0V, T_A=-40 to 85°C. Typical values are at T_A = +25°C. Circuit = Typical Application Circuit

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current PSAVE#, ON5, SYNC	SEQ = REF	 -1		 1	 µA
ON3 Input Leakage Current	ON3 = 15V	-2		2	
SHDN# Input Leakage Current	SHDN# = 15V	-1	3	10	µA
Logic Output Low Voltage	RESET#, ISINK = 4mA			0.4	V
Logic Output High Current	RESET# = 3.5V		1		mA
ON5 Pull-down Resistance	ON5, RUN/ON3 = 0V, (SEQ = REF)		100		ohms
Gate Driver Sink/Source Current	DL3, DH3, DL5, DH5, forced to 2.5V		1		A
Gate Driver On-Resistance	BST3 to DH3, DH3 to PHASE3, BST5 to DH5, DH5 to PHASE5, VL to DL3, DL3 to PGND, VL to DL5, DL5 to PGND		1.5	7	ohms
Non-Overlap Threshold	PHASE3, PHASE5, DL3, or DL5		1.0		V
Shoot-through Delay	DHx falling edge to DLx rising edge DLx falling edge to DHz rising edge (1V threshold on DHx and DLx, no external capacitance on DLx/DHx.)	10 35	17 75	25 115	nsec

Note:
(1) This device is ESD sensitive. Use of standard ESD handling procedures required.
(2) Applicable for T_A = 0 to +85°C

Pin Configuration

TOP VIEW



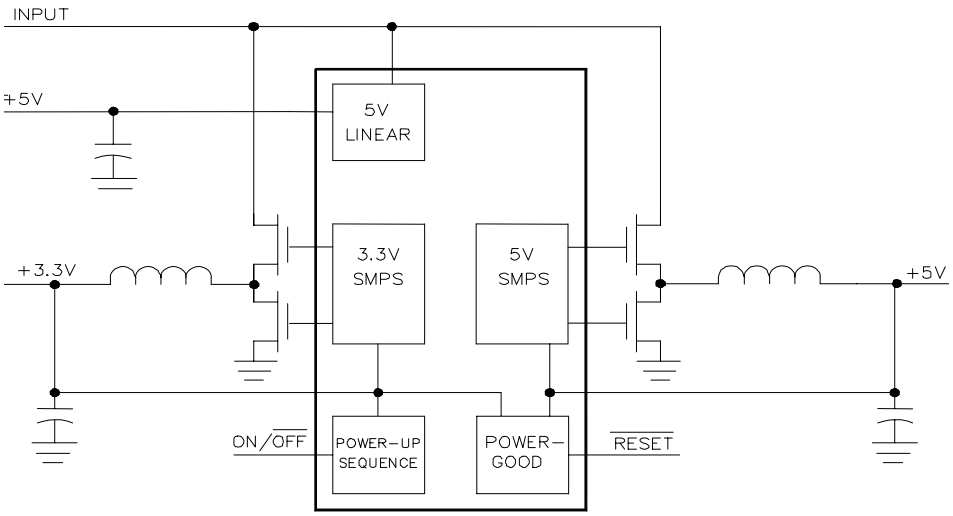
(28 Pin TSSOP)

Ordering Information

Device	Package	Temp. (T_A)
SC1403ITSTR	TSSOP-28	-40 - +85°C
SC1403ITSTRT	TSSOP-28 Lead-free option	-40 - +85°C

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Block Diagram



Pin Descriptions

Pin #	Pin Name	Pin Function
1	CSH3	High-side current sense input for 3.3V SMPS. Connect to the high side of the DCR RC network, or to the inductor side of a current sense resistor.
2	CSL3	Low side current sense input for 3.3V SMPS. For adjustable mode operation, connect to the 3.3V output, at either the low side of the DCR RC network, or the output side of a current sense resistor. For fixed-output operation, FB3 is grounded, and CSL3 also operates as the feedback sense input for the 3.3V SMPS.
3	FB3	Feedback Input for the 3.3V SMPS. In adjustable mode (using external feedback resistors), FB3 regulates to REF (2.5V). When FB3 is grounded, internal resistors set a fixed 3.3V output.
4	COMP3	Compensation output of the 3.3V error amplifier.
5	COMP5	Compensation output of the 5.0V error amplifier.
6	SYNC	Oscillator Synchronization and Frequency Select. Tie to VL for 300kHz operation; tie to GND for 200kHz. Drive externally to synchronize between 240kHz and 350kHz.
7	ON5	5V ON/OFF Control Input. Connect a 1K - 10K ohm resistor in series with ON5 to allow 5V shutdown.
8	GND	Low noise Analog Ground and Feedback reference point.
9	REF	2.5V Reference Voltage Output. Bypass to GND with 1 µF minimum.
10	PSAVE#	Logic Control Input that disables PSAVE Mode when high. Connect to GND for normal use.
11	RESET#	Active Low Timed Reset Output. RESET# swings GND to VL. Goes high after a fixed 32,000 clock cycle delay following a successful power up.
12	FB5	Feedback Input for the 5V SMPS. In adjustable mode (using external feedback resistors), FB3 regulates to REF (2.5V). When FB5 is grounded, internal resistors set a fixed 5V output.
13	CSL5	Low side current sense input for 5V SMPS. For adjustable mode operation, connect to the 5V output, at either the low side of the DCR RC network, or the output side of a current sense resistor. For fixed-output operation, FB5 is grounded, and CSL5 also operates as the feedback sense input for the 5V SMPS.
14	CSH5	High-side current sense input for 5V SMPS. Connect to the high side of the DCR RC network, or to the inductor side of a current sense resistor.
15	SEQ	Input that selects SMPS sequence for RESET#.
16	DH5	Gate Drive Output for the 5V, high side N-Channel switch.
17	PHASE5	5V SMPS Switching Node (inductor) connection.
18	BST5	Boost capacitor connection for 5V high side gate drive.

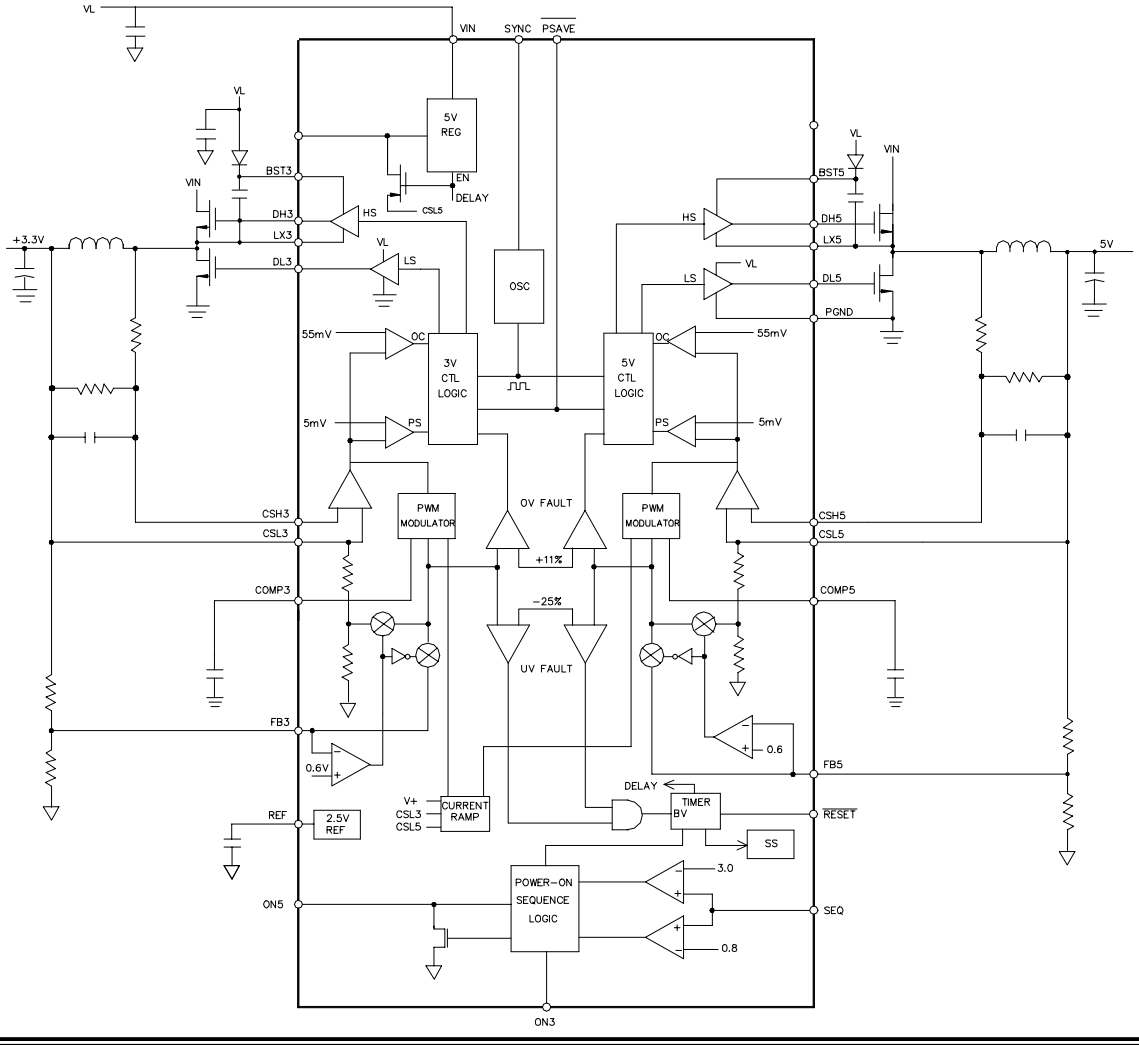
Note: All logic level inputs and outputs are open collector TTL compatible.

Pin Descriptions (Cont.)

Pin #	Pin Name	Pin Function
19	DL5	Gate Drive Output for the 5V low side synchronous rectifier MOSFET.
20	PGND	Power Ground.
21	VL	5V Internal Linear Regulator Output. For improved efficiency, VL connects to 5V SMPS output when 5V SMPS is enabled.
22	V+	Battery Voltage Input.
23	SHDN#	Shutdown Control Input, active low.
24	DL3	Gate Drive Output for the 3.3V low side synchronous rectifier MOSFET.
25	BST3	Boost Capacitor Connection for 3.3V high side gate drive.
26	PHASE3	3.3V Switching Node (inductor) Connection.
27	DH3	Gate Drive Output for the 3.3V, high side N-Channel switch.
28	ON3	3.3V ON/OFF Control Input.

Note: All logic level inputs and outputs are open collector TTL compatible.

Block Diagram



Functional Information

Detailed Description

The SC1403 is a versatile multiple-output power supply controller designed to power battery operated systems. The SC1403 provides synchronous rectified buck control in fixed frequency forced-continuous mode and hysteretic PSAVE mode, for two switching power supplies over a wide load range. Out of phase switching improves signal quality and reduces input RMS current, therefore reducing size of input filter inductors and capacitors. Lossless current sensing eliminates the need for discrete current sense resistors. The two switchers have on-chip preset output voltages of 5.0V and 3.3V. An external resistor divider can be used to set the switcher outputs from 2.5V to 5.5V. The control circuitry for each PWM controller includes digital softstart, voltage error amplifier with built-in slope compensation, pulse width modulator, power save, overcurrent, overvoltage and undervoltage fault protection. One linear regulator and a precision reference voltage are also provided. The 5V/30mA linear regulator uses battery power to feed the gate drivers; for improved efficiency the 5V switcher output is used instead when available. Semtech's proprietary Virtual Current Sense™ provides greater advantages in the aspect of stability and signal-to-noise ratio than the conventional current sense method.

PWM Control

There are two separate PWM control blocks for each switcher. They are switched out-of-phase with each other. The interleaved topology reduces steady state input filter requirements by reducing current drawn from the filter capacitors. To avoid both switchers switching at the same instance, there is a built-in delay between the turn-on of the 3.3V switcher and 5V switcher, the amount of which depends on the input voltage (see Out-of-Phase Switching).

The PWM provides two modes of control over the entire load range. The SC1403 operates in forced continuous conduction mode as a fixed frequency peak current mode controller with falling edge modulation. Current sense is done differently than in conventional peak current mode control. Semtech's proprietary Virtual Current Sense™ emulates the necessary inductor current information for proper functioning of the IC. In order to accommodate a wide range of output filters, a COMP pin is also available for compensating the error amplifier externally. A nominal gain of 18 is used in the error amplifier to further improve the system loop gain response and the output transient behavior.

When the switcher is operating in continuous conduction mode, the high-side mosfet is turned on at the start of each switching cycle. It is turned off when the desired duty cycle is reached. Active shoot-through protection delays the turn-on of the lower mosfet until the phase node drops below 1V. The low-side mosfet remains on until the beginning of the next switching cycle. Again, active shoot-through protection ensures that the gate to the low-side mosfet has dropped low before the high-side mosfet turns on.

Under light load conditions when the PSAVE# pin is low, the SC1403 operates as a hysteretic controller in the discontinuous conduction mode to reduce its switching frequency and switching bias current. The switching of the output mosfet does not depend on a given oscillator frequency, but on the hysteretic feedback voltage set around the reference. When entering PSAVE# mode, if the minimum (valley) inductor current measured across the CSH and CSL pins is below the PSAVE# threshold for four switching cycles, the virtual current sensing circuitry is shutdown and PWM switches from forced continuous to hysteretic mode. If the minimum (valley) inductor current is above the threshold for four switching cycles, PWM control changes from hysteretic to forced continuous mode. The SC1403 provides built-in hysteresis to inhibit chattering between the two modes of operation.

Gate Drive / Control

The gate drivers on the SC1403 are designed to switch large mosfets up to 350kHz. The high-side gate driver is required to drive the gates of high-side mosfet above the V+ input. The supply for the gate drivers is generated by charging a boostrap capacitor from the VL supply when the low-side driver is on. Monitoring circuitry ensures that the bootstrap capacitor is charged when coming out of shutdown or fault conditions where the bootstrap capacitor may be depleted. In continuous conduction mode, the low-side driver output that controls the synchronous rectifier in the power stage is on when the high-side driver is off. Under light load conditions when PSAVE# pin is low, the inductor ripple current will approach the point where it reverses polarity. This is detected by the low-side driver control and the synchronous rectifier is turned off before the current reverses, preventing energy drain from the output. The low-side driver operation is also affected by various fault conditions as described in the Fault Protection section.

Internal Bias Supply

The VL linear regulator provides a 5V output used to power the gate drivers, 2.5V reference and internal control section of the SC1403. The regulator is capable of supplying up to 30mA (including mosfet gate charge current). The VL pin should be bypassed to GND with 4.7uF to supply the peak current requirements of the gate driver outputs.

The regulator receives its input power from the V+ battery input. Efficiency is improved by providing a boot-strapping mode for the VL bias. When the 5V SMPS output voltage reaches 5V, internal circuitry turns on a pmos pass device between CSL5 and VL. The internal VL regulator is then disabled and VL bias is provided by the high efficiency 5V switcher.

The REF output is accurate to +/- 2% over temperature. It is capable of delivering 5mA max and should be bypassed with 1uF minimum capacitor. Loading the REF pin will reduce the REF voltage slightly as shown in the following table.

Functional Information (Cont.)

Loading Resistance (ohm)	511	2.67K	49.9K	255K	1Meg
Vref Deviation	8.3mV	3.1mV	0.5mV	0.3mV	0mV

Current Sense (CSH, CSL)

Output current of each supply is sensed as the voltage between the CSH and CSL pins. Overcurrent is detected when the current sense voltage exceeds +55/-50 mV typical. A positive overcurrent turns off the high-side driver, a negative overcurrent turns off the low-side driver; each on a cycle-by-cycle basis. Output current can be sensed by DCR (lossless) sensing, or optionally with a current-sense resistor; see Applications Information.

Oscillator

When the SYNC pin is high the oscillator runs at 300kHz; when SYNC is low the frequency is 200kHz. The oscillator can be synchronized to the falling edge of a clock on the SYNC pin with a frequency between 240kHz and 350kHz. In general, 200kHz operation provides highest efficiency, while 300kHz is used to obtain smaller output ripple and/or smaller filter components.

Fault Protection

In addition to cycle-by-cycle current limit, the SC1403 provides overtemperature, output overvoltage, and undervoltage protection. Overtemperature protection will shut the device down if die temperature exceeds 150°C, with 10°C hysteresis.

If either SMPS output is more than 10% above its nominal value, both SMPS are latched off and the low side mosfets are latched on. To prevent the output from ringing below ground in a fault condition, a 1A Schottky diode should be placed across each output.

Two different levels of undervoltage (UV) are detected. If the output falls 9% below its nominal value, the RESET# output is pulled low. If the output falls 25% below its nominal value, both SMPS are latched off.

Both of the latched faults (OVP and UV) persist until SHDN or ON3 is toggled, or the V+ input is brought below 1V.

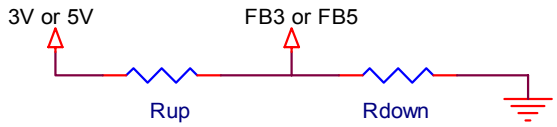
Shutdown and Operating Modes

Holding the SHDN pin low disables the SC1403, reducing the V+ input current to less than 10uA. When SHDN is high, the part enters standby mode where the VL regulator and VREF are enabled. Turning on either SMPS will put the SC1403 in run mode.

SHDN	ON3	ON5	MODE	DESCRIPTION
Low	X	X	Shut-down	Minimum bias current
High	Low	Low	Standby	VREF and VL regulator enable
High	High	High	Run Mode	Both SMPS Running

Output Voltage Selection

If FBx is grounded, internal resistors determine 3.3V and/or 5V output voltages. In adjustable mode, the internal resistors are disabled and the output is determined by external resistors, based on 2.5V regulated at the FB pin. The output voltage is determined according the following formula. Rdown should not exceed 10 Kohms.



$$Vout = 2.5 \cdot \left(1 + \frac{Rup}{Rdown}\right)$$

Power up Controls and Soft Start

The user controls the SC1403 RESET# through the SEQ, ON3 and ON5 pins, as shown in the Startup Sequence Chart. At startup, RESET# is held low for 32K switching cycles, and then RESET# is determined by the output voltages and the SEQ pin.

To prevent surge currents at startup, each SMPS has a counter and DAC to incrementally raise the current limit (CSH-CSL voltage). The current limit follows discrete steps of typically 25%, 40%, 60%, 80%, and 100%, each step lasting 128 clock cycles. To charge up the output capacitors, inductor current at startup must exceed load current. When the output voltage reaches it's nominal value the SMPS will reduce duty cycle, but the excess LI^2 energy of the inductor must flow into the load and output capacitors. If the output capacitor is relatively small, the peak output voltage can approach the overvoltage trip point. To prevent nuisance OVP at startup, the inductance and capacitance must meet the following criteria:

$$\frac{L_{MAX}}{C_{MIN}} \le \frac{V_{O\_NOM}^2}{IL_{MAX\_OC}^2} \cdot 1.59$$

IL_{MAX_OC} is the maximum inductor current set by the current-limit components, and V_{O_NOM} is the nominal output voltage.

Functional Information (Cont.)

Startup Sequence Chart

SEQ	ON3	ON5	RESET	DESCRIPTION
REF	LOW	LOW	Follows 3.3V SMPS.	Independant start control mode. Both SMPSs off.
REF	LOW	HIGH	Low.	5V SMPS ON, 3.3V SMPS OFF.
REF	HIGH	LOW	Follows 3.3V SMPS.	3.3V SMPS ON, 5V SMPS OFF.
REF	HIGH	HIGH	Follows 3.3V SMPS.	Both SMPSs on.
GND	LOW	X	Low.	Both SMPSs off.
GND	HIGH	HIGH/LOW	High after both outputs are in regulation.	5V starts when ON3 goes high. If ON5 = HIGH, 3V is on. If ON5 = LOW, 3V is off.
VL	LOW	X	Low.	Both SMPSs off.
VL	HIGH	HIGH/LOW	High after both outputs are in regulation.	3V starts when ON3 goes high. If ON5 = HIGH, 5V is on. If ON5 = LOW, 5V is off.

Applications Information

Reference Circuit Design

The schematic for the reference circuit is shown on page 27. The reference circuit is configured as follows:

Switching Regulator 1	Vout1 = 3.3V @ 6A
Switching Regulator 2	Vout2 = 5.0V @ 6A
Linear Regulator	Vout3 = 5.0V @ 50mA
Input voltage	Vin = 7 to 21V

Designing the Output Filter

Before calculating the filter inductance and capacitance, an acceptable inductor ripple current is determined. Maximum allowable ripple depends on the transient requirements. Ripple current is usually set at 10% to 20% of the maximum load. However, increasing the ripple current allows for a smaller inductor and will also quicken the output transient response. In this example, we set the ripple current to be 25% of maximum load.

$$\Delta Io = 25\% \times 6A = 1.5A$$

The inductance is found from ripple current, frequency, input voltage, and output voltage. Minimum required inductance is found at maximum Vin, where ripple current is the greatest.

$$Lmin = Vo \times \frac{(1 - Vo / Vin)}{F \times \Delta Io} = 6.18uH$$

The next standard value is 6.8uH. For the reference design, the Coiltronics DR127-6R8 is used.

To specify the output capacitance, the allowable output ripple voltage must be determined. Output ripple is often specified at 1% of the output voltage. For the 3.3V output, we selected a maximum ripple voltage of 33mVp-p. The maximum allowable ESR would then be:

$$ESR_{MAX} = \Delta Vo / \Delta Io = 33mV / 1.5A = 22m\Omega$$

Panasonic SP Polymer Aluminum capacitors are a good choice. For this design, use one 180uF, 4V device, with ESR of 15mΩ.

The output capacitor must support the inductor RMS ripple current. To check the actual ripple versus the capacitor's RMS rating:

$$I_{RMS\_actual} = \frac{\Delta Io}{\sqrt{12}} = \frac{1.5A}{\sqrt{12}} = 0.43A$$

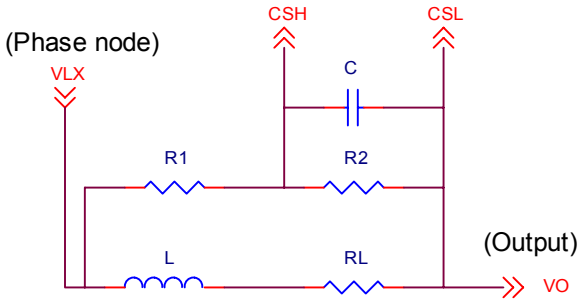
This is much less than the capacitor's ripple rating of 3.3A.

Choosing Current Sense Components

Since the SC1403 implements Virtual Current Sense™, current sensing is not required for the control loop. But it is required for cycle-by-cycle current limit and for startup. Cycle-by-cycle current limit is reached when the voltage of CSH-CSL exceeds 55mV nominal. Depending on the system requirement, this current limit can vary, but it is typically 10% to 30% higher than the maximum load.

This design uses the DC resistance of the inductor as a current sense element, which eliminates the cost and space required for a separate current sense resistor. Below is a typical DCR application circuit. The inductor is shown along with it's wiring resistance RL. In place of the current sense resistor are C, R2, and R1, which are connected across the inductor terminals.

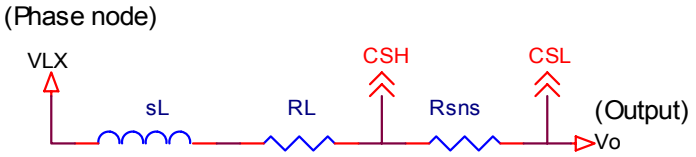
Applications Information (Cont.)



The equation for the current sense signal, CSH - CSL, is given by:

$$V_{(CSH-CSL)} = (V_{LX} - V_o) \cdot \frac{R2}{R2 + R1 + sC \cdot R2 \cdot R1} \quad (EQ1)$$

where (V_{LX} - Vo) is the voltage across the inductor terminals. The values for C, R2, and R1 can be found by comparing the above circuit with resistive sensing, which is shown below.



With resistive sensing, the current sense signal CSH-CSL can be written in the complex s-domain as:

$$V_{(CSH-CSL)} = (V_{LX} - V_o) \cdot \frac{Rsns}{Rsns + RL + sL} \quad (EQ2)$$

where (V_{LX} - Vo) is the voltage across the inductor terminals. Note the similarity between EQ 1 and EQ 2. By choosing proper values for C, R1, and R2, the current-sense voltage (CSH-CSL) will track the inductor current.
The following equations determine C, R1, and R2:

$$R1 = \frac{L \cdot ILpk}{C \cdot 55mV}$$

$$R2 = R1 \cdot \frac{55mV}{(ILpk \cdot RL - 55mV)}$$

The recommended value for C is 1.0uF. RL inductor resistance is specified at 11.6 mohm typical. 55mV is the current sense threshold. For the reference design, the values are set to C = 1uF and R1 = R2 = 1.3K. This sets the current limit to approximately 10A.

Two guidelines must be used when selecting C, R1, and R2:

The values of R2 and R1 should not exceed approximately 1.5Kohm. The bias current from the CSH input flows through these resistors and creates an error term.

The value for R1 should not be too small due to power considerations. During a switching cycle, the voltage across R1 is either (Vin - Vo) or (-Vo). This creates a power loss in R1: the power loss can be determined by:

$$P_{R1} = \frac{Vo \cdot (Vin - Vo)}{R1} = \frac{3.3 \cdot (21 - 3.3)}{1.3k\Omega} = 45\ mW$$

Choosing the Main Switching mosfet

The IRF7143 is used in the reference design. Before choosing the main (high-side) mosfet, we need to check three parameters: voltage, power, and current rating.

The maximum drain to source voltage of the mosfet is mainly determined by the switcher topology. Since this is a buck topology,

$$V_{DS\_MAX} = V_{IN\_MAX} = 21V$$

The IRF7413 is a 30V device, which allows for 70% derating at 21V operation.

The mosfet power dissipation has three components: conduction losses, switching losses, and gate drive losses. The conduction loss is determined using the RMS mosfet current; the equation is shown below. The mosfet current is a trapezoid waveform with values equal to:

$$I_{MIN} = I_{LOAD} - \frac{\Delta I_L}{2} \qquad I_{MAX} = I_{LOAD} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = \frac{Vo \cdot (1-D)}{fs \cdot L} \qquad D = \frac{Vo}{Vin}$$

$$I_{RMS} = \sqrt{D \cdot (I_{MIN}^2 + I_{MIN} \cdot I_{MAX} + I_{MAX}^2)}$$

As input voltage decreases, the duty cycle increases and the ripple current decrease, and overall the RMS mosfet current will increase. The conduction losses are then given by the formula below, where Rds(on) is 18m-ohm for the IRF7413 at room temperature. Note that Rds(on) increases with temperature.

$$P_{CONDUCTION} = R_{ds(on)} \cdot I_{RMS}^2$$

The mosfet switching loss is estimated according to:

$$P_{SWITCHING} = \frac{C_{RSS} \cdot V_{IN}^2 \cdot fs \cdot I_{OUT}}{I_G}$$

Crss is the reverse transfer capacitance of the mosfet, which is 240pF for IRF7413. Ig is the gate driver current, which is 1A for SC1403.

The mosfet gate drive loss is estimated from:

Applications Information (Cont.)

$$P_{GATE} = \frac{1}{2} \cdot C_G \cdot V^2 \cdot f_S$$

Cg is the effective gate capacitance, equal to the Total Gate Charge divided by VGS from the vendor datasheet, and is 7.9nF for the IRF7413. V in the above formula is the final gate-source voltage on the mosfet, 5V for the SC1403.

The total mosfet losses is the sum of the three loss components.

$$P_{TOTAL\_DISS} = P_{CONDUCTION} + P_{SWITCHING} + P_{GATE}$$

The mosfet dissipation under conditions of 15V input, 6A load, and ambient temperature of 25C, can be determined as:

DNOM = 0.22 ΔIL = 1.26A
IMIN = 5.37A IMAX = 6.63A IRMS = 4.88A

Rds(on) (100C) = 18 mohm
PCONDUCTION = 429mW

· PSWITCHING = 97mW PGATE = 30mW

PTOTAL_DISS = 429 + 97 + 30 = 556 mW

The junction temperature rise resulting from the power dissipation is calculated as:

$$\Delta T_J = P_T \cdot \theta_{JA}$$

P_T is the total device dissipation, and θ_{JA} is the package thermal resistance, which is 50°C/W for the IRf7413. The junction temperature rise is then:

ΔT_J = 0.556W · 50°C/W = 27.8°

This is a modest temperature rise, so no special heat sinking is required when laying out the mosfet.

Applications Information (Cont.)

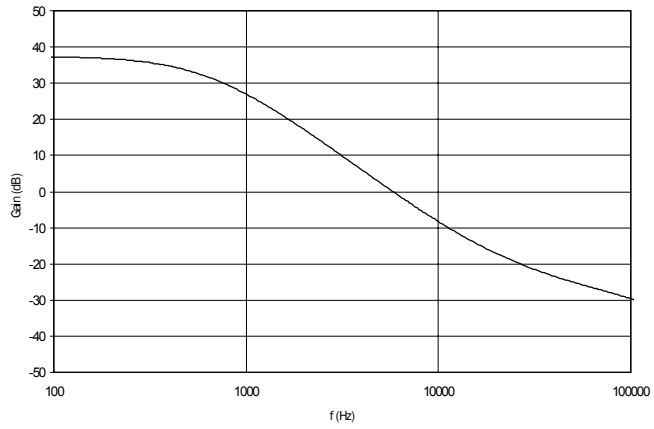
Designing the Loop

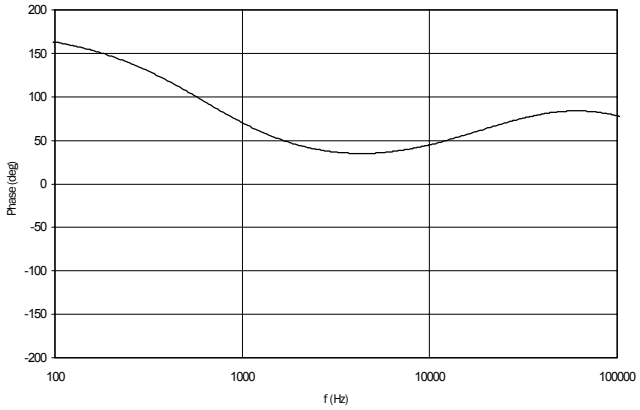
There are two aspects concerning the loop design. One is the power train design and the other is the external compensation design. A good loop design is a combination of the two. In the SC1403, the control-to-output/power train response is dominated by the load impedance, the effective current sense resistor, output capacitance, and the ESR of the output caps. The low frequency gain is dominated by the output load impedance and the effective current sense resistor. Inherent to Virtual Current Sense™, there is one additional low frequency pole sitting between 100Hz and 1kHz and a zero between 15kHz and 25kHz. To compensate for the SC1403 is easy since the output of error amplifier COMP pin is available for external compensation. A traditional pole-zero-pole compensation is not necessary in the design using SC1403. To ensure high phase margin at crossover frequency while minimizing the component count, a simple high frequency pole is usually sufficient. In the reference design below, single-pole compensation method is demonstrated. And the loop measurement results are compared to those obtained from the simulation model. Transient response is also done to validate the model. Also, to help speed up the design process, a list of recommended output caps vs compensation caps value is given in table I.

Single-Pole Compensation Method

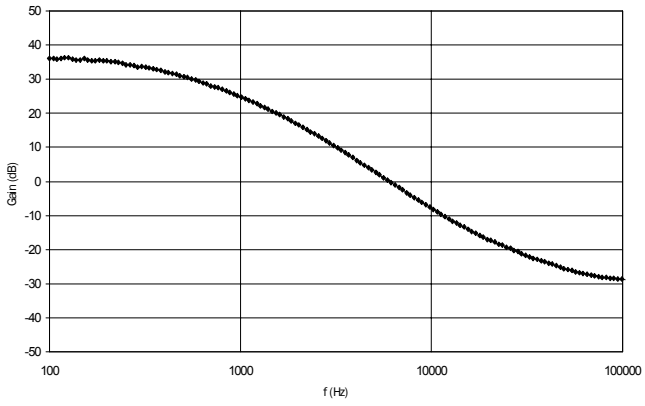
Given parameters:
Vin = 19V, Vout = 3.3V @ 2.2A,
Output impedance, Ro = 3.3V/2.2A = 1.5 Ω ,
Panasonic SP cap, Co = 180uF, Resr = 15 mΩ ,
Output inductor, Lo = 4.7uH
Switching frequency, Fs = 300kHz

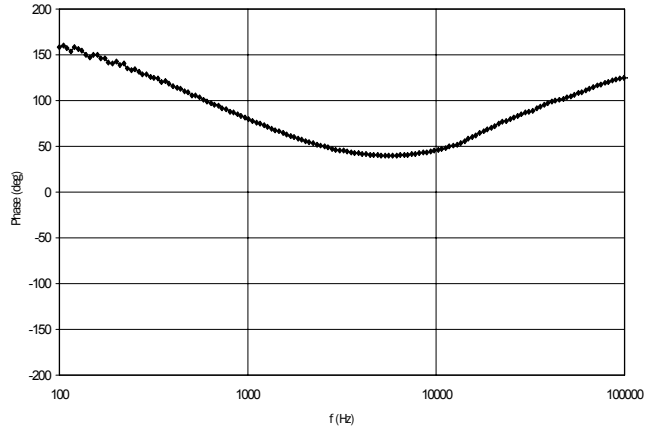
Simulated Control-to-Output gain & phase response (up to 100kHz) is plotted below.





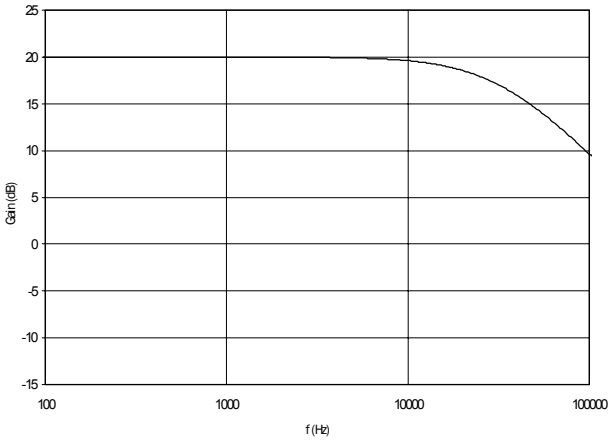
Measured Control-to-Output gain & phase response (up to 100kHz) is plotted below.

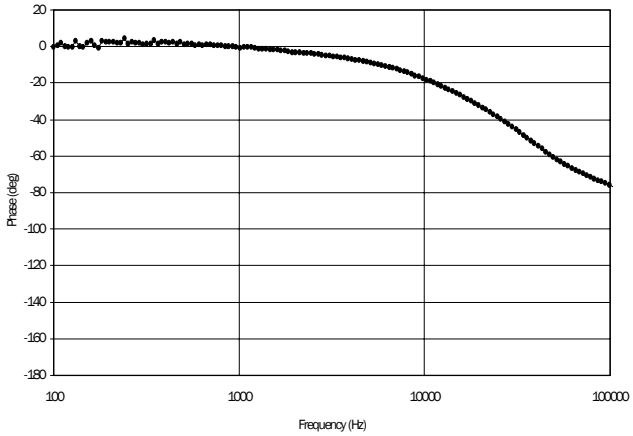




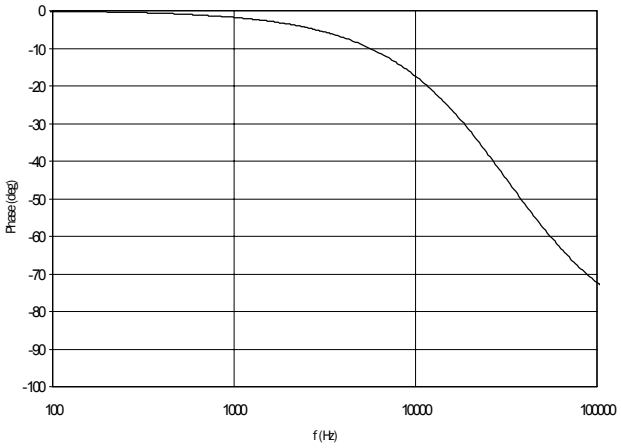
Single-pole compensation of the error amplifier is achieved by connecting a 100pF capacitor from the COMP pin of the SC1403 to ground. The simulated feedback gain & phase response (up to 100kHz) is plotted below.

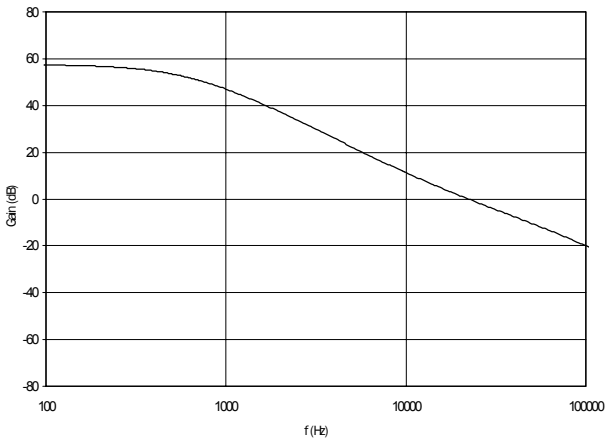
Applications Information (Cont.)



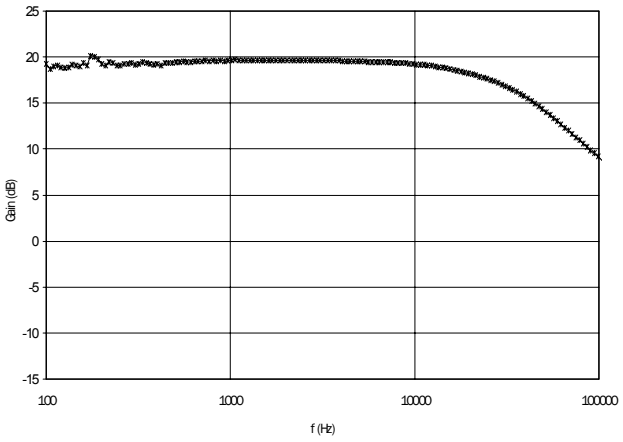


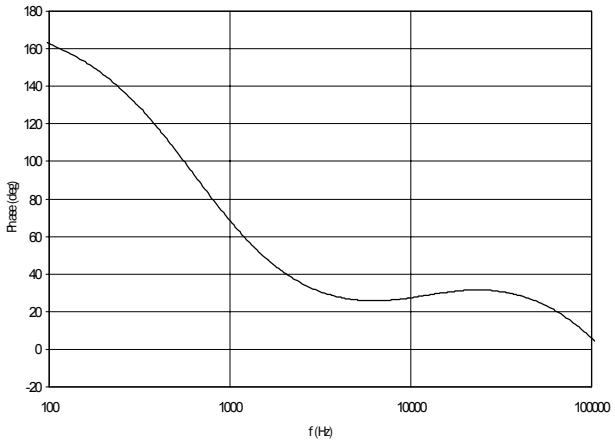
Simulated overall gain & phase responses (up to 100kHz) is plotted below.





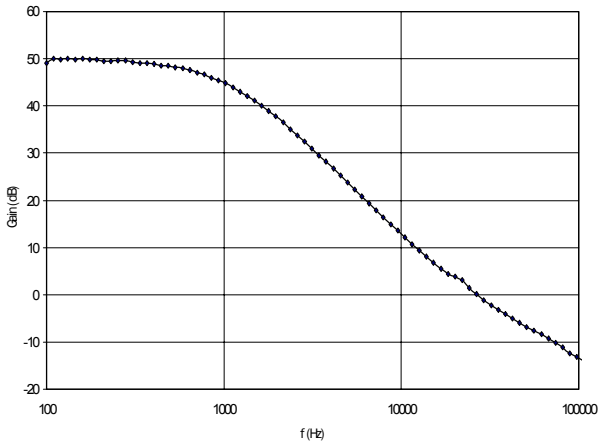
Measured feedback gain & phase responses (up to 100kHz) is plotted below.





Applications Information (Cont.)

Measured overall gain & phase response of the single-pole compensation using SC1403 is plotted below.



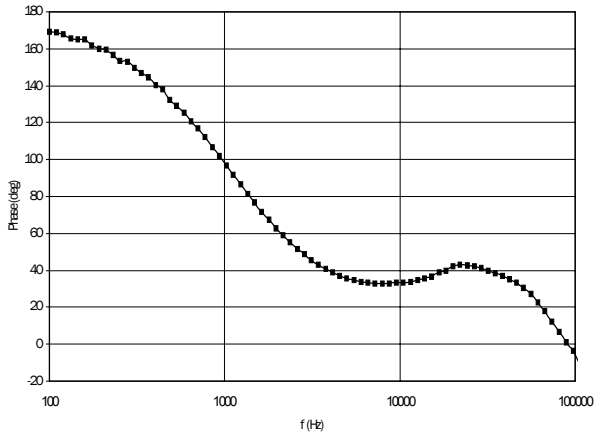


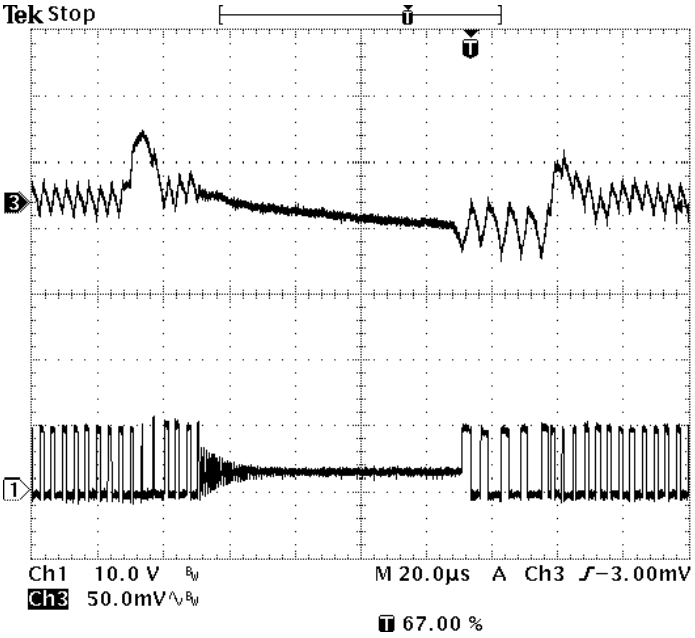
Table I. Recommended compensation cap for different output capacitance.

Output Cap	Recommended Compensation Cap Value
< = 180µF	100pF
> 180µF & <1000µF	200pF
>1000µF	330pF

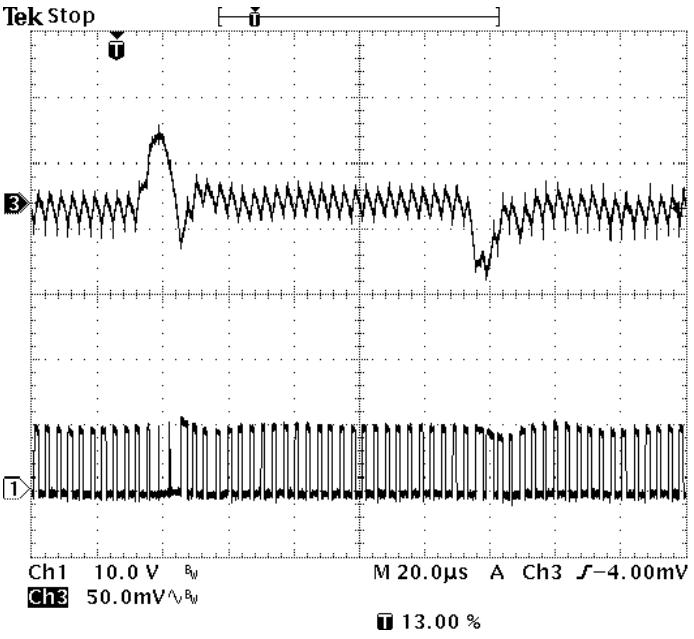
Typical Characteristics

Transient response using single-pole (capacitive) compensation is shown on the following pages. The load steps are from 0A to 3A and 3A to 6A. The applied di/dt is 2.5A/usec.

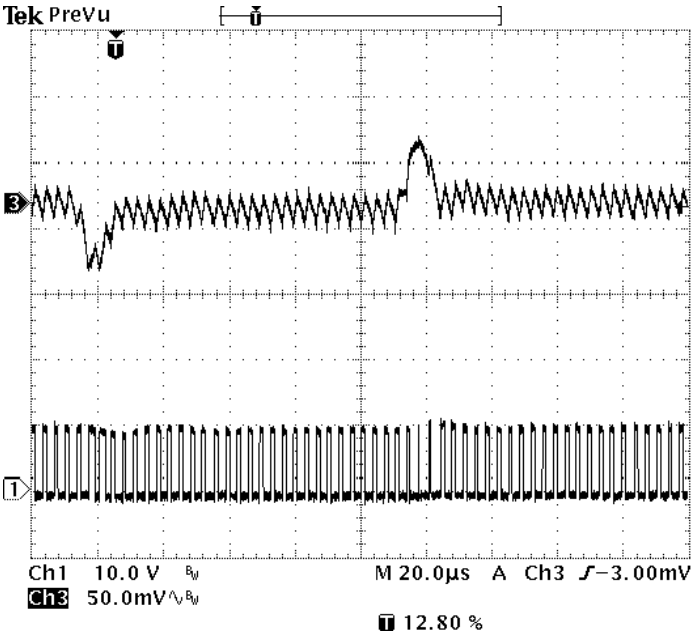
3.3V PSAVE enabled Vin = 10V, ILoad= 0A to 3A



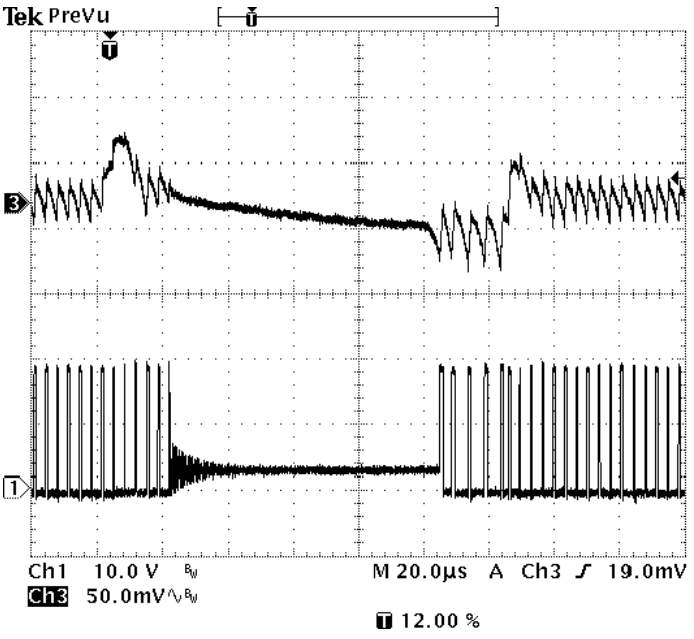
3.3V PSAVE disabled Vin = 10V, ILoad= 0A to 3A



3.3V Forced-Continuous Vin = 10V, ILoad= 3A to 6A

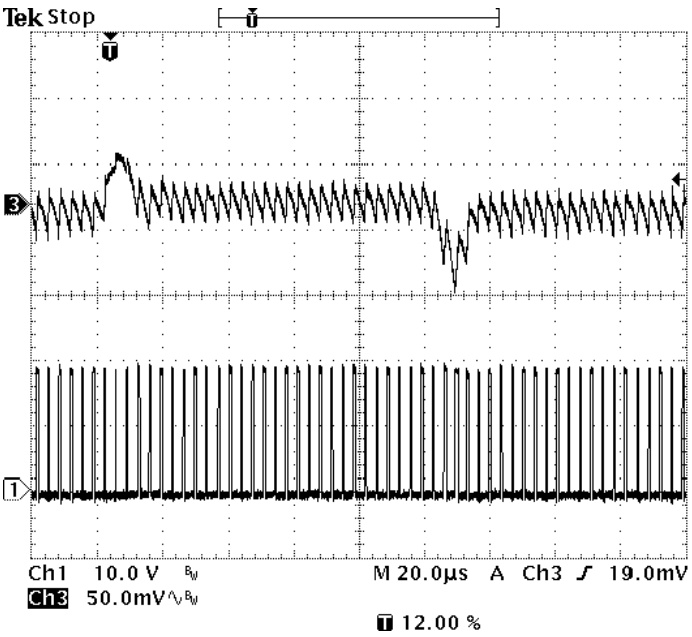


3.3V PSAVE enabled Vin = 19V, ILoad= 0A to 3A

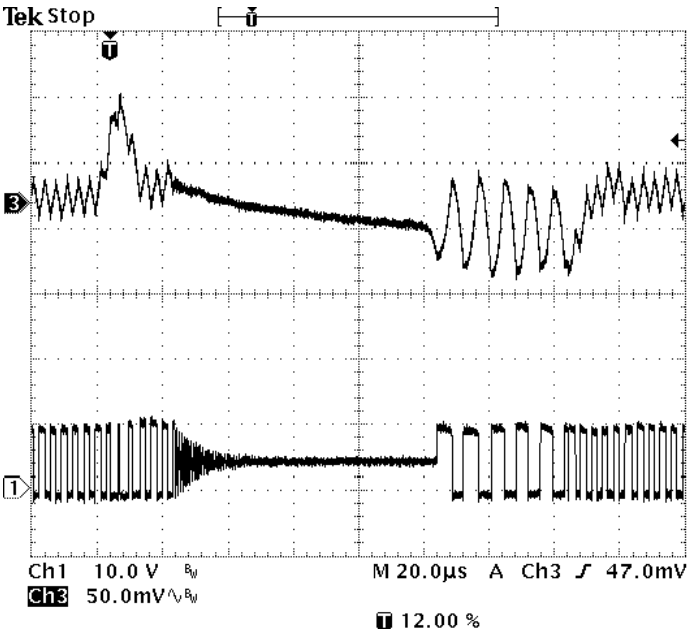


Typical Characteristics (Cont.)

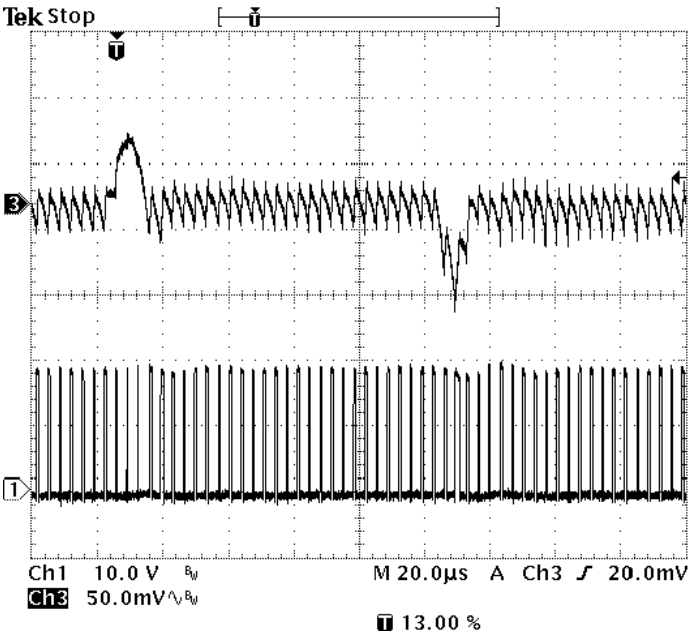
3.3V PSAVE disabled Vin = 19V, ILoad= 0A to 3A



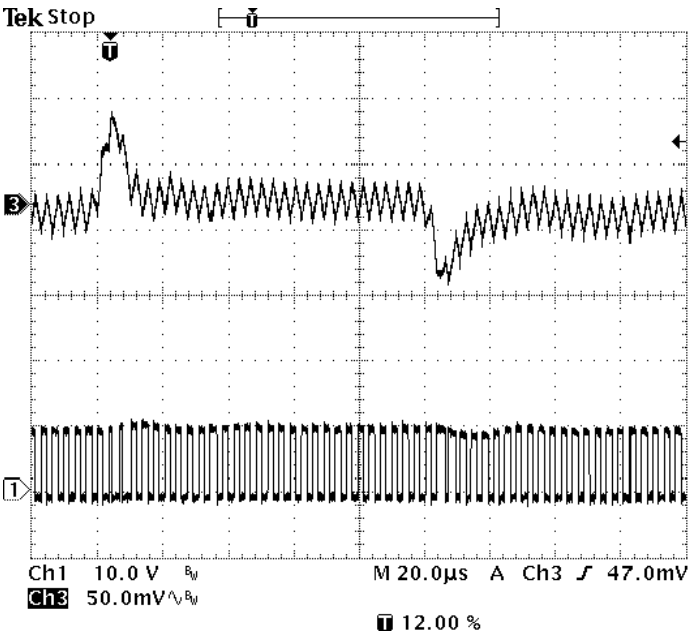
5.0V PSAVE enabled Vin = 10V, ILoad= 0A to 3A



3.3V Forced ContinuousVin = 19V, ILoad= 3A to 6A

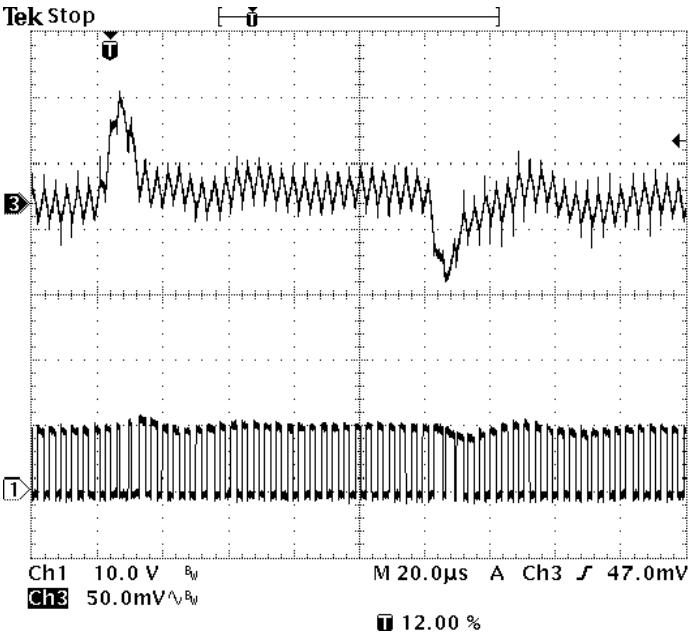


5.0V PSAVE disabled Vin = 10V, ILoad= 0A to 3A

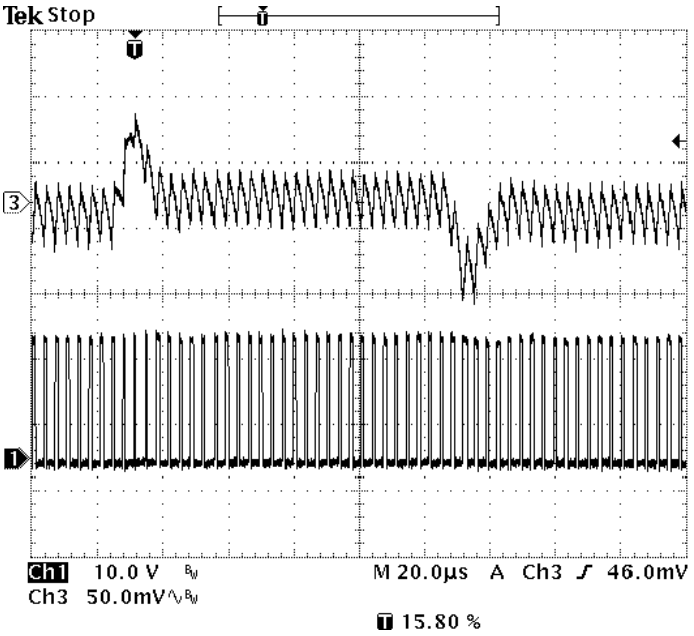


Typical Characteristics (Cont.)

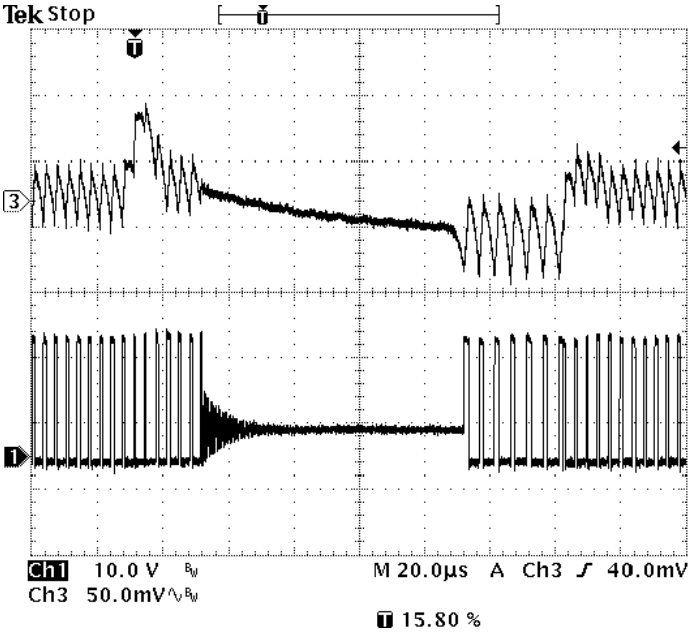
5.0V Forced Continuous Vin = 10V, ILoad= 3A to 6A



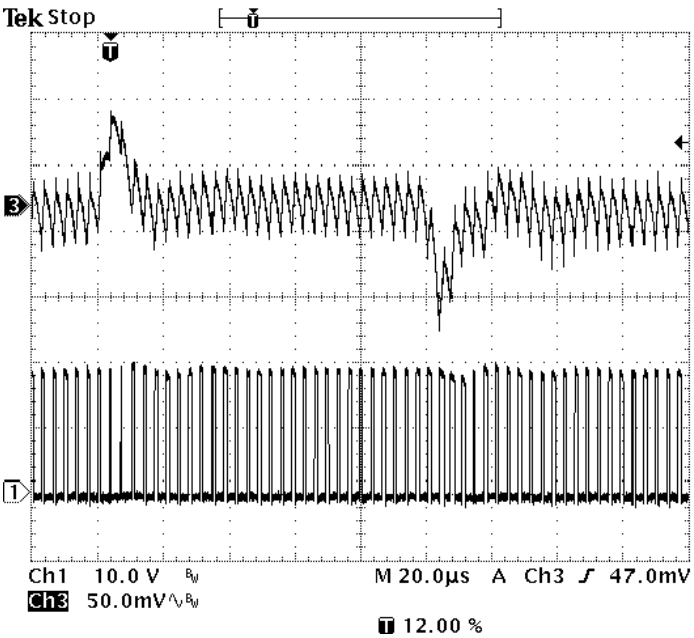
5.0V PSAVE disabled Vin = 19V, ILoad= 0A to 3A



5.0V PSAVE enabled Vin = 19V, ILoad= 0A to 3A



5.0V Forced Continuous Vin = 19V, ILoad= 3A to 6A

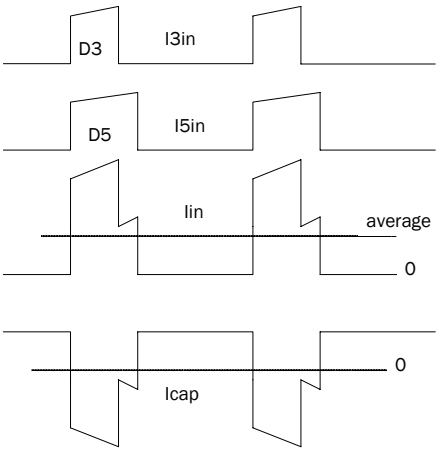


Applications Information

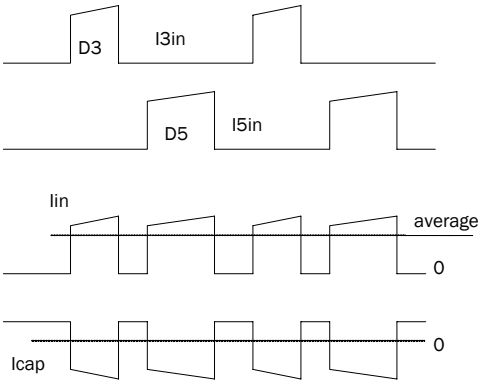
Input Capacitor Selection and Out-of-phase Switching

The SC1403 uses out-of-phase switching between the two converters to reduce input ripple current, allowing smaller, cheaper input capacitors compared to in-phase switching.

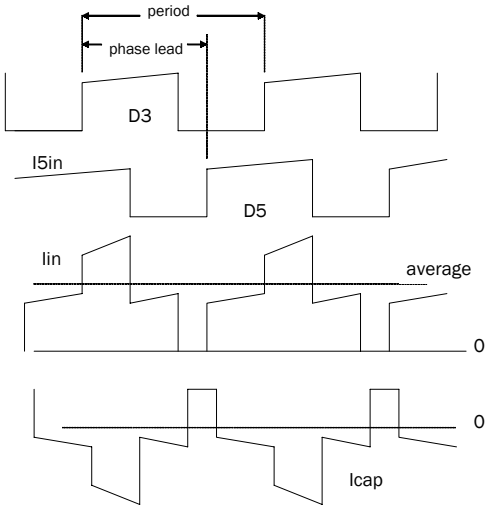
The figure below shows in-phase switching. I3in is the input current drawn by the 3.3V converter, I5in is the input current drawn by the 5V converter. The two converters start each switching cycle simultaneously, causing in a significant amount of overlap. This overlap increases the peak current. The total input current to the converter is the third trace, Iin, which shows how the two currents add together. The fourth trace shows the current flowing in and out of the input capacitors.



The next figure shows out-of-phase switching. The 3.3V and 5V converters are spaced apart, thus there is no overlap. This gives two benefits. The peak current is reduced, and the effective switch frequency is raised; both of which make filtering easier. The third trace shows the total input current, and the fourth trace shows the current flowing in and out of the input capacitors. The RMS value of the capacitor current is significantly lower than the in-phase case, which allows for smaller capacitors.



As the input voltage is reduced, the duty cycle of both converters increases. For all input voltages less than 8.3V it is impossible to prevent overlap when producing 3.3V and 5V outputs, regardless of the phase relationship between the two converters. Overlap can be seen in the following figure.



From an input filter standpoint it is desirable to minimize the overlap; but it is also desirable to keep the turn-on and turn-off transitions of the two converters separated in time, to prevent the two converters from affecting each other due to switching noise. The SC1403 keeps the turn-on and turn-off transitions separated in time by changing the phase relationship between the converter depending on the input voltage. The following table shows the phase relationship between 3V and 5V turn-on, based on input voltage.

Input voltage	Phase lead from 3V to 5V rising edge
Vin > 9.6 V	41% of switching period. No switching overlap between 3V and 5V.
9.6V > Vin > 6.7V	59% of switching period. Small overlap to prevent simultaneous 3V/5V switching.
6.7 > Vin	64% of switching period. Small overlap to prevent simultaneous 3V/5V switching.

Applications Information (Cont.)

Input ripple current calculations: The following equations provide quick approximations for input ripple current:

$$D3 = 3.3V / V_{IN} = 3V \text{ duty cycle}$$

$$D5 = 5V / V_{IN} = 5V \text{ duty cycle}$$

$$I3 = 3V \text{ DC load current}$$

$$I5 = 5V \text{ DC load current}$$

D_{OVL} = overlapping duty cycle of the 3V and 5V pulses (varies according to input voltage)

$$D_{OVL} = 0 \text{ for } 9.6V \le V_{IN}$$

$$D_{OVL} = (D5 - 0.41) \text{ for } 6.7V \le V_{IN} < 9.6V$$

$$D_{OVL} = (D5 - 0.36) \text{ for } V_{IN} < 6.7$$

$$I_{IN} = \text{Average DC input current}$$

$$I_{IN} = I3 \cdot D3 + I5 \cdot D5$$

$$I_{SW\_RMS} = \text{RMS current drawn from } V_{IN}$$

$$I_{SW\_RMS}^2 = D3 \cdot I3^2 + D5 \cdot I5^2 + 2 \cdot D_{OVL} \cdot I3 \cdot I5$$

$$I_{RMS\_CAP} = \sqrt{I_{SW\_RMS}^2 + I_{IN\_AVE}^2}$$

The worst-case ripple current varies by application. For the case of I3 = I5 = 6A, the worst-case ripple occurs at Vin = 7.5V, at which point the rms capacitor ripple current is 4.2A. To handle this the reference design uses 4 paralleled ceramic capacitors, (Murata GRM32NF51E106Z, 10 uF 25V, size 1210). Each capacitor is rated at 2.2A.

Choosing Synchronous mosfet and Schottky Diode

Since this is a buck topology, the voltage and current ratings of the synchronous mosfet are the same as the main switching mosfet. It makes sense cost- and volume-wise to use the same mosfet for the main switch as for the synchronous mosfet. Therefore, IRF7413 is used again in the design for synchronous mosfet.

To improve overall efficiency, an external Schottky diode is used in parallel to the synchronous mosfet. The freewheeling current is going into the Schottky diode instead of the body diode of the synchronous mosfet, which usually has very high forward drop and slow transient behavior. It is really important when laying out the board to place both the synchronous mosfet and Schottky diode close to each other to reduce the current ramp-up and ramp-down time due to parasitic inductance between the channel of the mosfet and the Schottky diode. The current rating of the Schottky diode can be determined by the following equation:

$$I_{F\_AVG} = I_{LOAD} \cdot \frac{100n}{T_S} = 0.2A$$

where 100nsec is the estimated time between the mosfet turning off and the Schottky diode taking over and Ts = 3.33uS. Therefore a Schottky diode with a forward current of 0.5A is sufficient for this design.

External Feedback Design

In order to optimize the ripple voltage during Power Save mode, it is strongly recommended to use external voltage dividers (R10 and R9 for 5V power train; R8 and R11 for 3.3V power train) to achieve the required output voltages. In addition a 56pF (C22 for 5V and C21 for 3.3V) cap is recommended connecting from the output to both feedback pins (pin # 3 and #12). The signal-to-noise ratio is therefore increased due to the added zeros.

Applications Information (Cont.)

Operation Below 6V input

The SC1403 will operate below 6V input voltage with careful design, but there are limitations. The first limitation is the maximum available duty cycle from the SC1403, which limits the obtainable output voltage. The design should minimize all circuit losses through the system in order to deliver maximum power to the output.

A second limitation with operation below 6V is transient response. When load current increases rapidly, the output voltage drops slightly; the feedback loop normally increases duty cycle briefly to bring the output voltage back up. If duty cycle is already near the maximum limit, the duty cycle cannot increase enough to meet the demand, and the output voltage sags more than normal. This problem can not be solved by changing the feedback compensation, it is a function of the input voltage, duty cycle, and inductor and capacitor values.

If an application requires 5V output from an input voltage below 6V, the following guidelines should be used:

1 - Set the switching frequency to 200 kHz (Tie SYNC to GND). This increases the maximum duty cycle compared to 300 kHz operation.

2 - Minimize the resistance in the power train. Select mosfets, inductor, and current sense resistor to provide the lowest resistance as is practical.

3 - Minimize the pcb resistance for all traces carrying high current. This includes traces to the input capacitors, mosfets and diodes, inductor, current sense resistor, and output capacitor.

4 - Minimize the resistance between the SC1403 circuit and the power source (battery, battery charger, AC adaptor).

5 - Use low ESR capacitors on the input to prevent the input voltage dropping during on-time.

6 - If large load transients are expected, high capacitance and low ESR capacitors should be used on both the input and output.

Overvoltage Test

Measuring the overvoltage trip point can be problematic. Any buck converter with synchronous mosfets can act as a boost converter, sending energy from output to input. In some cases the energy sent to the input is enough to drive the input voltage beyond normal levels, causing input overvoltage. To prevent this enable the SC1403 PSAVE# feature, which effectively disables the low side mosfet drive so that little energy, if any, is transferred back to the input.

Semtech recommends the following circuit for measuring the overvoltage trip point. D1 prevents the output voltage from damaging lab supply 1. R1 limits the amount of energy that can be cycled from the output to the input. R2 absorbs the energy that might flow from output to input, and D2 protects lab supply from possible damage. The ON5 signal is monitored to indicate when overvoltage occurs.

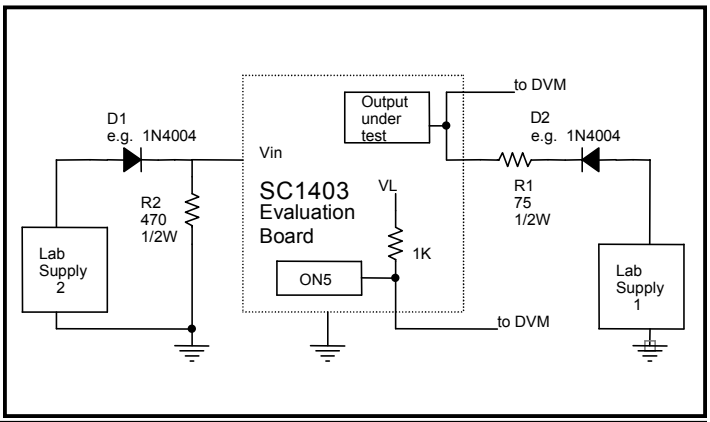
Initial conditions:

Both lab supplies set to zero volts
No load connected to 3V or 5V
PSAVE# enabled (PSAVE# tied to GND)
ON5, ON3 both enabled
DVMs monitoring ON5 and the output under test
Oscilloscope probe connected to Phase Node
of the output under test (not strictly required)

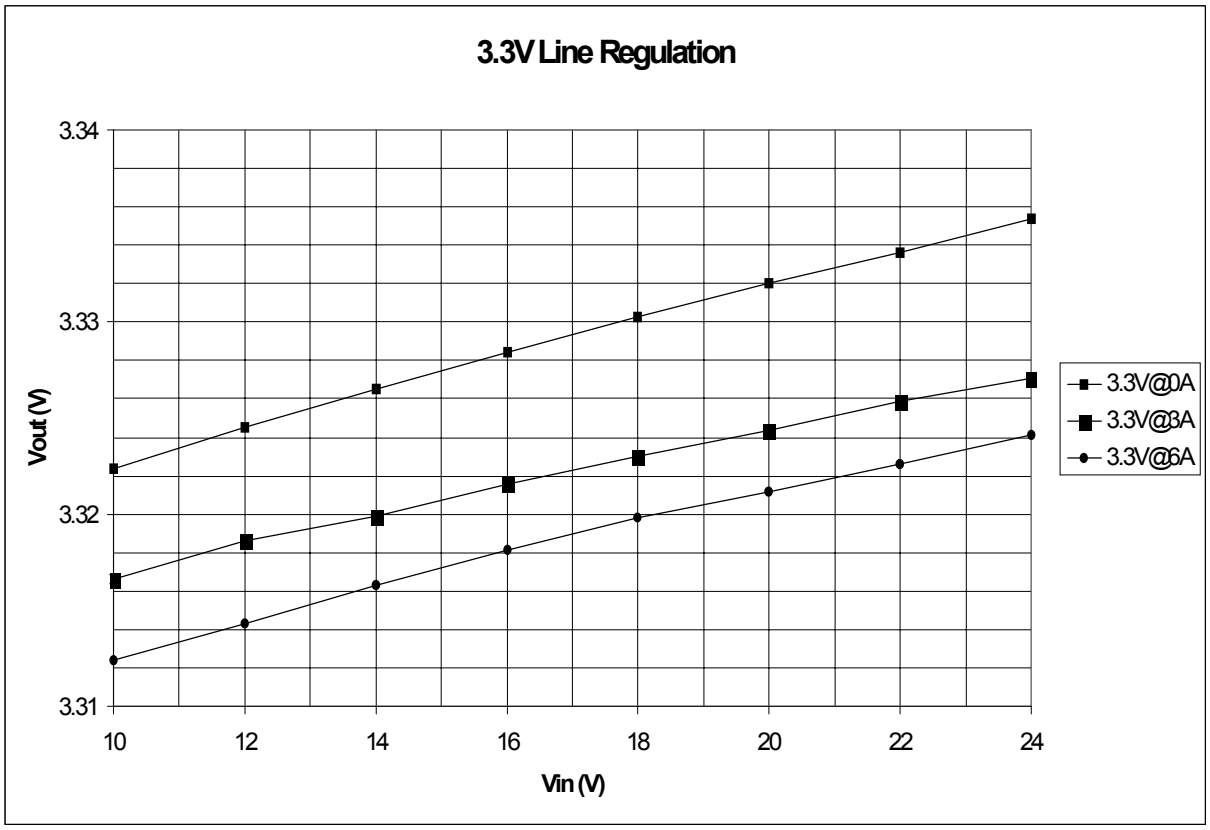
Set lab supply 2 to provide 10V at the SC1403 input. The phase node of the output being tested should show some switching activity. The ON5 pin should be above 4V.

Slowly increase lab supply 1 until the output under test rises slightly above it's normal DC level. As the input lab supply 1 increases, switching activity at the phase node will cease. The ON5 pin should remain above 4V.

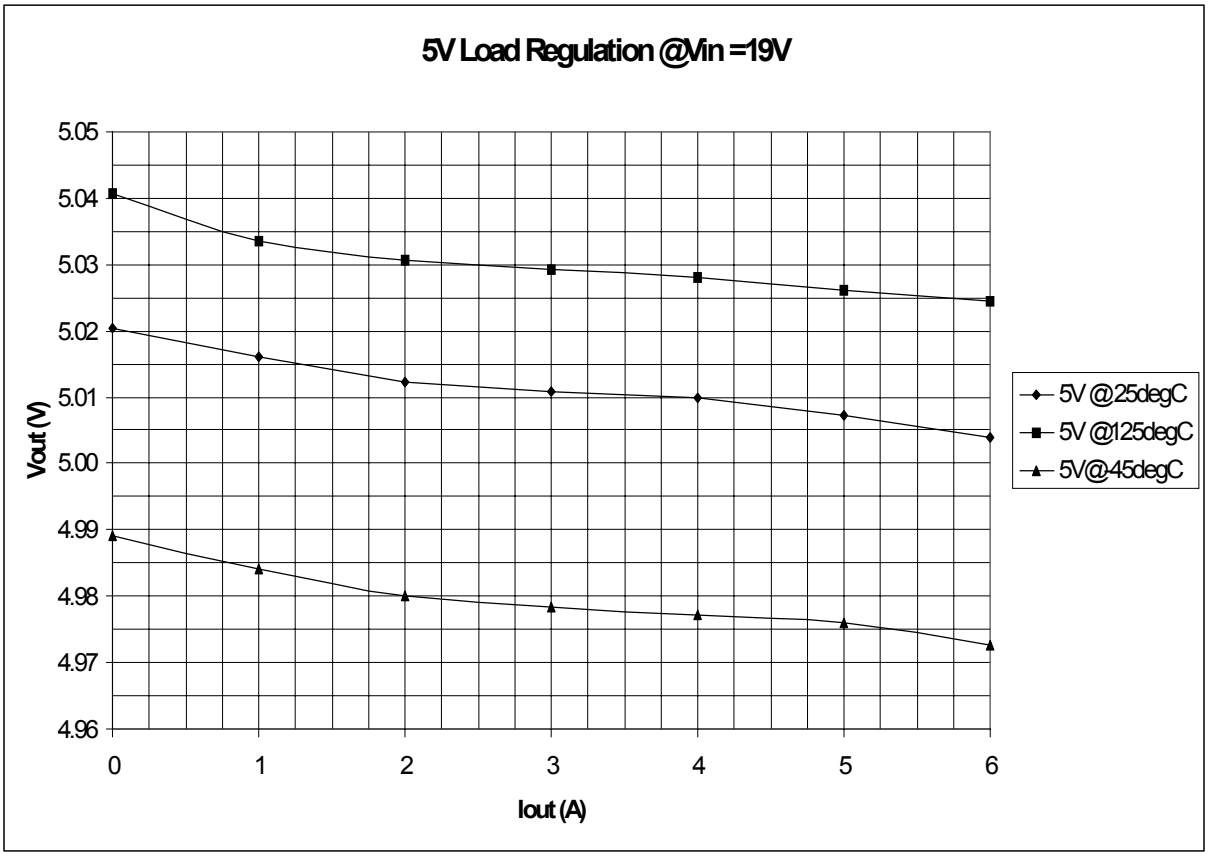
Increase lab supply 1 in very small increments, monitoring both ON5 and the output under test. The overvoltage trip point is the highest voltage seen at the output before ON5 pulls low (approximately 0.3V). Do not record the voltage seen at the output after ON5 has pulled low; when ON5 pulls low, the current flowing in D1 changes, corrupting the voltage seen at the output.

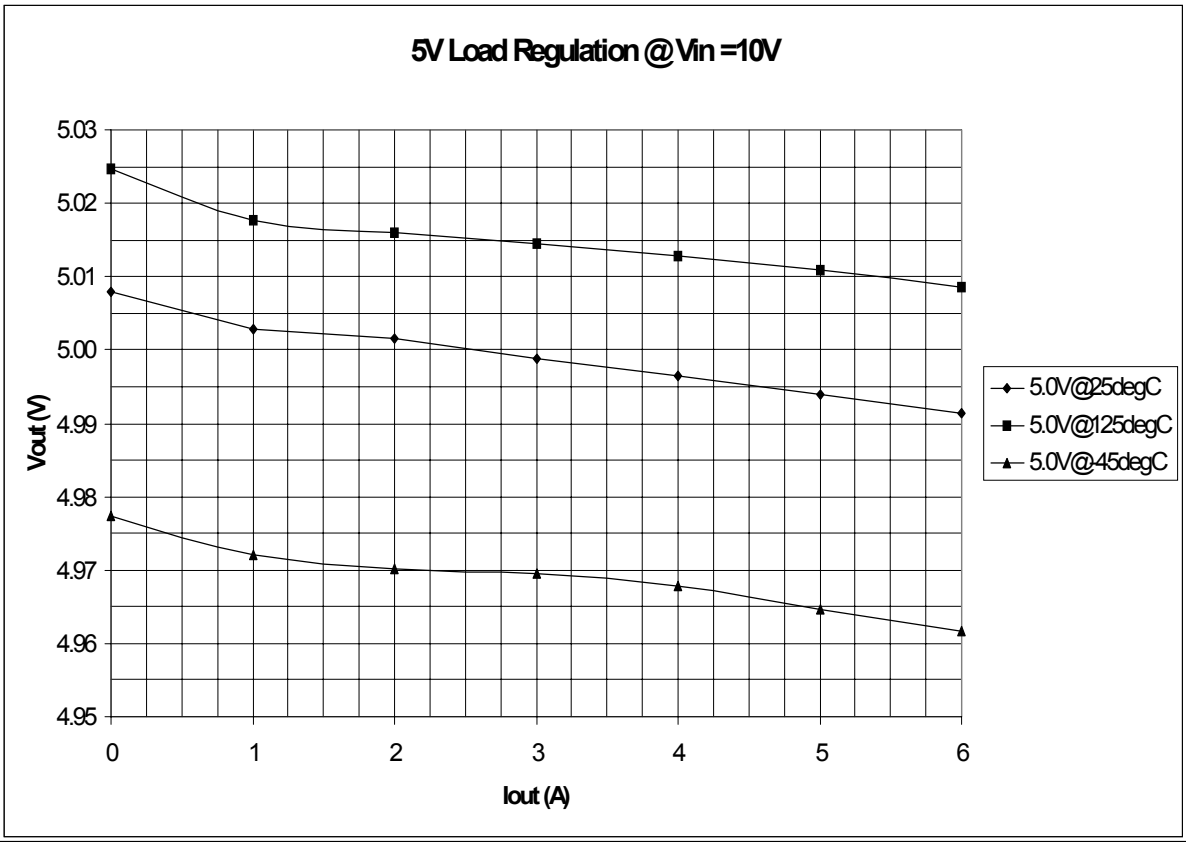


Typical Characteristics

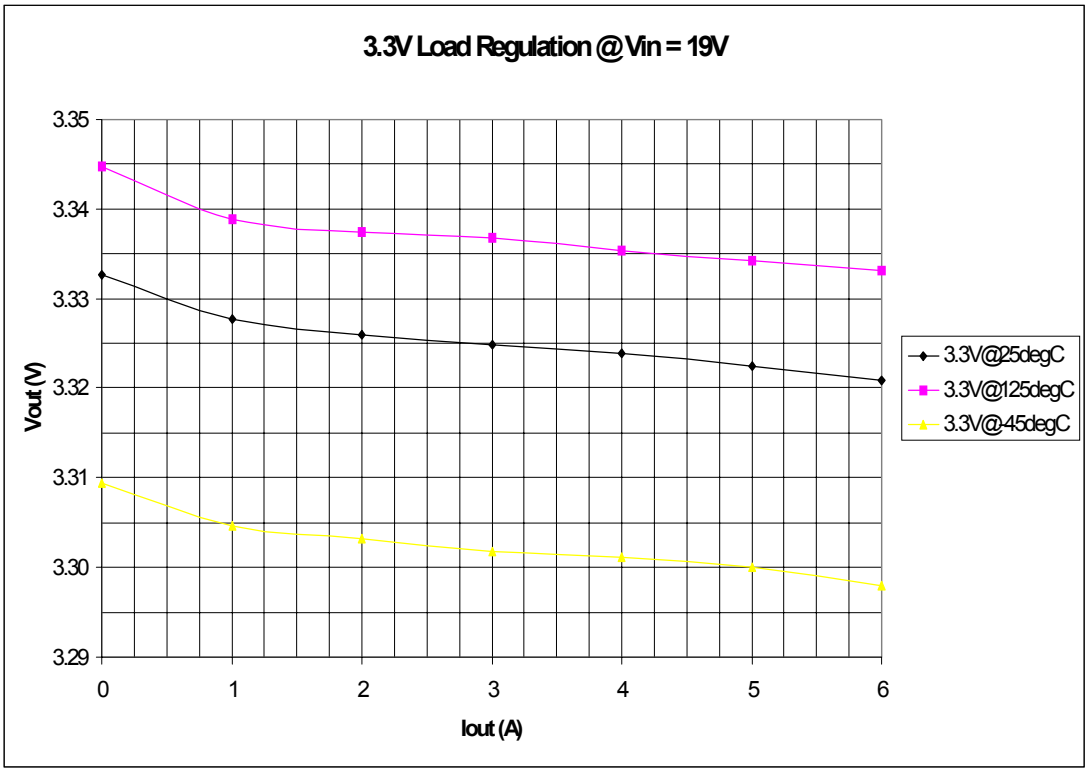


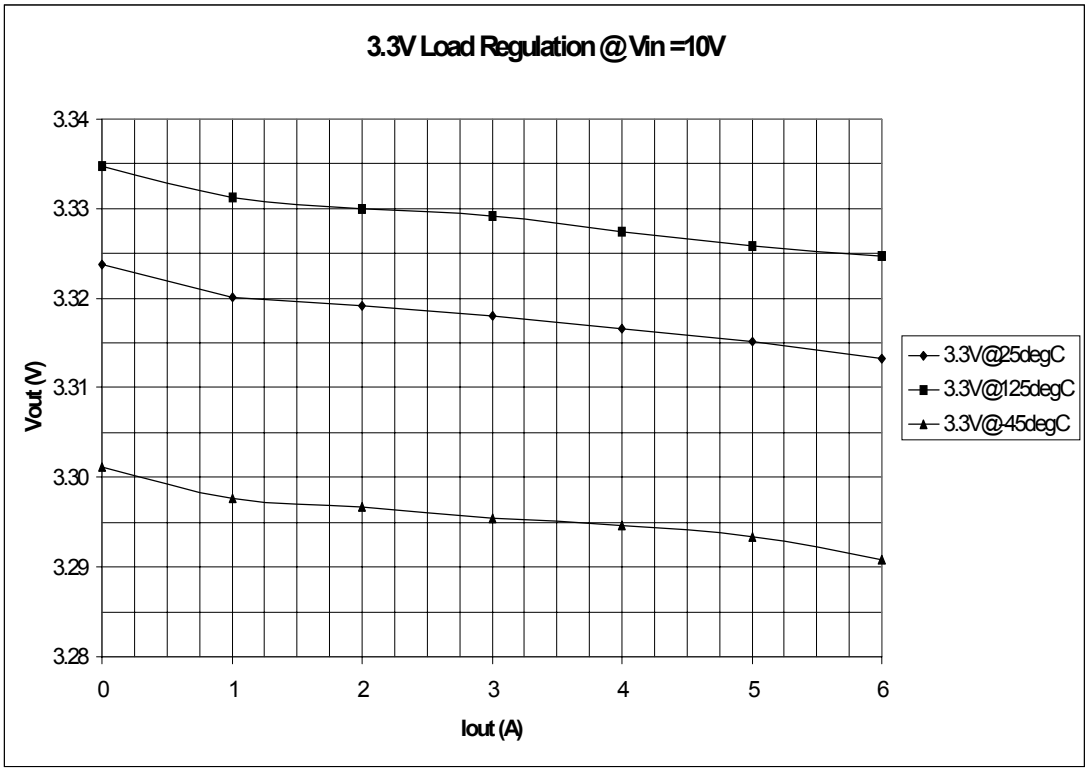
Typical Characteristics (Cont.)



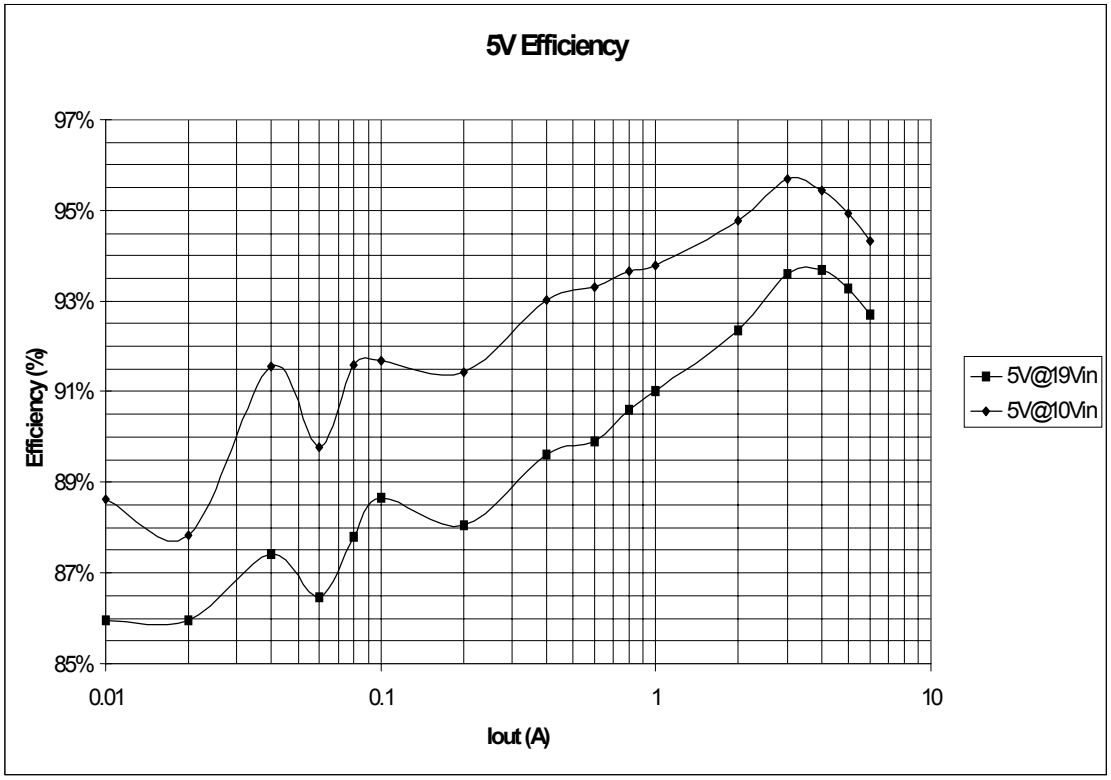


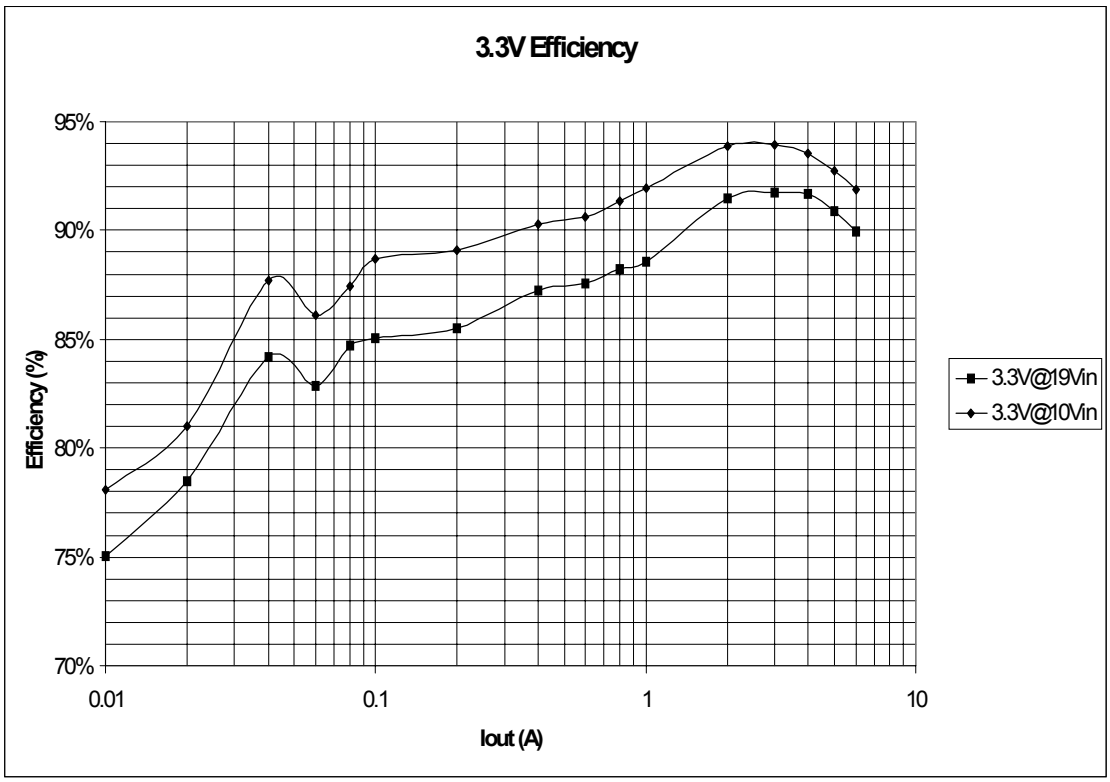
Typical Characteristics (Cont.)



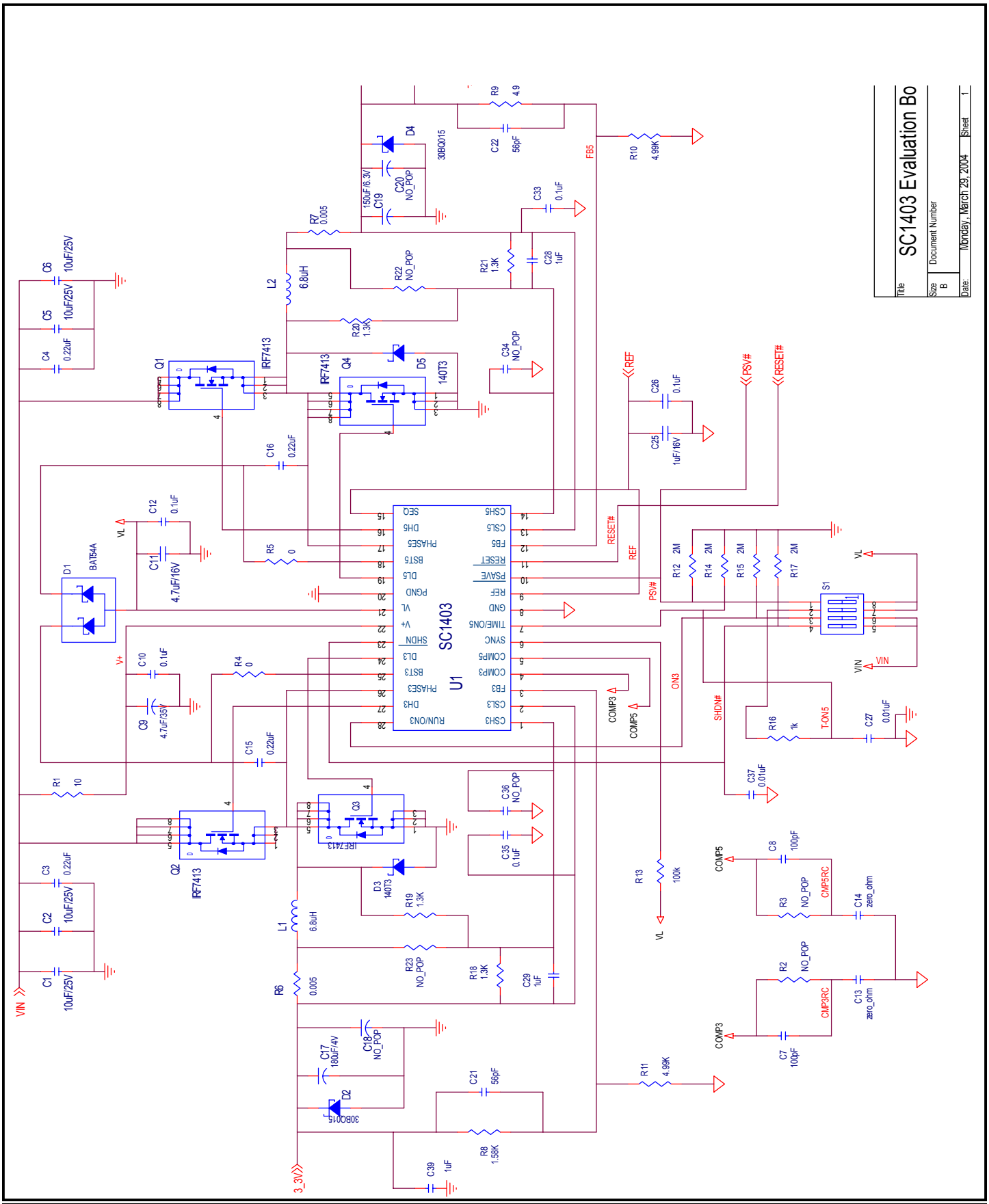


Typical Characteristics (Cont.)





Evaluation Board Schematic

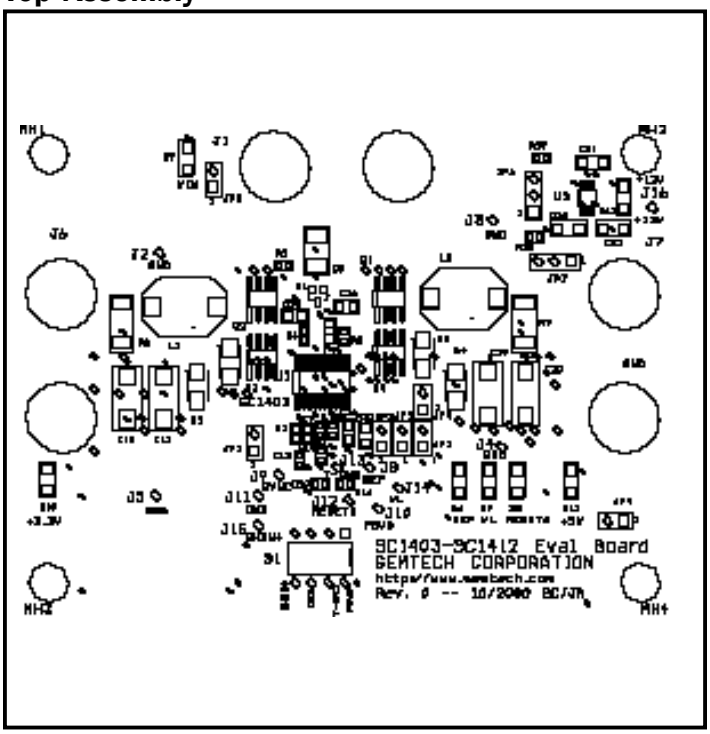


Evaluation Board Bill of Materials

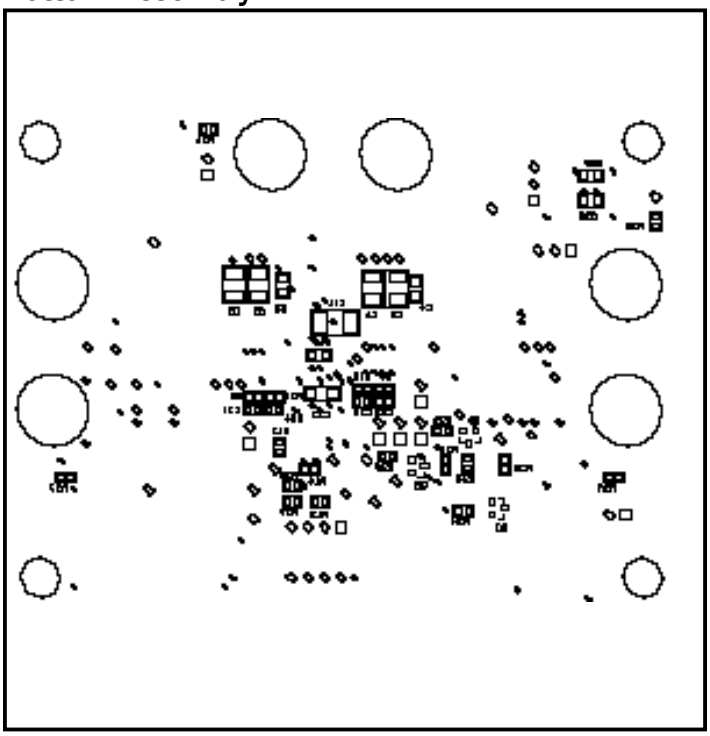
Item	Quanity	Designation	Part Number	Description	Manufacturer	Case
1	4	C1,C2,C5,C6	GRM230Y5V106Z025	10uF, 25V	Murata	1210
2	4	C3,C4,C15,C16		0.22uF		0806
3	2	C7,C8		100pF		0603
4	2	C9, C11		4.7uF		
5	1	C25, C28, C29		1uF ceramic		
6	1	C17	EEF-UE0G181R	180uF, 4V	Panasonic	D_Case_7343
7	1	C19	EEF-UE0J151R	150uF, 6.3V	Panasonic	D_Case_7343
8	1	D1	BAT54A	30V, 200ma, dual anode	Zetex	SOT-23
9	2	D3, D5	MBRS140T3	40V, 1A Schottky	Motorola	SMB
10	2	D2, D4	30BQ015	15V, 3A Schottky	International Rectifier	
11	2	L1, L2	DR127-6R8	SMT Inductor 6.8uH	Coiltronics	
12	4	Q1, Q2, Q3, Q4	IRF7413	30V N-channel MOSFET	International Rectifier	SO8
13	1	R1		10 ohm		603
14	2	R4, R5		0 ohm		603
15	2	R6, R7 (resistive sensing only)	WSL2512R005FB43	5mohm	Vishay Dale	2512
16	2	R16		1Kohm		603
18	1	U1	SC463ITS	Mobile PWM Controller with VCS	Semtech	TSSOP28

Evaluation Board Layout

Top Assembly



Bottom Assembly

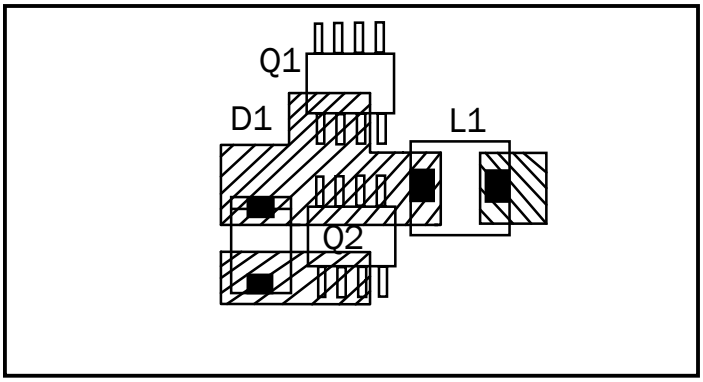


Layout Guidelines

As with any high frequency switching regulator design, a good PCB layout is very essential in order to achieve optimum noise, efficiency, and stability performance of the converter. Before starting PCB layout, a careful layout strategy is strongly recommended. See the PCB layout in the SC1403 Evaluation Kit manual for example. In most applications, use FR4 with 4 or more layers and at least 2 ounce copper (for output current up to 6A). Use at least one inner layer for ground connection. It is always a good practice to tie signal-ground and power-ground at one single point so that the signal-ground is not easily contaminated. High current paths should have low inductance and resistance by making trace widths as wide as possible and lengths as short as possible. Properly decouple lines that pull large amounts of current in short periods of time. The following layout strategy should be used in order to fully utilize the potential of SC1403.

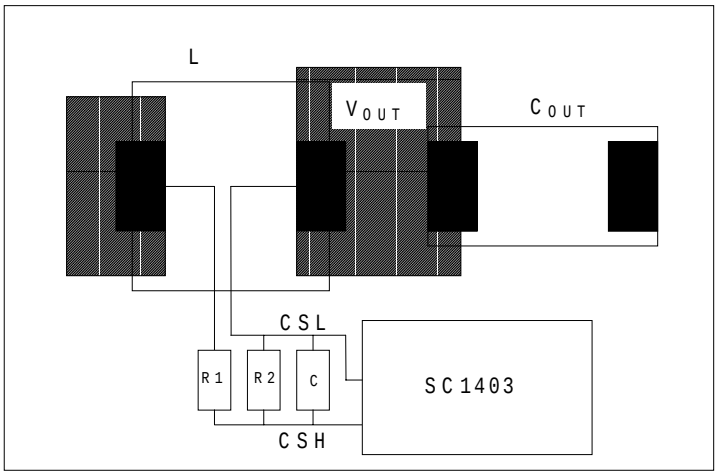
A. Power train arrangement.

Place power train components first. The following figure shows the recommended power train arrangement. Q1 is the main switching FET, Q2 is the synchronous Rectifier FET, D1 is the Schottky diode and L1 is the output inductor. The phase node, where the source of the upper switching FET and the drain of the synchronous rectifier meets, switches at very high rate of speed, and is generally the largest source of common-mode noise in the converter circuit. It should be kept to a minimum size consistent with its connectivity and current carrying requirements. Also place the Schottky diode as close to the phase node as possible to minimize the trace inductance, therefore reducing the efficiency loss due to the current ramp-up and down time. This becomes extremely important when the converter needs to handle high di/dt requirement. Vias between power components should be used only when necessary: if vias are required, use multiple vias to reduce the inter-component impedance, and keep the traces between vias and power components as short and wide as possible.

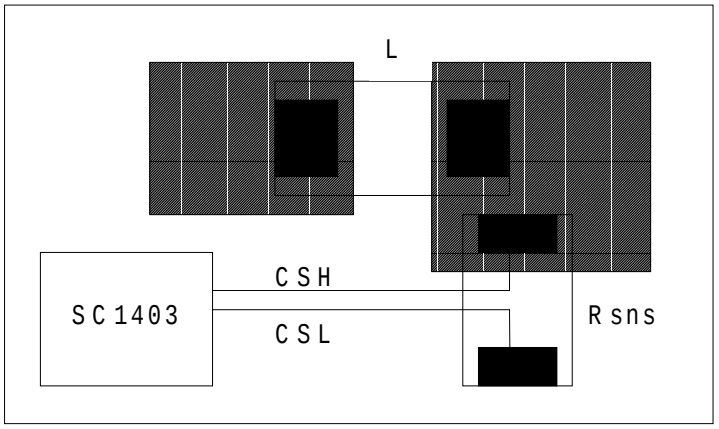


B. Current Sense.

With DCR sensing: The connections from the RC network to the inductor should be Kelvin connections directly at the inductor solder pads. Place the capacitor close to the CSH/CSL pins on the SC1403, and connect to the capacitor using short direct traces.



With resistive sensing: minimize the length of current sense signal traces. Keep them less than 15mm. Use Kelvin connections as shown below; keep the traces parallel to each other and as close together as possible.



C. Gate Drive.

The SC1403 has built-in gate drivers capable of sinking/sourcing 1A pk-pk. Upper gate drive signals are noisier than the lower ones, so place them away from sensitive analog circuits. Make sure the lower gate traces are as close as possible to the SC1403 pins, and make both upper and lower gate traces as wide as possible.

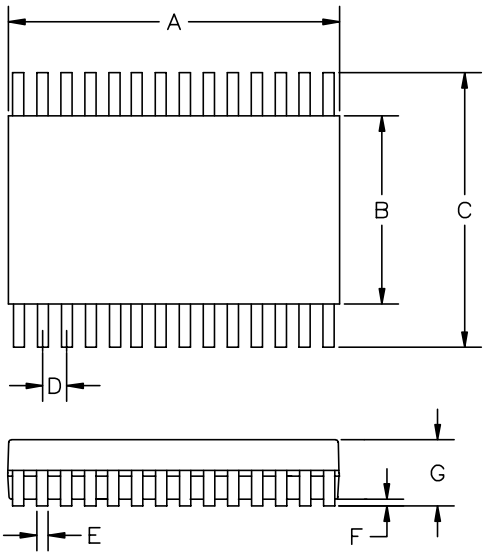
D. PWM placement (pins) and signal ground island.

Connect all analog grounds to a separate solid copper island plane, which connects to the SC1403's GND pin. This includes REF, FB3, FB5, COMP3, COMP5, SYNC, ON3, ON5, PSV# and RESET#.

E. Ground plane arrangement.

There are several ways to tie the different grounds together (analog ground, input power ground, and output power ground). With a buck topology, the output is quiet compared to the input side. The output is the best place to tie the analog ground to the power ground, often through a 0Ω resistor. The input power ground and the output power ground can be tied together using internal planes.

Outline Drawing - TSSOP-28



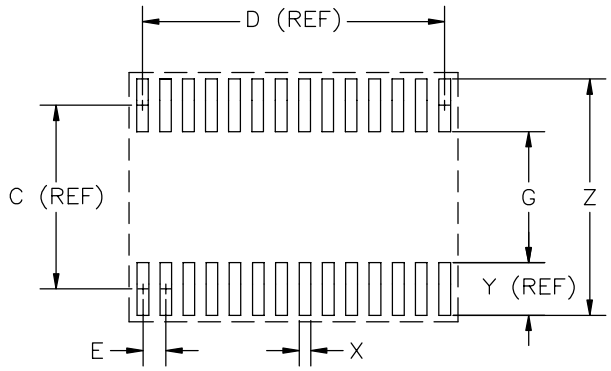
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO–153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

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