



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

| Parameter                               | Symbol        | Maximum     | Units |
|---|---------------|-------------|-------|
| Supply Voltage                          | $V_{IN}$      | 34          | V     |
| Voltage on BST Pins                     | $V_{BST}$     | 42          | V     |
| Oscillator Frequency <sup>(1)</sup>     |               | 2           | MHz   |
| VCC                                     |               | 8           | V     |
| Thermal Resistance Junction to Case     | $\theta_{JC}$ | 25          | °C/W  |
| Thermal Resistance Junction to Ambient  | $\theta_{JA}$ | 80          | °C/W  |
| Operating Temperature Range             | $T_A$         | -40 to +85  | °C    |
| Storage Temperature Range               | $T_{STG}$     | -55 to +150 | °C    |
| Lead Temperature (Soldering) 10 seconds | $T_{LEAD}$    | 300         | °C    |

Note: (1) Maximum frequency and maximum supply voltage could cause excessive power dissipation in the part.

**Electrical Characteristics**

Unless specified  $V_{IN} = 24V$ ,  $T_A = 25^\circ C$

| Parameter                  | Conditions        | Min  | Typ  | Max  | Units      |
|----------------------------|-------------------|------|------|------|------------|
| Supply Voltage, $V_{IN}$   |                   | 8.5  |      | 30   | V          |
| Supply Current             | ENABLE = 0        |      | 30   | 40   | mA         |
| Under Voltage Lockout      |                   |      | 5.8  |      | V          |
| UVLO Hysteresis            |                   |      | 400  |      | mV         |
| <b>Voltage Regulator</b>   |                   |      |      |      |            |
| Pre Regulator Voltage      |                   | 6    |      | 7    | V          |
| Bgout Voltage              | $C_{REF} = 4.7nF$ | 0.99 | 1    | 1.01 | V          |
| Bgout Impedance            |                   |      | 3    |      | K $\Omega$ |
| REGDRV Pin Sink Current    | $I_{REGDRV}$      |      | 5    |      | mA         |
| <b>Error Amp</b>           |                   |      |      |      |            |
| Input Offset Voltage       |                   |      |      | 15   | mV         |
| Input Offset Mismatch      |                   |      |      | 4    | mV         |
| Input Impedance            |                   | 5    |      |      | K $\Omega$ |
| Linear Transconductance    |                   |      | .002 |      | A/V        |
| <b>Internal Oscillator</b> |                   |      |      |      |            |
| Frequency                  | $R_{REF} = 30K$   |      | 1    |      | MHz        |
| Frequency                  | $R_{REF} = 60K$   |      | 500  |      | kHz        |
| Ramp Valley to Peak        | $V_{IN} = 12V$    |      | 1.5  |      | V          |
| Ramp Valley to Peak        | $V_{IN} = 24V$    |      | 3    |      | V          |

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified  $V_{IN} = 24V$ ,  $T_A = 25^\circ C$ 

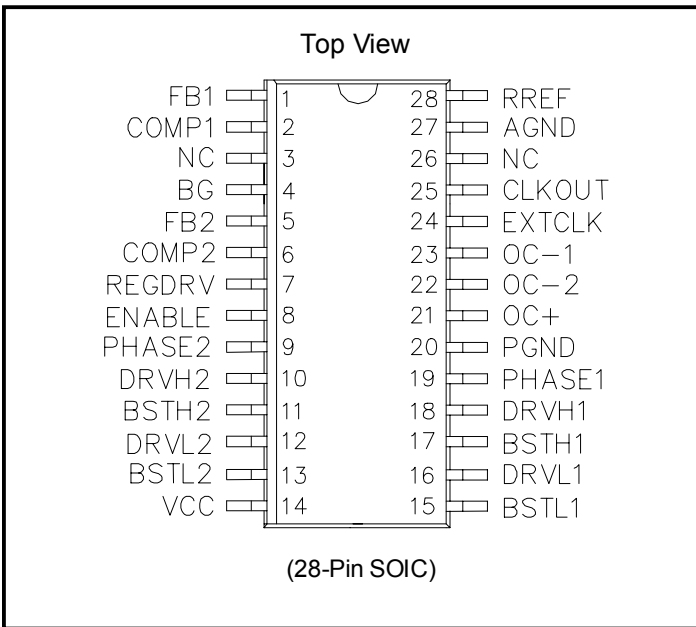
| Parameter                      | Conditions                       | Min  | Typ             | Max | Units      |
|--------------------------------|----------------------------------|------|-----------------|-----|------------|
| <b>External Clock</b>          |                                  |      |                 |     |            |
| Detect Time                    | Rise Time < 50ns                 |      |                 | 2   | $\mu s$    |
| Unlock Time                    |                                  | 10   |                 | 50  | $\mu s$    |
| Frequency Range                |                                  | 0.27 |                 | 1   | MHz        |
| <b>High Side Gate Drive</b>    |                                  |      |                 |     |            |
| Max Duty Cycle                 |                                  |      | 45              |     | %          |
| Peak Source                    | $C_{LOAD} = 10nF$                |      | 1               |     | A          |
| Peak Sink                      | $C_{LOAD} = 10nF$                |      | 1               |     | A          |
| <b>Low Side Gate Drive</b>     |                                  |      |                 |     |            |
| Peak Source                    | $C_{LOAD} = 10nF$                |      | 2               |     | A          |
| Peak Sink                      | $C_{LOAD} = 10nF$                |      | 2               |     | A          |
| <b>Sync Drive Timing</b>       |                                  |      |                 |     |            |
| Min Non-overlap                | $C_{LOAD} = 1nF$ Fet Drive < 1V  | 20   | 50              |     | ns         |
| PWM Match                      | 50% Duty Cycle, $F_{OSC} = 1MHz$ | -1   |                 | 1   | %          |
| <b>Logic Input Pins</b>        |                                  |      |                 |     |            |
| Input Bias Current             | $V_{IN} = 0 - 5V$                | -10  |                 | 10  | $\mu A$    |
| Logic Threshold                |                                  |      | 0.8             |     | V          |
| FB2 Disable Threshold          |                                  |      | $V_{CC} - 0.7V$ |     | V          |
| <b>Over Current Protection</b> |                                  |      |                 |     |            |
| OCP Threshold                  |                                  | 103  | 115             | 127 | mV         |
| OC+ I/P Bias Current           | $V_{IN} = 24V$                   |      | 700             |     | $\mu A$    |
| OC- I/P Bias Current           |                                  |      | 50              |     | $\mu A$    |
| <b>Over Voltage Protection</b> |                                  |      |                 |     |            |
| OVP Threshold                  |                                  |      | 120             |     | %          |
| Thermal Shutdown               |                                  |      | 150             |     | $^\circ C$ |

Note:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

## POWER MANAGEMENT

### Pin Configuration



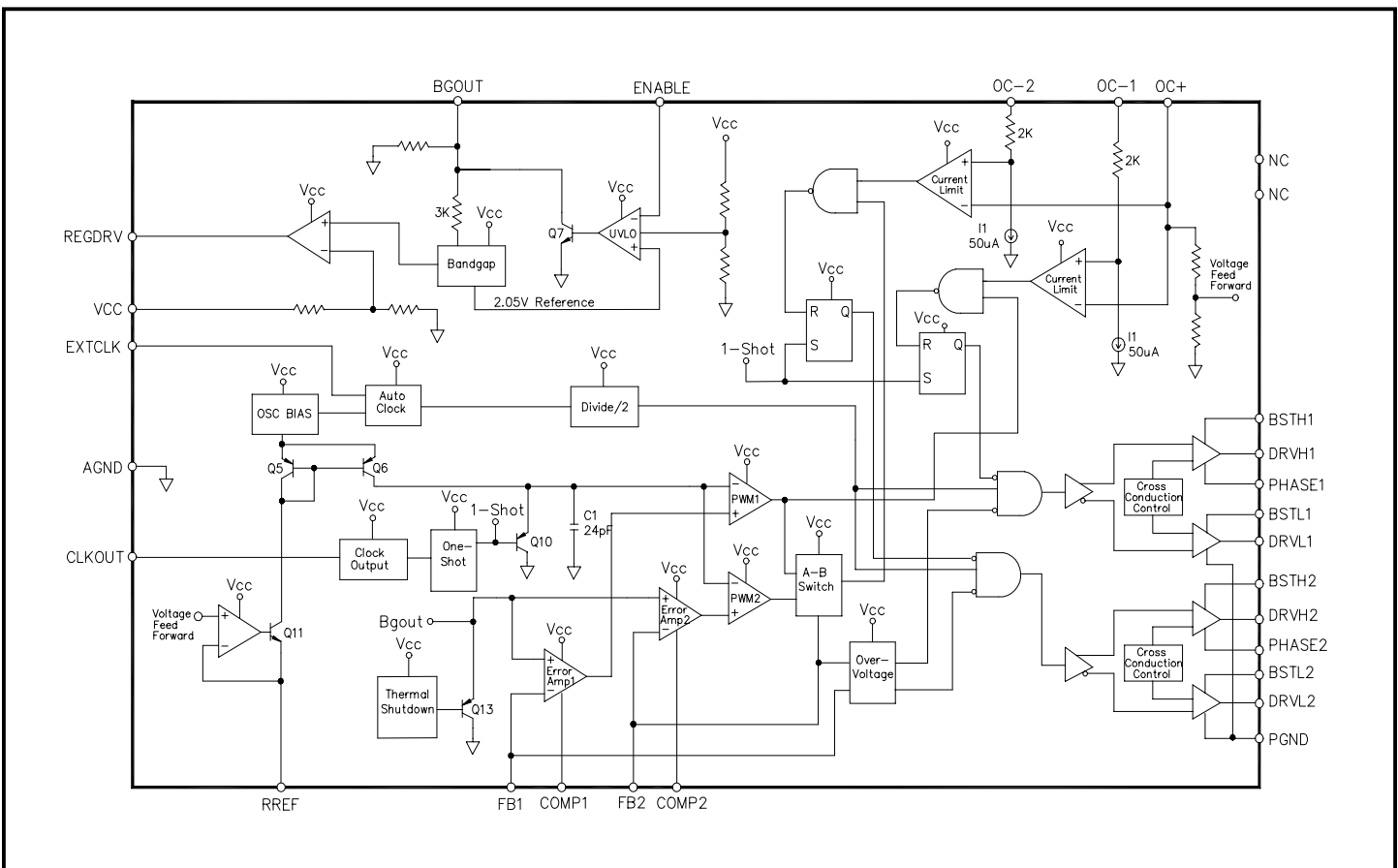
### Ordering Information

| Part Number                 | PACKAGE <sup>(1)</sup>  | T <sub>AMB</sub> (T <sub>A</sub> ) |
|-----------------------------|-------------------------|------------------------------------|
| SC2450ISWTR                 | SO-28                   | -40 - +85°C                        |
| SC2450ISWTRT <sup>(2)</sup> |                         |                                    |
| SC2450EVB                   | SC2450 Evaluation Board |                                    |

#### Notes:

- (1) Only available in tape and reel packaging. A reel contains 1000 devices.
- (2) Lead free product. This product is fully WEEE and RoHS compliant.

### Block Diagram



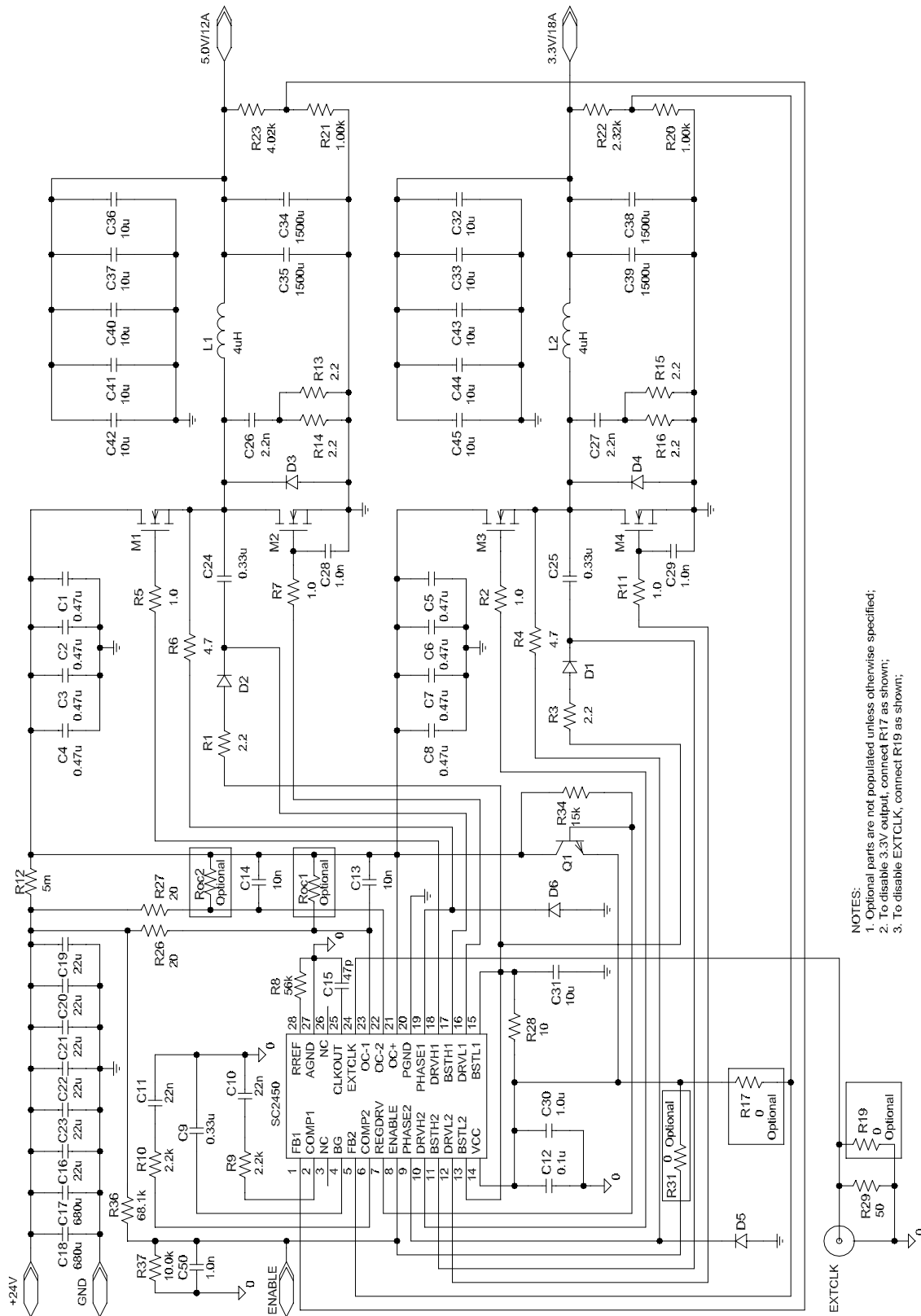
**POWER MANAGEMENT**
**Pin Descriptions**

| Pin | Pin Name | Pin Function   |
|-----|----------|--|
| 1   | FB1      | Feedback for channel 1.  |
| 2   | COMP1    | Compensation for channel 1.  |
| 3   | NC       | No connection.   |
| 4   | BG       | 1V reference for error amplifiers, 3K source impedance.                            |
| 5   | FB2      | Feedback for channel 2.  |
| 6   | COMP2    | Compensation for channel 2.  |
| 7   | REGDRV   | Regulator drive for external pass transistor.                                      |
| 8   | ENABLE   | Enable threshold is 2.05 V, connect to ground to disable.                          |
| 9   | PHASE2   | Phase node input for channel 2.  |
| 10  | DRVH2    | Gate drive for high side channel 2.  |
| 11  | BSTH2    | Bootstrap input for high side channel 2.   |
| 12  | DRVL2    | Gate drive for low side channel 2.   |
| 13  | BSTL2    | Supply for low side channel 2.   |
| 14  | VCC      | Pre-regulated IC power supply.   |
| 15  | BSTL1    | Supply for low side channel 1.   |
| 16  | DRVL1    | Gate drive for low side channel 1.   |
| 17  | BSTH1    | Bootstrap input for high side channel 1.   |
| 18  | DRVH1    | Gate drive for high side channel 1.  |
| 19  | PHASE1   | Phase node input for high side channel 1.  |
| 20  | PGND     | Power ground.  |
| 21  | OC+      | Overcurrent comparator inverting input.  |
| 22  | OC-2     | Overcurrent comparator non-inverting input for channel 2.                          |
| 23  | OC-1     | Overcurrent comparator non-inverting input for channel 1.                          |
| 24  | EXTCLK   | External clock, converter locks to this input when a valid signal is present.      |
| 25  | CLKOUT   | Clock out, logic level drive to provide synchronizing signal for other converters. |
| 26  | NC       | No connection.   |
| 27  | AGND     | Analog ground.   |
| 28  | RREF     | External reference resistor for internal oscillator and ramp generator.            |

## POWER MANAGEMENT

### Typical Application

#### Schematic for Two Channel Operation



- NOTES:
1. Optional parts are not populated unless otherwise specified;
  2. To disable 3.3V output, connect R17 as shown;
  3. To disable EXTCLK, connect R19 as shown;

**POWER MANAGEMENT**
**Typical Application (Cont.)**
**Bill of Material for Two Channel Operation**

| Item | Qty | Reference                                   | Part Number/Value                     | Manufacturer                           |
|------|-----|---|---------------------------------------|--|
| 1    | 8   | C1 - C8                                     | 0.47 $\mu$ F, 50V, Cer.               | Any                                    |
| 2    | 3   | C9,C24,C25                                  | 0.33 $\mu$ F, Cer., 1206              | Any                                    |
| 3    | 2   | C10,C11                                     | 22nF, Cer., 1206                      | Any                                    |
| 4    | 1   | C12   | 0.1 $\mu$ F, Cer., 1206               | Any                                    |
| 5    | 2   | C13,C14                                     | 10nF, Cer., 1206                      | Any                                    |
| 6    | 1   | C15   | 47pF, Cer., 1206                      | Any                                    |
| 7    | 6   | C16,C19,C20,C21,C22,C23                     | 22 $\mu$ F, 35V, Tant.                | Any                                    |
| 8    | 2   | C17,C18                                     | 680 $\mu$ F, 35V, Alum.               | Any                                    |
| 9    | 2   | C26,C27                                     | 2.2nF, Cer., 1206                     | Any                                    |
| 10   | 3   | C28,C29,C50                                 | 1.0nF, Cer., 1206                     | Any                                    |
| 11   | 1   | C30   | 1.0 $\mu$ F, Cer., 1206               | Any                                    |
| 12   | 11  | C31,C32,C33,C36,C37,C40,C41,C42,C43,C44,C45 | 10 $\mu$ F, Cer., 1206                | Any                                    |
| 13   | 4   | C34,C35,C38,C39                             | 1500 $\mu$ F, 6.3V, Alum.             | Any                                    |
| 14   | 4   | D1,D2,D5,D6                                 | 1A, 40V, Schottky, MELF,<br>1N5819M   | Any                                    |
| 15   | 2   | D3,D4                                       | 3A, 40V, Schottky, 30BQ040            | Any                                    |
| 16   | 2   | L1,L2                                       | Inductor, 9 turns                     | Magnetics:<br>Kool Mu<br>P/N: 77206-A7 |
| 17   | 4   | M1,M2,M3,M4                                 | N-Channel MOSFET, TO-<br>263AB        | Fairchild<br>P/N: FDB7030BL            |
| 18   | 1   | Q1  | 80V, 1A, NPN, Med. Pwr.<br>SOT-223    | BCP56CT                                |
| 19   | 2   | R1,R3                                       | 2.2, 5%, 1206                         | Any                                    |
| 20   | 2   | R4,R6                                       | 4.7, 5%, 1206                         | Any                                    |
| 21   | 4   | R2,R5,R7,R11                                | 1.0, 5%, 1206                         | Any                                    |
| 22   | 1   | R8  | 56k, 5%, 1206                         | Any                                    |
| 23   | 2   | R9,R10                                      | 2.2k, 5%, 1206                        | Any                                    |
| 24   | 1   | R12   | Chip resistor,<br>0.005, 1W, 1%, 2512 | Any                                    |

**POWER MANAGEMENT**
**Typical Application (Cont.)**
**Bill of Material for Two Channel Operation (Cont.)**

| Item | Qty | Reference       | Part Number/Value                   | Manufacturer                                    |
|------|-----|-----------------|-------------------------------------|---|
| 25   | 4   | R13,R14,R15,R16 | 2.2, 1/4W, 5%, 1210                 | Any   |
| 26   | 1   | R17*,R19,R31*   | Chip resistor, 0, 1206              | Any   |
| 27   | 2   | R20,R21         | 1.00k, 1%, 1206                     | Any   |
| 28   | 1   | R22             | 2.32k, 1%, 1206                     | Any   |
| 29   | 1   | R23             | 4.02k, 1%, 1206                     | Any   |
| 30   | 2   | R26,R27         | 20, 5%, 1206                        | Any   |
| 31   | 1   | R28             | 10, 5%, 1206                        | Any   |
| 32   | 1   | R29             | 51, 5%, 1206                        | Any   |
| 33   | 1   | R34             | 15k, 5%, 1206                       | Any   |
| 34   | 1   | R36             | 68.1k, 1%, 1206                     | Any   |
| 35   | 1   | R37             | 10.0k, 1%, 1206                     | Any   |
| 36   | 0   | Roc1*,Roc2*     | TBD, 1%, 1206                       | Any   |
| 37   | 1   | SC2450          | Bi-Phase/Dual Controller,<br>SO-28W | Semtech Corp.<br>P/N: SC2450ISW<br>805-498-2111 |

**Notes:**

1. \* Indicates optional parts.
2. Some parts are selected due to availability or lead time, and are not optimized.



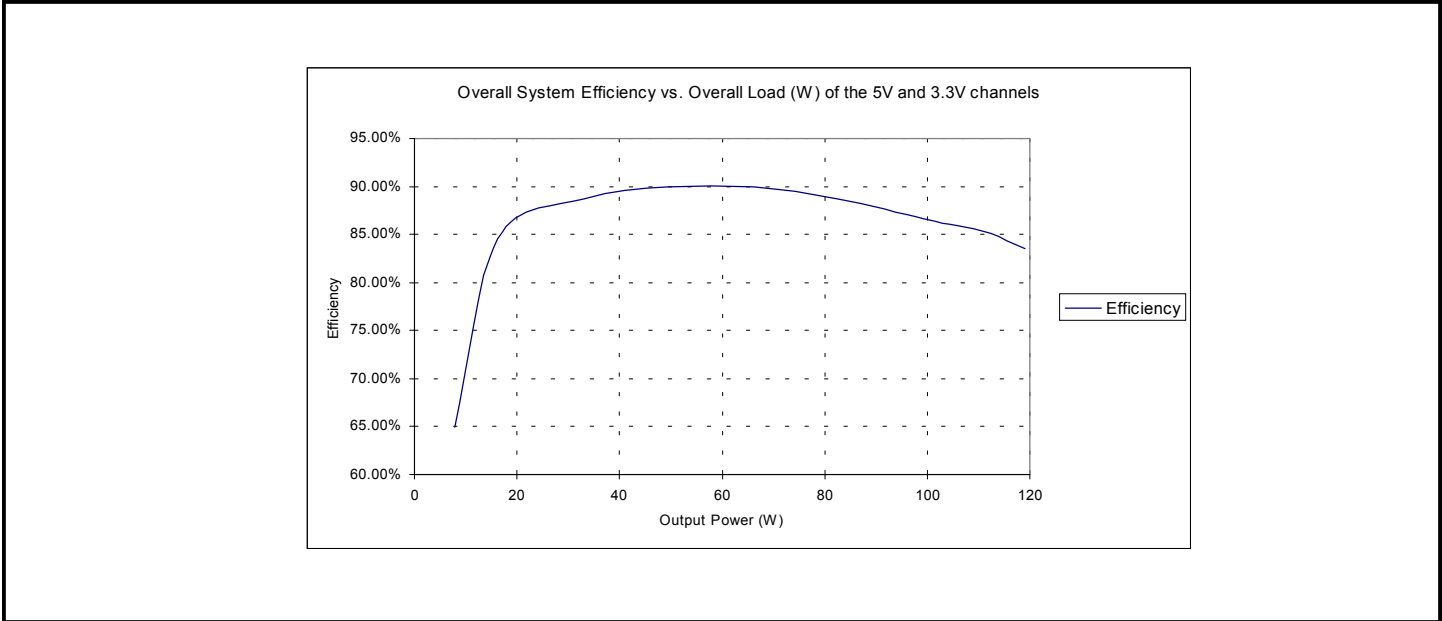


**POWER MANAGEMENT**

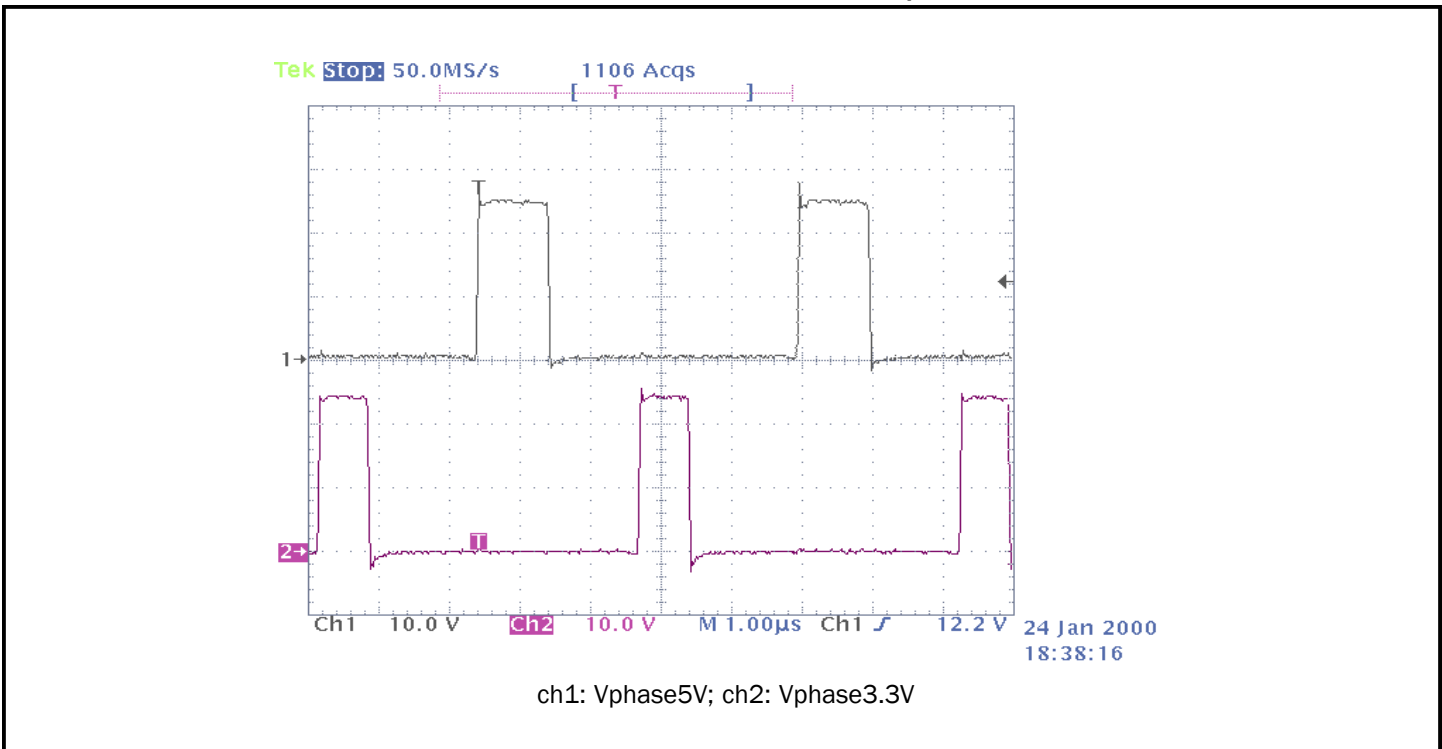
**Electrical Characteristic Curves**

**Two Channel Operation**

**Efficiency in Two-Channel Application Circuit (5V/12A, 3.3V/18A)**



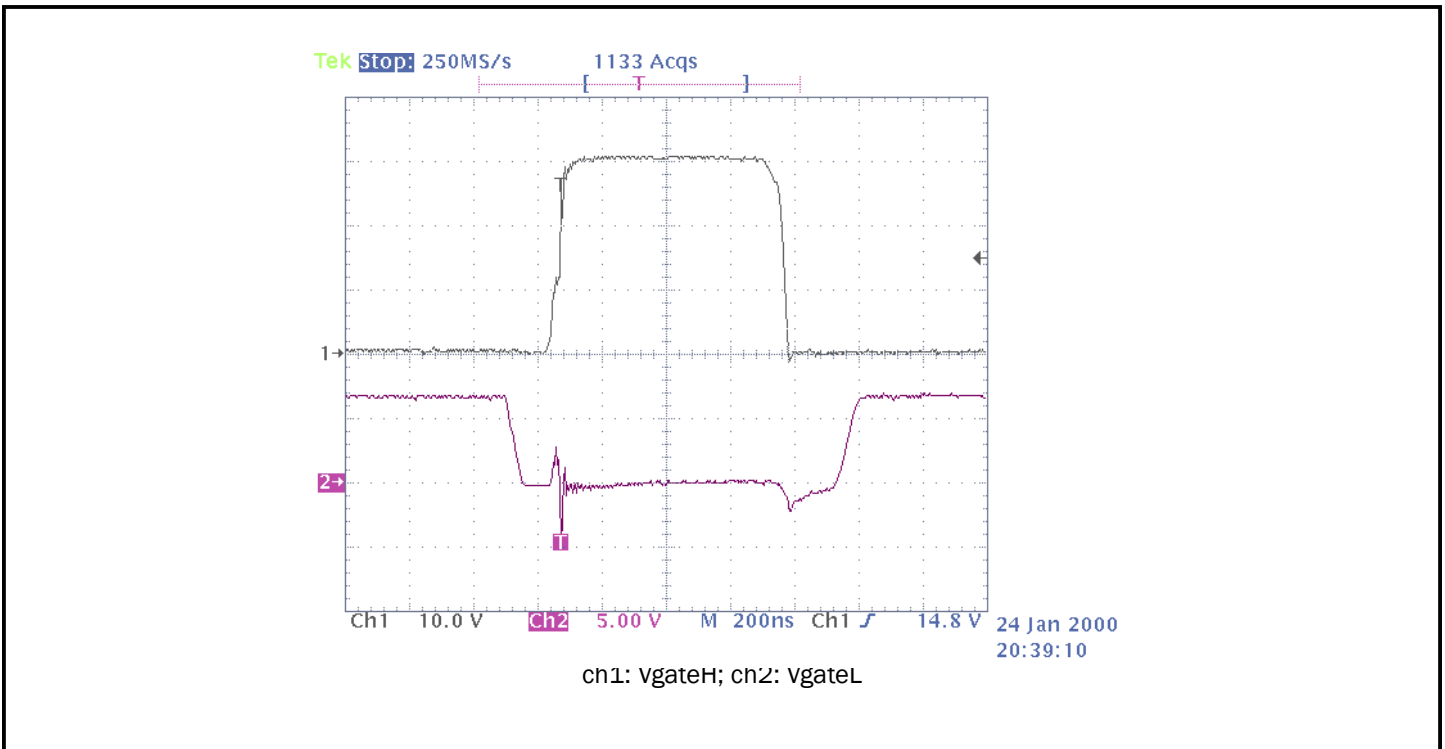
**Phase Node Waveform of Two-Channel Application Circuit (Vin = 24V, Load Current = 12A for 5V, Load Current = 18A for 3.3V)**



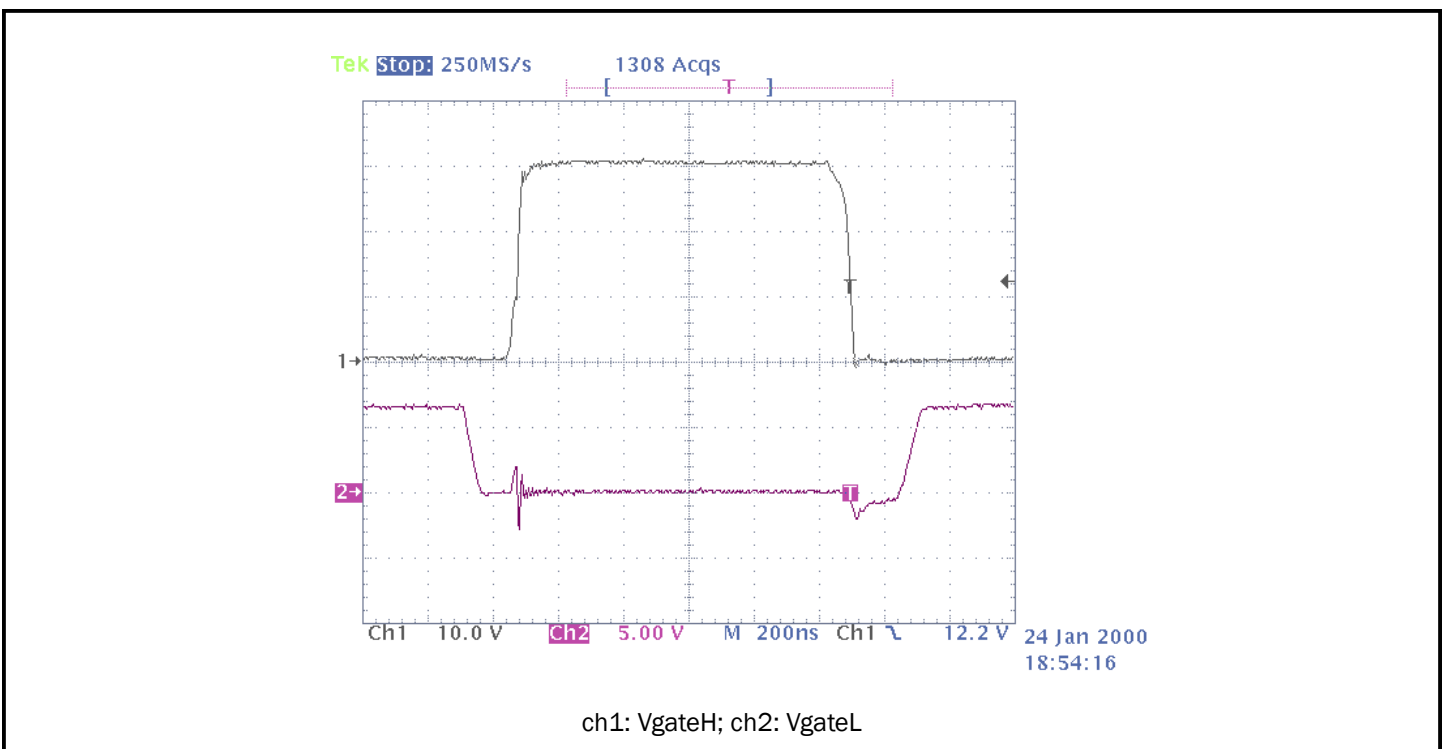
## POWER MANAGEMENT

### Electrical Characteristic Curves (Cont.)

#### 3.3V Channel Gate Waveform (Vin = 24V, Load Current = 18A)



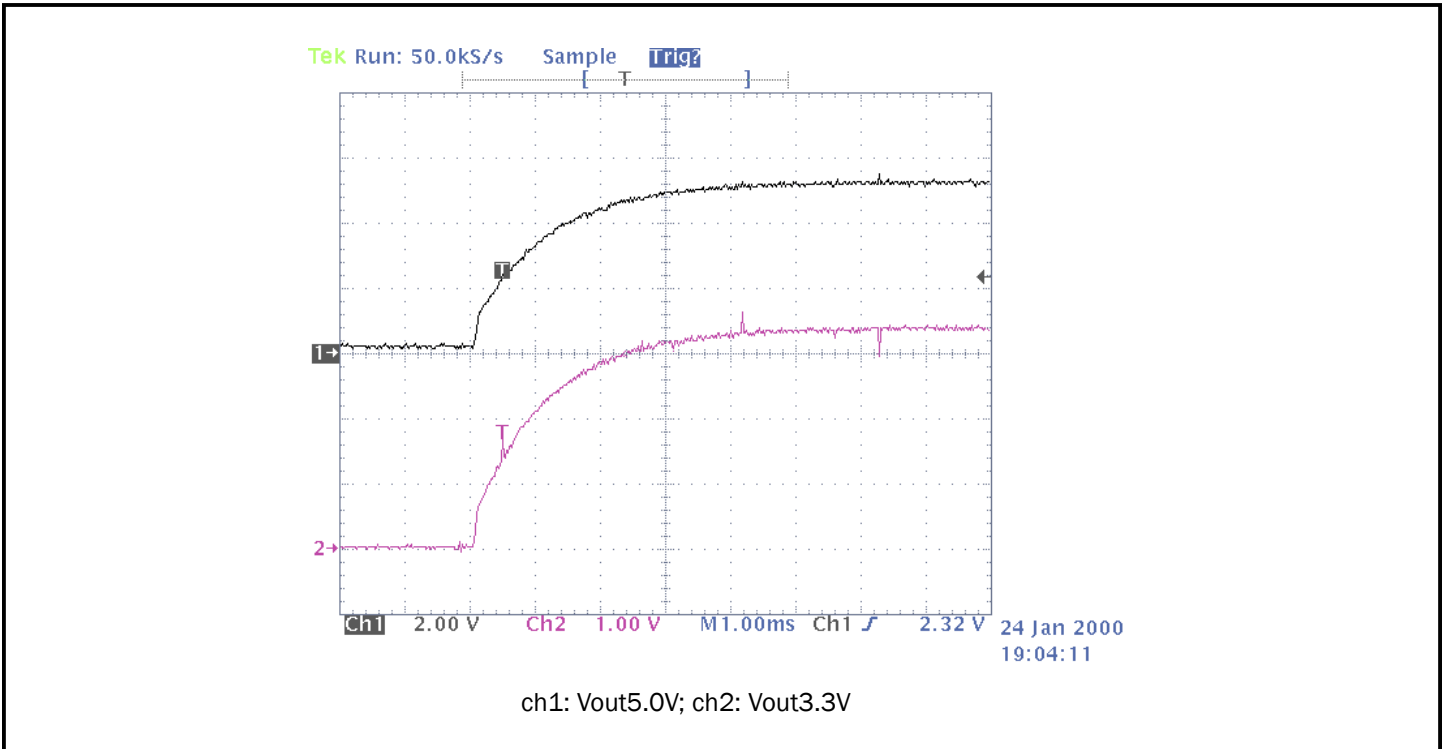
#### 5.0V Channel Gate Waveform (Vin = 24V, Load Current = 12A)



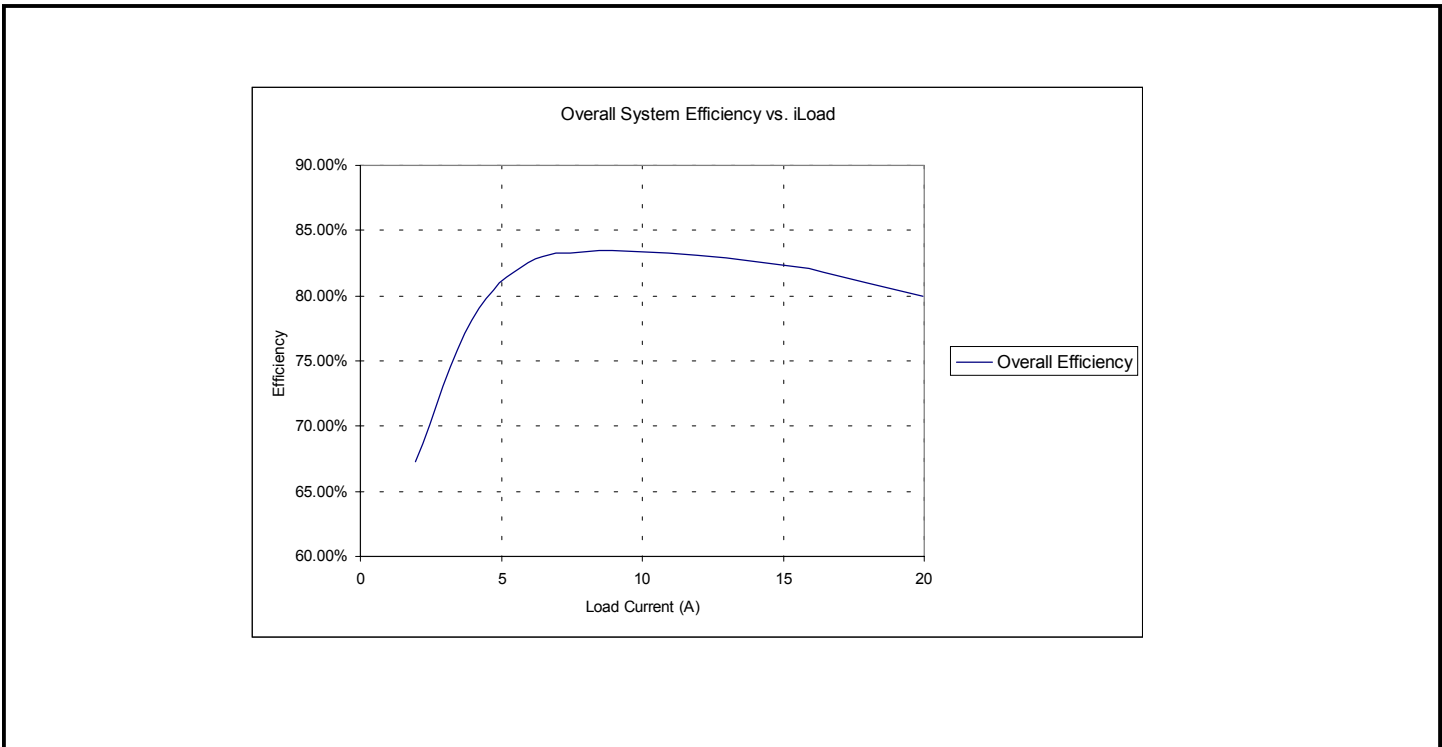
**POWER MANAGEMENT**

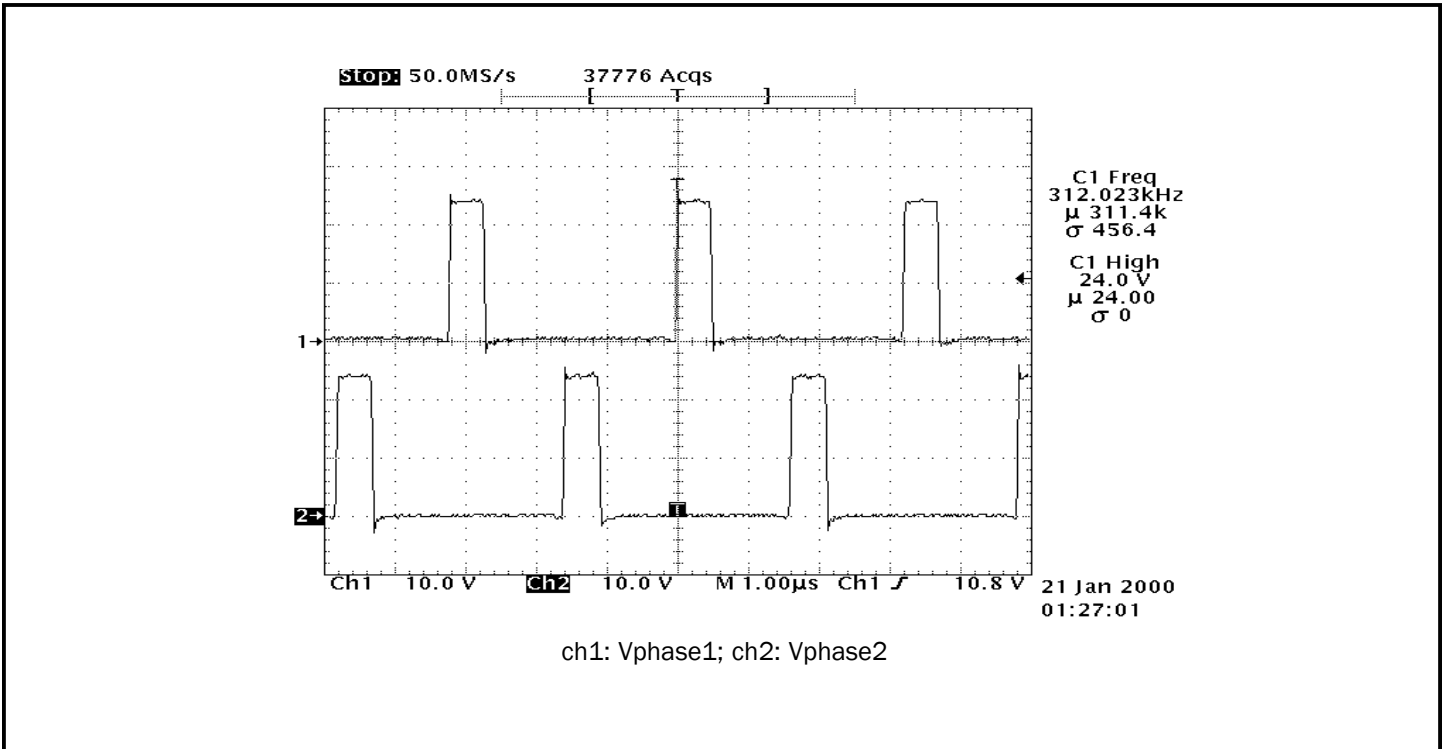
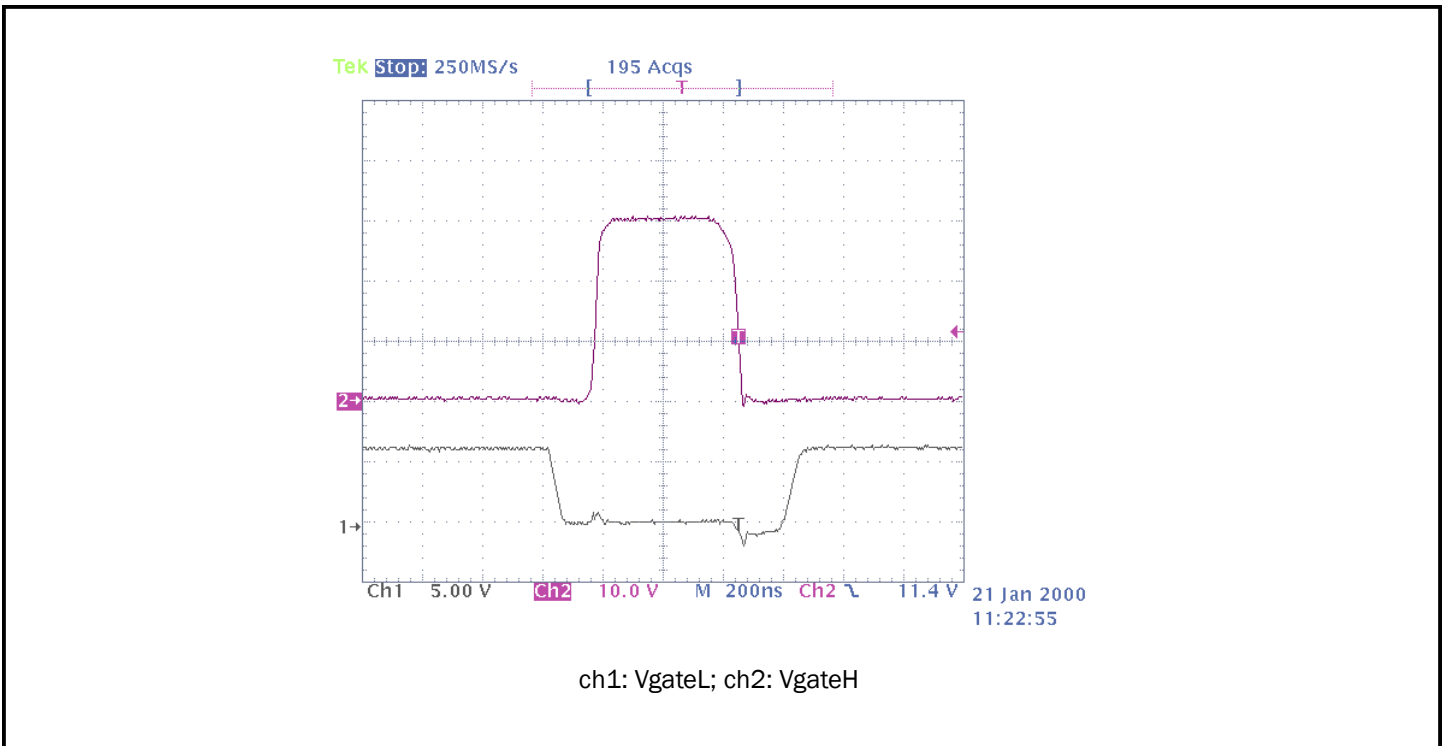
**Electrical Characteristic Curves (Cont.)**

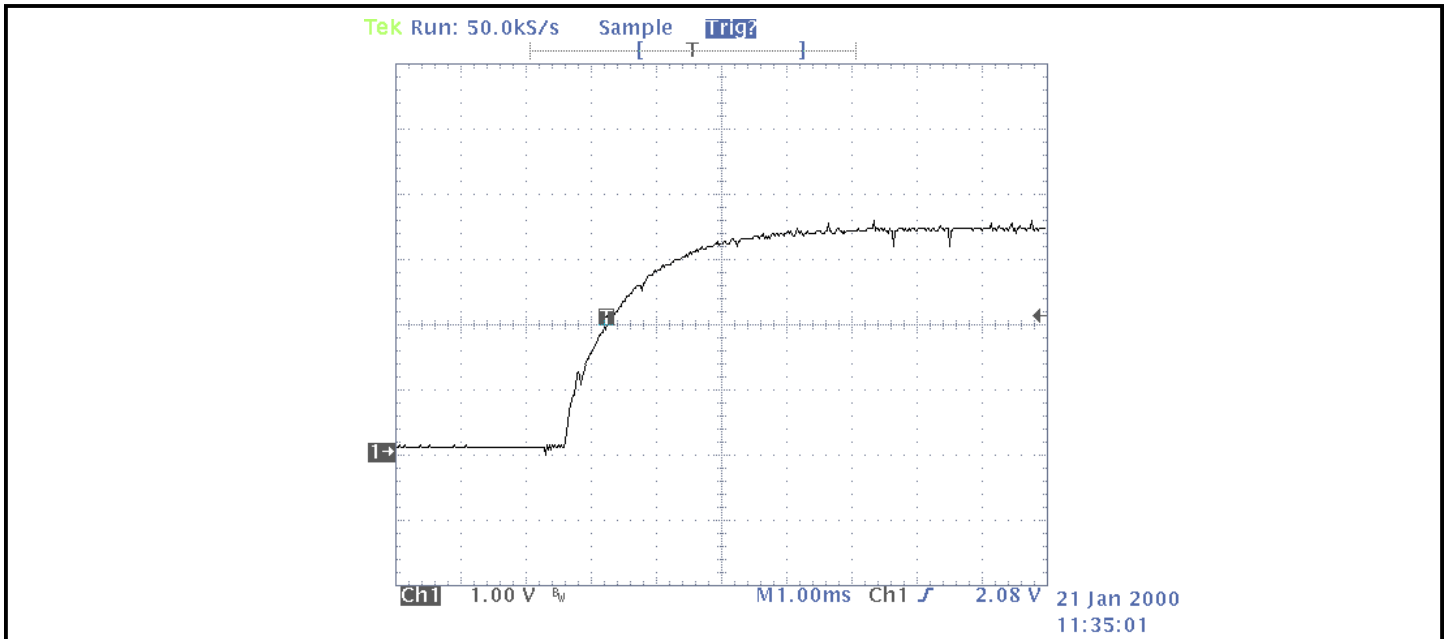
**Start-up ( $V_{in} = 24V$ ,  $V_{out1} = 5.0V/12A$ ,  $V_{out2} = 3.3V /18A$ )**



**Bi-Phase Operation ( $V_{out} = 3.3V$ , Max. Load Current = 20A)**  
**Efficiency in Bi-Phase Application Circuit (3.3V/20A)**



**POWER MANAGEMENT**
**Electrical Characteristic Curves (Cont.)**
**Phase Node Waveform (Vin = 24V, Vout = 3.3V, Load Current = 20A)**

**Gate Waveform (Vin = 24V, Vout = 3.3V, Load Current = 10A/phase)**


**POWER MANAGEMENT**
**Electrical Characteristic Curves (Cont.)**
**Start-up ( $V_{in} = 24V$ ,  $V_{out} = 3.3V$ , Load Current = 5A/phase)**

**Theory of Operation**

The SC2450 employs a voltage mode control with feed forward to provide fast output response to load and line transients.

The SC2450 has two outputs, which can be used to generate two separate supply voltages or can be combined in bi-phase operation to generate one single supply voltage. The internal reference is trimmed to 1 V with +/-1% accuracy, and the outputs voltages can be adjusted by two external resistors. In bi-phase operation, the dual switching regulators are operated 180° out of phase. Load current sharing between phases is normally required, and this can be achieved by using precise feedback voltage divider resistors (typically 0.1%) to match individual phase output voltage. In addition, small drooping resistors (could be PCB traces) are employed at the output of each phase to enhance phase current balance.

**PWM Control**

Changes on the output voltages are fed to the inverting input of the Error Amplifiers, by the FB1 and FB2 pins, and compared with the internal 1 V reference. The compensation to the transconductance amplifier is achieved by connecting a capacitor in series with a resistor from the COMP1 and COMP2 pins to AGND respectively. The error signal from the error amplifier is compared to the saw tooth waveform by the PWM comparator, and

matched timing signal is generated to control the upper and lower gate drives of the two phases. A single Ramp signal is used to generate the control signals for both of phases, hence the maximum duty cycle is less than 50%.

**Oscillator Frequency Selection**

The sawtooth signal is generated by charging an internal capacitor with a current source. The charge current is set by an external resistor connected from the RREF pin to AGND. The oscillator frequency and the external resistance follow an inversely proportional relationship.

**Feed Forward**

The SC2450 incorporates a voltage feed forward scheme to improve line transient immunity when changes of the input voltage occur. As the input voltage changes, the ramp valley to peak voltage of the internal oscillator follows this change instantly. As a result the output voltage will have minimum disturbance due to the input line change.

**Synchronized Operation**

The internal oscillator can be synchronized to an external clock operating in the range of 270 kHz to 1 MHz. The switching frequency of each channel is one half of the oscillator frequency. The oscillator clock is also available externally through the CLKOUT pin and can be used to provide synchronization for other converters.

**POWER MANAGEMENT****Theory of Operation (Cont.)****Bias Generation**

A 6-7 Volt supply voltage is required to power up the SC2450. This voltage could be provided by an external power supply or derived from VIN through an external pass transistor. REGDRV is the control signal to the base of the pass transistor that will regulate VCC. The voltage at the VCC pin is compared to the internal voltage reference, and the REGDRV pin can sink up to 5 mA current to regulate the voltage at the VCC pin.

**Enable**

If the ENABLE pin is connected to logic high, the SC2450 is enabled, while connecting it to ground will put the device into disabled mode. The ENABLE pin can also be configured as input UVLO through input voltage divider resistors. The controller will be enabled when the ENABLE pin voltage reaches 2.05 V, and will be disabled with 400 mV hysteresis.

**Under Voltage Lockout**

Under Voltage lockout (UVLO) circuitry senses VCC through a voltage divider. If this signal falls below 5.8 V, with a typical hysteresis of 400 mV, the BG pin is pulled low by an internal transistor causing the lower MOSFET gate to be on and the upper MOSFET gate off for both phases.

**Over Voltage Protection**

The SC2450 provides OVP protection for each output individually. Once the converter output voltage exceeds 120% nominal output voltage, the lower MOSFET gates are latched on and the upper MOSFET gates are latched off. The latch is then reset once the OVP condition is removed.

**Soft Start**

An external capacitor at the BG pin is used to set up the Soft Start duration. The capacitor value, in conjunction with the internal 3K resistor at the BG pin, control the duration to bring up the bandgap to its final level. As the BG capacitor is being charged through the internal resistor, the PWM pulse opens accordingly until the bandgap is charged completely. This controlled start up of the PWM prevents output voltage overshoot, unnecessary component stress, and noise generation during start up.

**Over Current Protection**

The SC2450 current limit provides protection during an over current condition. A sense resistor or PCB trace can be used to sense the input supply current.

The over current protection trip point is determined by the voltage drop across the sense resistor. Once this voltage drop exceeds 115 mV, OCP protection circuit will be triggered. Due to component and layout parasitics, filtering might be necessary across the OC+ and OC- pins. It is recommended to use 20 Ohm resistor and 10 nF capacitor for filtering. The OCP accuracy may be affected by non-ideal PCB layout and MOSFET variations. To accommodate these variations, the OCP threshold can be externally adjusted by a voltage divider across the sense resistor to attenuate the voltage drop across the sense resistor, so that increase the OCP threshold accordingly. See application circuits.

Once an over current condition occurs, the lower MOSFET gates are latched on and the upper MOSFET gates are latched off. The latch is then reset at the beginning of the next clock cycle. The cycle is repeated indefinitely until the over current condition removed.

**Thermal Shutdown**

In addition to current limit, the SC2450 monitors over temperature condition. The over temperature detection will shut down the part if the SC2450 die temperature exceeds 150°C, and will auto reset once the die temperature is dropped down.

**Gate Drive**

The SC2450 integrates high current gate drivers for fast switching of large MOSFETs. The high-side gates can be switched with peak currents of 1 Amp, while the larger low-side gates can be switched with peak currents of 2 Amps. A cross conduction prevention circuitry ensures a non-overlapping operation between the Upper and Lower MOSFETs. This prevents false current limit tripping and provides high efficiency.

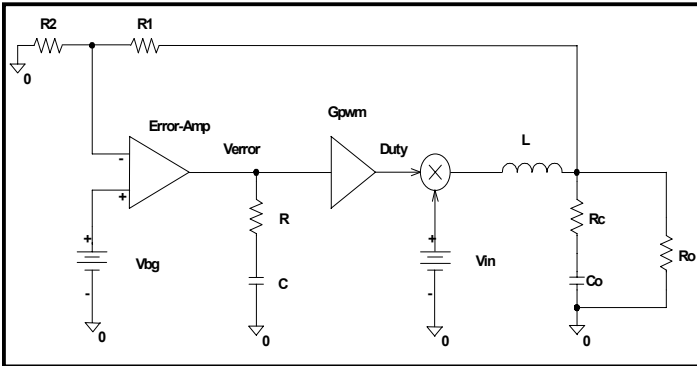
**POWER MANAGEMENT**
**Control Loop Design**


Fig. 1. SC2450 control model.

The control model of SC2450 can be depicted in Fig. 1. This model can also be used in Spice kind of simulator to generate loop gain Bode plots. The bandgap reference is 1 V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2.

The error amplifier is transconductance type with fixed gain of:

$$G_{\text{ERROR}} := 0.002 \frac{\text{A}}{\text{V}}$$

The compensation network includes a resistor and a capacitor in series, which terminates from the output of the error amplifier to the ground.

This device uses voltage mode control with input voltage feed forward. The peak-to-peak ramp voltage is proportional to the input voltage, which results in an excellent performance to reject input voltage variation. The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{\text{PWM}} := \frac{1}{V_{\text{RAMP}}}$$

where the ramp amplitude (peak-to-peak) is 3 volts when input voltage is 24 volts.

The total control loop-gain can then be derived as follows:

$$T(s) = T_o \cdot \left( \frac{1 + s \cdot R \cdot C}{s \cdot R \cdot C} \right) \cdot \frac{1 + s \cdot R_c \cdot C_o}{1 + s \cdot \left( R_c \cdot C_o + \frac{L}{R_o} \right) + s^2 \cdot L \cdot C_o \cdot \left( 1 + \frac{R_c}{R_o} \right)}$$

where

$$T_o = G_{\text{error}} \cdot V_{\text{in}} \cdot G_{\text{pwm}} \cdot R \cdot \left( \frac{R_2}{R_1 + R_2} \right)$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

- (1) Calculate the corner frequency of the output filter:

$$F_o := \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$$

- (2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{\text{esr}} := \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o}$$

- (3) Check that the ESR zero frequency is not too high.

$$F_{\text{ers}} < \frac{F_{\text{SW}}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

- (4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency or the output ripple frequency in bi-phase mode operation:

$$F_{\text{x\_OVER}} \leq \frac{F_{\text{SW}}}{5}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R := \frac{1}{G_{\text{pwm}} \cdot V_{\text{in}} \cdot G_{\text{error}}} \cdot \left( \frac{F_{\text{esr}}}{F_o} \right)^2 \cdot \left( \frac{F_{\text{x\_over}}}{F_{\text{esr}}} \right) \cdot \left( \frac{V_o}{V_{\text{bg}}} \right)$$

when:

$$F_o < F_{\text{esr}} < F_{\text{x\_over}}$$



**POWER MANAGEMENT**
**Control Loop Design (Cont.)**

or

$$R := \frac{1}{G_{pwm} \cdot V_{in} \cdot G_{error}} \cdot \left( \frac{F_o}{F_{esr}} \right)^2 \cdot \left( \frac{F_{x\_over}}{F_o} \right) \cdot \left( \frac{V_o}{V_{bg}} \right)$$

when

$$F_{esr} < F_o < F_{x\_over}$$

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} := \frac{F_o}{5}$$

$$C := \frac{1}{2 \cdot \pi \cdot R \cdot F_{zero}}$$

(6) The final step is to generate the Bode plot, either by using the simulation model in Fig. 1 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot. Usually, this design procedure ensures a healthy phase margin.

An example is given below to demonstrate the procedure introduced above. The parameters of the power supply are given as:

$$V_{in} := 24 \text{ V}$$

$$V_o := 2.5 \text{ V}$$

$$I_o := 20 \text{ A}$$

$$F_{sw} := 150 \text{ KHz}$$

$$L := 4 \text{ } \mu\text{H}$$

$$C_o := 3000 \text{ } \mu\text{F}$$

$$R_c := 0.02 \text{ } \Omega$$

$$R_1 := 1.5 \text{ K}\Omega$$

$$R_2 := 1.0 \text{ K}\Omega$$

Step 1. Output filter corner frequency

$$F_o = 1.453 \text{ KHz}$$

Step 2. ESR zero frequency:

$$F_{esr} = 2.653 \text{ KHz}$$

Step 3. Check the following condition:

$$F_{esr} < \frac{F_{sw}}{5}$$

Which is satisfied in this case.

Step 4. Choose crossover frequency and calculate compensator R:

$$F_{x\_over} = 30 \text{ KHz}$$

$$R = 5.89 \text{ K}\Omega$$

Step 5. Calculate the compensator C:

$$C = 92.98 \text{ nF}$$

Step 6. Generate Bode plot and check the phase margin. In this case, the phase margin is about 85°C that ensures the loop stability. Fig. 2 shows the Bode plot of the loop.

**POWER MANAGEMENT**

**Control Loop Design (Cont.)**

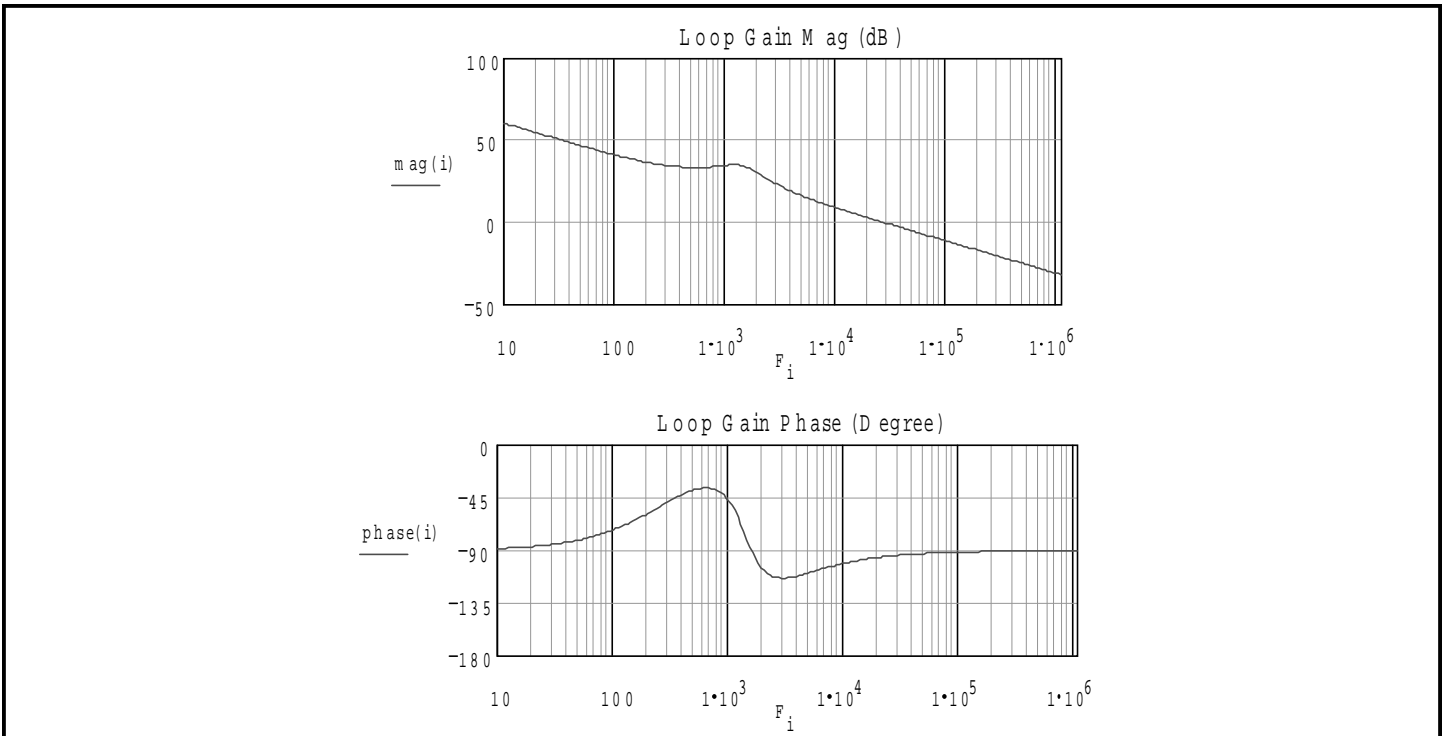


Fig. 2. Bode plot of the loop

**Layout Guidelines**

Good layout is necessary for successful implementation of the SC2450 bi-phase/dual controller. Important layout guidelines are listed below.

1). The high power parts should be laid out first. The parasitic inductance of the pulsating power current loop (start from positive end of the input capacitor, to top MOSFET, then to bottom MOSFET back to power ground) must be minimized. The high frequency input capacitors and top MOSFETs should be close to each other. The freewheeling Schottky diode, the bottom MOSFET snubber, and the bottom MOSFET should be placed close to each other. The MOSFET gate drive and current sense loop areas should be minimized. The gate drive trace should be short and wide.

2). The layout of the two phases should be made as symmetrical as possible. The SC2450 controller should be placed in the center of the two phases. Please see evaluation board layout as an example.

3). Separate ground planes for analog and power should

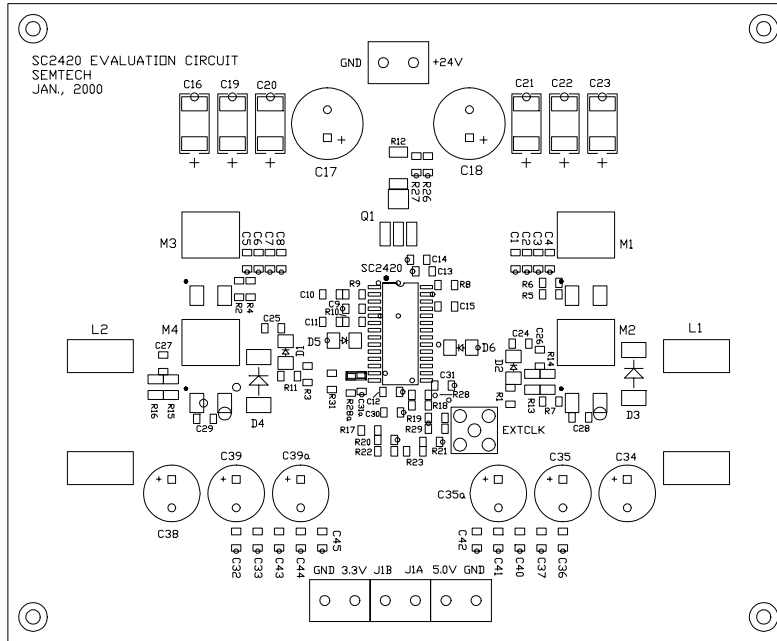
be provided. Power current should avoid running over the analog ground plane. The AGND is star connected to the PGND at the converter output to provide best possible ground sense. Refer to the application schematics, certain components should be connected directly to the AGND.

4). If a multi-layer PCB is used, power layer and ground layer are recommended to be adjacent to each other. Typically the power layer is on the top, followed by the ground layer. This results in the least parasitic inductance in the MOSFET-capacitor power loop, and reduces the ringing on the phase node. The rest of the layers could be used to run DC supply traces and signal traces.

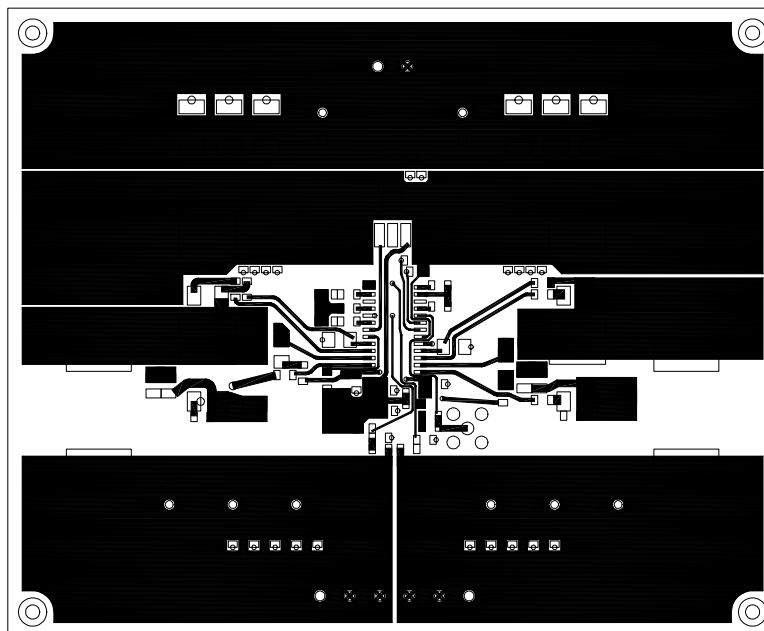
An example of a two-layer PCB layout is given below to illustrate these layout principles.

**POWER MANAGEMENT**

**Layout Guidelines (Cont.)**



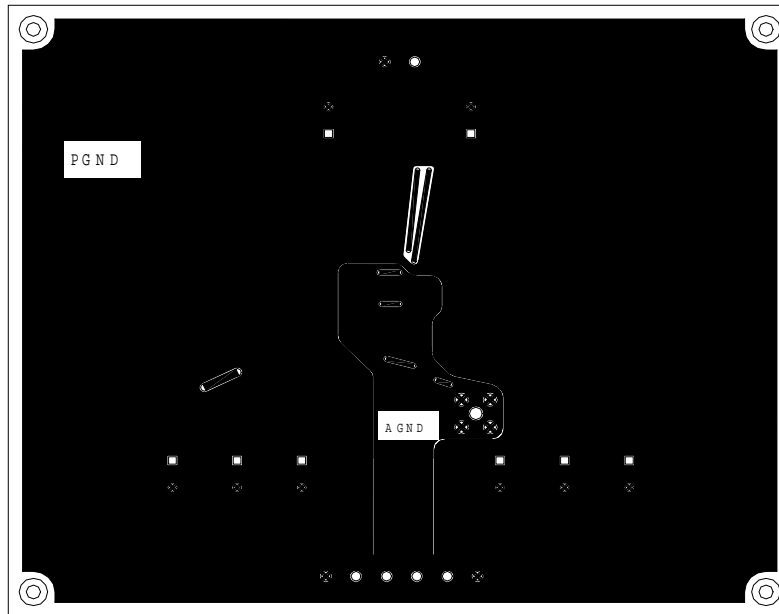
Component Side (TOP)



Copper (TOP)

**POWER MANAGEMENT**

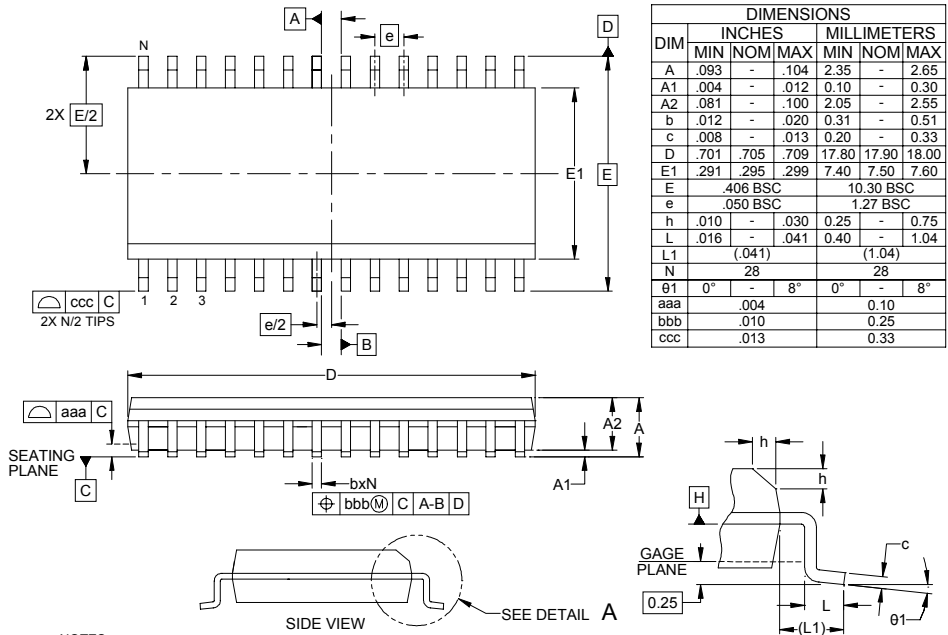
Layout Guidelines (Cont.)



Copper (BOTTOM)

**POWER MANAGEMENT**

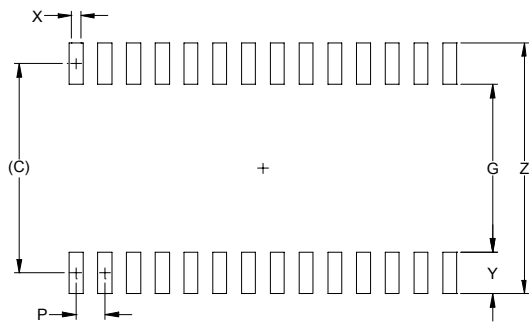
**Outline Drawing - SO-28**



| DIM | INCHES   |      |      | MILLIMETERS |       |       |
|-----|----------|------|------|-------------|-------|-------|
|     | MIN      | NOM  | MAX  | MIN         | NOM   | MAX   |
| A   | .093     | -    | .104 | 2.35        | -     | 2.65  |
| A1  | .004     | -    | .012 | 0.10        | -     | 0.30  |
| A2  | .081     | -    | .100 | 2.05        | -     | 2.55  |
| b   | .012     | -    | .020 | 0.31        | -     | 0.51  |
| c   | .008     | -    | .013 | 0.20        | -     | 0.33  |
| D   | .701     | .705 | .709 | 17.80       | 17.90 | 18.00 |
| E1  | .291     | .295 | .299 | 7.40        | 7.50  | 7.60  |
| E   | .406 BSC |      |      | 10.30 BSC   |       |       |
| e   | .050 BSC |      |      | 1.27 BSC    |       |       |
| h   | .010     | -    | .030 | 0.25        | -     | 0.75  |
| L   | .016     | -    | .041 | 0.40        | -     | 1.04  |
| L1  | (.041)   |      |      | (1.04)      |       |       |
| N   | 28       |      |      | 28          |       |       |
| θ1  | 0°       | -    | 8°   | 0°          | -     | 8°    |
| aaa | .004     |      |      | 0.10        |       |       |
| bbb | .010     |      |      | 0.25        |       |       |
| ccc | .013     |      |      | 0.33        |       |       |

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-013, VARIATION AE.

**Land Pattern - SO-28**



| DIM | INCHES | MILLIMETERS |
|-----|--------|-------------|
| C   | .362   | (9.20)      |
| G   | .276   | 7.00        |
| P   | .050   | 1.27        |
| X   | .024   | 0.60        |
| Y   | .087   | 2.20        |
| Z   | .449   | 11.40       |

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 307A.

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