TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HC4060AP,TC74HC4060AF

14-Stage Binary Counter/Oscillator

The TC74HC4060A is a high speed CMOS 14-STAGE BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The oscillator configuration allows designs using either RC or crystal oscillator circuits, or an external clock may be used.

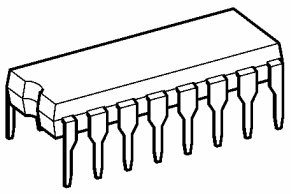
The clear input resets the counter to a low level on all outputs and disables the oscillator.

A high CLR accomplishes this reset function.

A negative transition on the clock input ($\overline{\varphi}$ I) increments the counter Ten levels of divided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. At the last stage (Q14), a 1/16384 divided frequency is obtained.

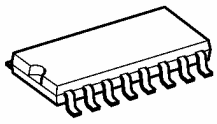
The $\overline{\varphi}$ I input and CLR input are equipped with protection circuits against static discharge or transient excess voltage.

TC74HC4060AP



DIP16-P-300-2.54A

TC74HC4060AF



SOP16-P-300-1.27A

Weight

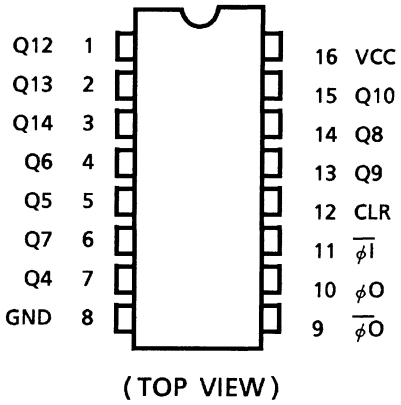
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Features

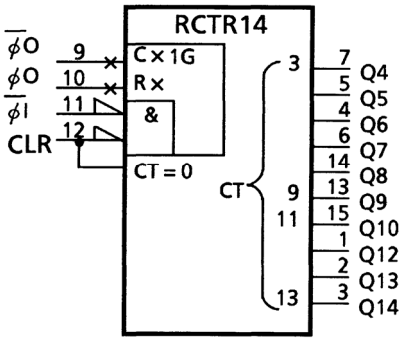
- High speed: f_{max} = 58 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Oscillator configuration: RC or crystal oscillator
- Pin and function compatible with 4060B

Pin Assignment



(TOP VIEW)

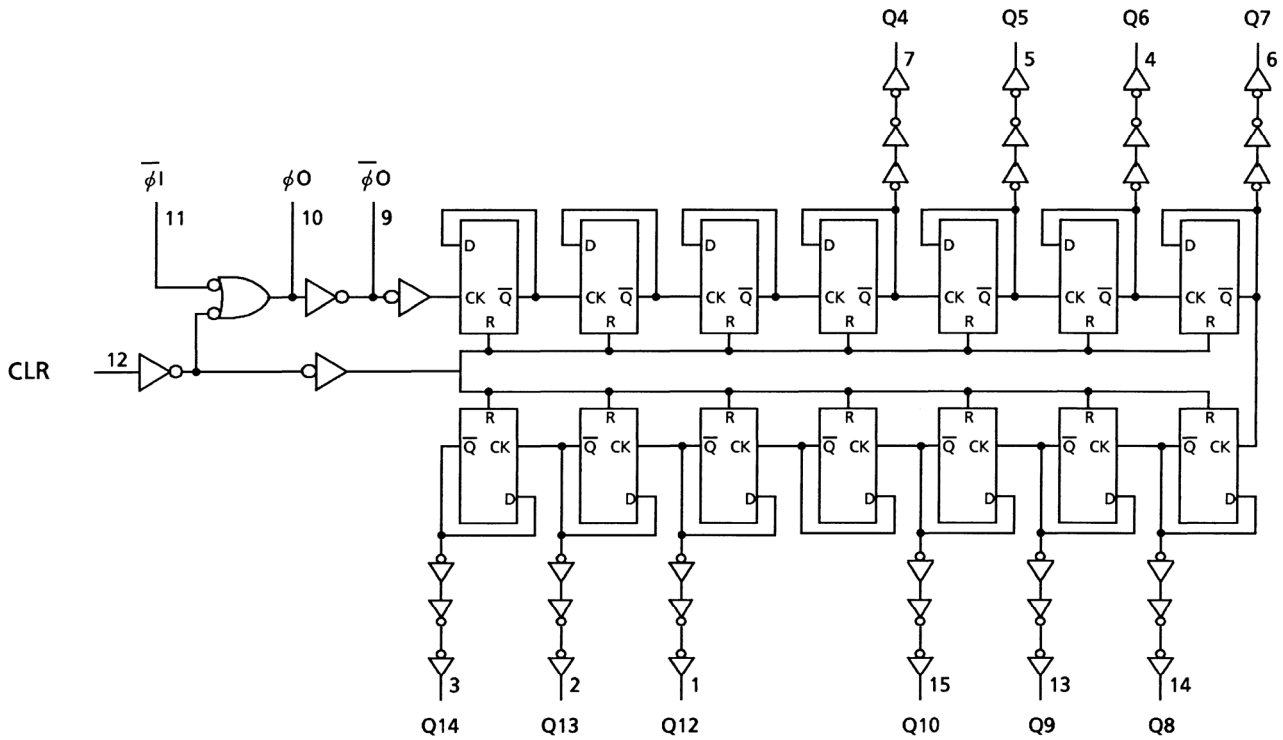
IEC Logic Symbol



Truth Table

Inputs		Function
$\overline{\phi}$I	CLR	
X	H	Counter is reset to zero state. ϕO output goes to high level. $\overline{\phi}$O output goes to low level.
↓	L	Count up one step.
↑	L	No Change

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Range (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage (Qn)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
High-level output voltage (ϕO, $\bar{\phi}$O)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.8	2.0	—	1.8	—	V
				4.5	4.0	4.5	—	4.0	—	
				6.0	5.5	5.9	—	5.5	—	
Low-level output voltage (Qn)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.0	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Low-level output voltage (ϕO, $\bar{\phi}$O)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.2	—	0.2	V
				4.5	—	0.0	0.5	—	0.5	
				6.0	—	0.1	0.5	—	0.5	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = −40 to 85°C	Unit
		V_{CC} (V)	Typ.	Limit		Limit	
Minimum pulse width ($\overline{\phi}$I)	$t_{W\ (L)}$ $t_{W\ (H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse time (CLR)	$t_{W\ (H)}$	—	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum removal time	t_{rem}	—	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	30	24	
			6.0	—	35	28	

AC Characteristics ($C_L = 15$ pF, $V_{CC} = 5$ V, Ta = 25°C, input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	—	—	4	8	ns
Propagation delay time ($\overline{\phi}$I -Q_4)	t_{pLH} t_{pHL}	—	—	36	53	ns
Propagation delay time difference (Qn-Qn + 1)	Δt_{pd}	C_L = 15 pF (Qn, Qn + 1)	—	6	14	ns
Propagation delay time (CLR)	t_{pHL}	—	—	19	34	ns
Maximum clock frequency	f_{max}	—	33	58	—	MHz

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	30	75	—	95	ns
			4.5	—	8	15	—	19	
			6.0	—	7	13	—	16	
Propagation delay time ($\bar{\phi}$I -Q_4)	t_{pLH} t_{pHL}	—	2.0	—	170	300	—	375	ns
			4.5	—	41	60	—	75	
			6.0	—	30	51	—	64	
Propagation delay time difference (Qn-Qn + 1)	Δt_{pd}	C_L = 50 pF (Qn, Qn + 1)	2.0	—	32	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	5	13	—	16	
Propagation delay time (CLR)	t_{pHL}	—	2.0	—	85	195	—	245	ns
			4.5	—	23	39	—	49	
			6.0	—	17	33	—	42	
Maximum clock frequency	f_{max}	—	2.0	6	12	—	5	—	MHz
			4.5	30	50	—	24	—	
			6.0	35	65	—	28	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note)		—	27	—	—	—	pF

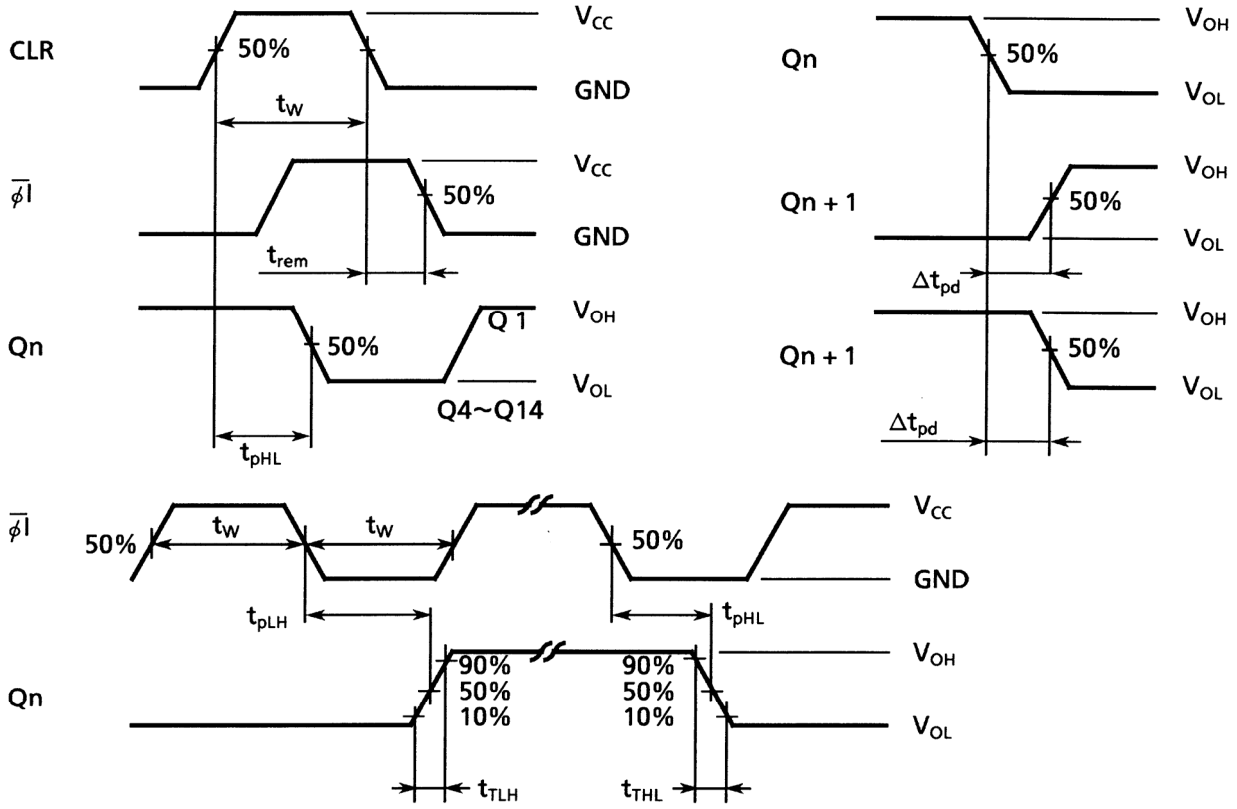
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

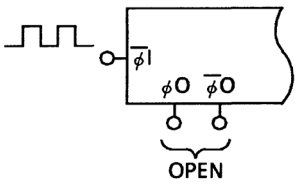
When CR or Crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the above calculation, because these oscillation circuits spend much supply current.

Switching Characteristics Test Waveform

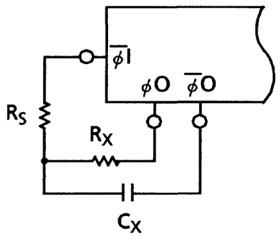


Typical Clock Drive Circuits

External Clock Drive

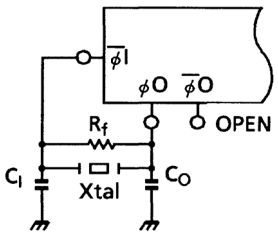


Typical RC Circuit



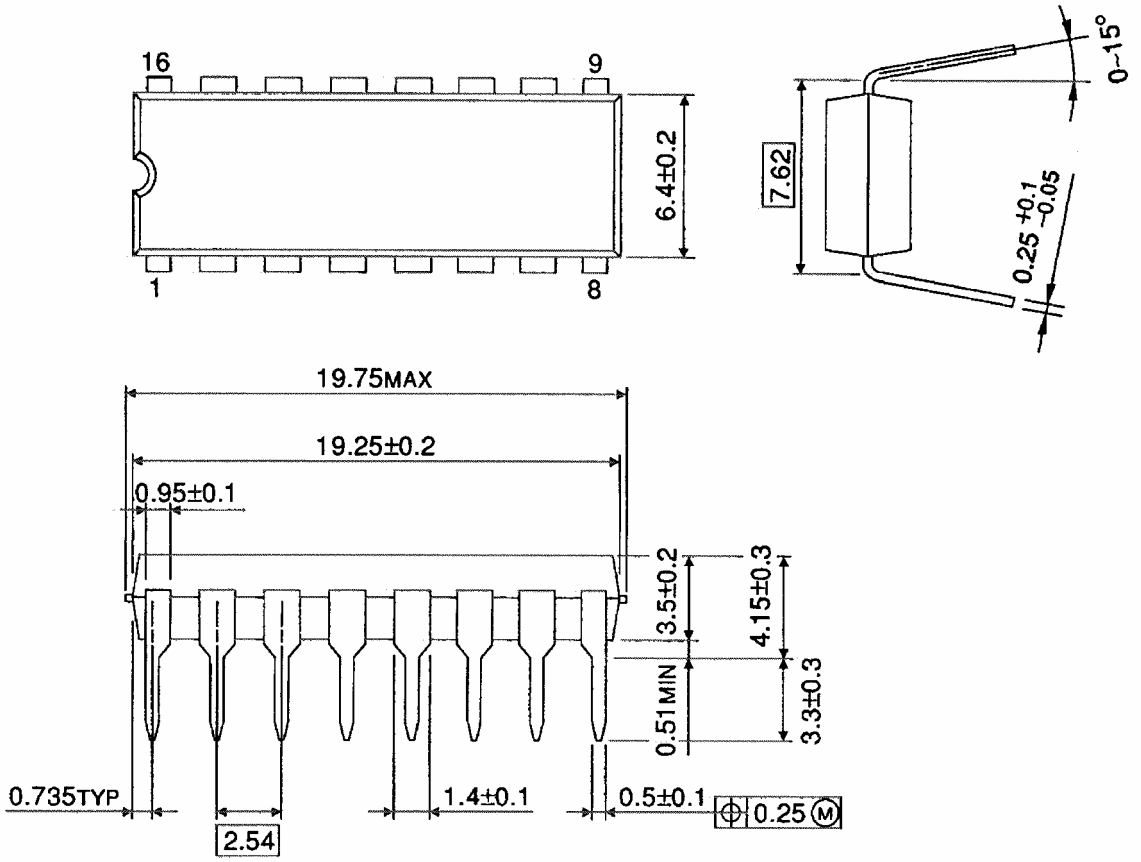
$R_S : 2R_X \sim 10R_X$

Typical Crystal Circuit



Package Dimensions

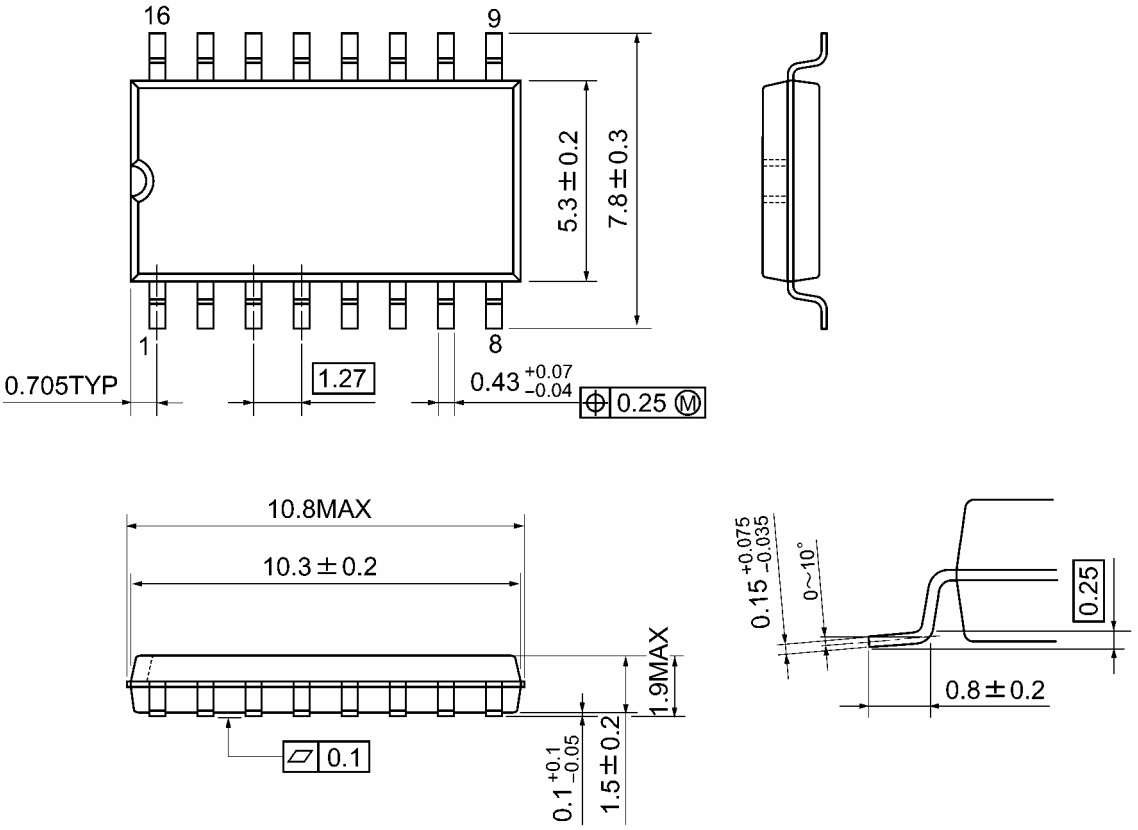
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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