TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74HC423AP,TC74HC423AF

#### **Dual Retriggerable Monostable Multivibrator**

The TC74HC423A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs,  $\overline{A}$  input (negative edge), and B input (positive edge). These inputs are valid for a slow rise/fall time signal (tr = tf = 1 s) as they are schmitt trigger inputs.

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the  $\overline{\text{CLR}}$  input breaks this state. In the MONOSTABLE state, if a new trigger is applied, it extends the MONOSTABLE period (retrigger mode).

Limitations for Cx and Rx are:

External capacitor, Cx: No limit

External resistor, Rx:  $V_{\rm CC}$  = 2.0 V more than 5  $k\Omega$ 

 $V_{CC} \ge 3.0 \text{ V}$  more than  $1 \text{ k}\Omega$ 

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

#### Features (Note)

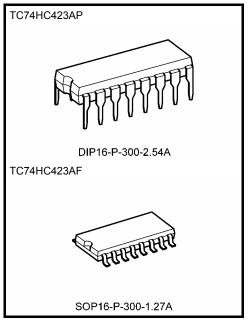
- High speed:  $t_{pd} = 25 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation

Standby state:  $I_{\rm CC}$  = 4  $\mu A$  (max) at Ta = 25°C

Active state:  $I_{\rm CC}$  = 700  $\mu A$  (max) at  $V_{\rm CC}$  = 5 V

- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: |I<sub>OH</sub>| = I<sub>OL</sub> = 4 mA (min)
- Balanced propagation delays:  $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range:  $V_{CC}$  (opr) = 2~6 V
- Pin and function compatible with 74LS423

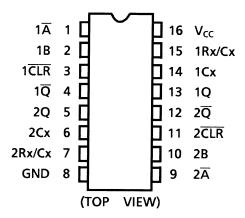
Note: In the case of using only one circuit,  $\overline{CLR}$  should be tied to GND,  $Rx/Cx \cdot Cx \cdot Q \cdot \overline{Q}$  should be tied to OPEN, the other inputs should be tied to  $V_{CC}$  or GND.



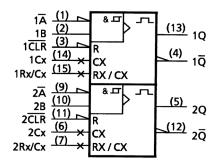
Weight

DIP16-P-300-2.54A : 1.00 g (typ.) SOP16-P-300-1.27A : 0.18 g (typ.)

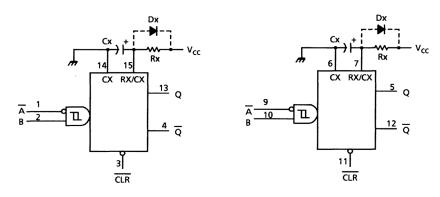
#### **Pin Assignment**



#### **IEC Logic Symbol**



#### **Block Diagram (Note 1)(Note 2)**



Note 1: Cx, Rx, Dx are external capacitor, resistor, and diode, respectively.

Note 2: External clamping diode, Dx;

The external capacitor is charged to  $V_{CC}$  level in the wait state, i.e. when no trigger is applied. If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and  $V_{CC}$  drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and  $V_{CC}$  drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is  $\pm 20$  mA.

In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \ge (V_{CC} - 0.7) Cx/20 mA$$

(tf is the time between the supply voltage turn off and the supply voltage reaching 0.4  $V_{CC}$ .)

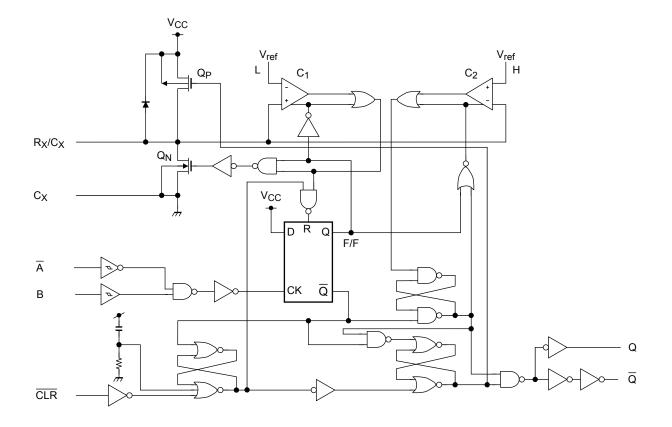
In the event a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from in rush current.

## **Truth Table**

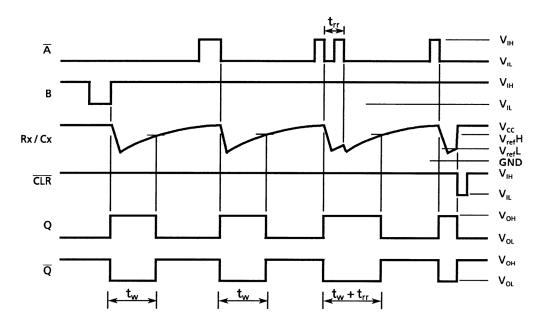
	Inputs		Out	puts	Note
Ā	В	CLR	Q	Q	Note
$\Box$	Н	Н	Л	T	Output Enable
Х	L	Η	L	Н	Inhibit
Н	Х	Н	L	Н	Inhibit
L		Н		Ţ	Output Enable
Х	Х	L	L	Н	Reset

X: Don't care

## **System Diagram**



#### **Timing Chart**



#### **Functional Description**

(1) Stand-by state

The external capacitor Cx is fully charged to  $V_{CC}$  in the stand-by state. That means, before triggering, the QP and QN transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in either of the following two cases. First, the condition where the  $\overline{A}$  input is low, and the B input has a rising signal; second, where the B input is high, and the  $\overline{A}$  input has a falling signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and QN is turned on. The external capacitor discharges through QN. The voltage level of the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and QN turns off. At that moment C1 stops but C2 continues operating.

After QN turns off, the voltage at the Rx/Cx starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx reaches Vref H, the IC returns to its MONOSTABLE state.

With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, tw (OUT), is as follows:

tw (OUT) =  $1.0 \cdot Cx \cdot Rx$ 

(3) Retrigger operation

When a new trigger is applied to input  $\overline{A}$  or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx/Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx

If the 2nd trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, trr (min), depends on VCC and Cx.

(4) Reset operation

In normal operation,  $\overline{\text{CLR}}$  input is held high. If  $\overline{\text{CLR}}$  is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, QP turns on and Cx is charged rapidly to  $\overline{\text{VCC}}$ 

This means if  $\overline{\text{CLR}}$  input is set low, the IC goes into a wait state.

#### **Absolute Maximum Ratings (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5~7	V
DC input voltage	V <sub>IN</sub>	-0.5~V <sub>CC</sub> + 0.5	V
DC output voltage	V <sub>OUT</sub>	-0.5~V <sub>CC</sub> + 0.5	٧
Input diode current	I <sub>IK</sub>	±20	mA
Output diode current	lok	±20	mA
DC output current	lout	±25	mA
DC V <sub>CC</sub> /ground current	Icc	±50	mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T <sub>stg</sub>	-65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of  $Ta = -40 \sim 65$ °C. From Ta = 65 to 85°C a derating factor of -10 mW/°C shall be applied until 300 mW.

#### **Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2~6	V
Input voltage	V <sub>IN</sub>	0~V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub> 0~V <sub>CC</sub>		٧
Operating temperature	T <sub>opr</sub>	-40~85	°C
Input rise and fall time ( CLR only)	t <sub>r</sub> , t <sub>f</sub>	0~1000 (V <sub>CC</sub> = 2.0 V) 0~500 (V <sub>CC</sub> = 4.5 V) 0~400 (V <sub>CC</sub> = 6.0 V)	ns
External capacitor	Cx	No limitation (Note 2)	F
External resistor	Rx	$\geq$ 5 k (V <sub>CC</sub> = 2.0 V) (Note 2) $\geq$ 1 k (V <sub>CC</sub> $\geq$ 3.0 V) (Note 2)	Ω

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC423A, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for  $Rx > 1 M\Omega$ .



### **Electrical Characteristics**

#### **DC Characteristics**

0	0 1 1	Test Condition		V <sub>CC</sub>	Ta = 25°C			Ta = -4	Unit		
Characteristics	Symbol					Тур.	Max	Min	Max	Ullit	
				2.0	1.50	_	_	1.50	_		
High-level input voltage	$V_{IH}$		_	4.5	3.15	_	_	3.15	_	V	
C				6.0	4.20	_	_	4.20	—		
				2.0	_	_	0.50	_	0.50		
Low-level input voltage	$V_{IL}$		_	4.5	_	_	1.35	_	1.35	V	
o de la companya de l				6.0	_	_	1.80	_	1.80		
				2.0	1.9	2.0	_	1.9	_		
High-level output		V <sub>IN</sub>	I <sub>OH</sub> = -20 μA	4.5	4.4	4.5	_	4.4	_		
voltage	V <sub>OH</sub>	= V <sub>IH</sub> or V <sub>IL</sub>		6.0	5.9	6.0	_	5.9	_	V	
(Q, Q)			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	_	4.13	_		
			$I_{OH} = -5.2 \text{ mA}$	6.0	5.68	5.80	_	5.63	_		
		V <sub>IN</sub> = V <sub>IH</sub> or		2.0	_	0.0	0.1	_	0.1		
Low-level output			I <sub>OL</sub> = 20 μA	4.5	_	0.0	0.1	_	0.1		
voltage	$V_{OL}$			6.0	_	0.0	0.1	_	0.1	V	
(Q, Q)		V <sub>IL</sub>	I <sub>OL</sub> = 4 mA	4.5	_	0.17	0.26	_	0.33		
			I <sub>OL</sub> = 5.2 mA	6.0		0.18	0.26	_	0.33		
Input leakage current	I <sub>IN</sub>	$V_{IN} = V_C$	C or GND	6.0	_	_	±0.1	_	±1.0	μА	
Rx/Cx terminal off-state current	I <sub>IN</sub>	$V_{IN} = V_C$	V <sub>IN</sub> = V <sub>CC</sub> or GND		_	_	±0.1	_	±1.0	μА	
Quiescent supply current	Icc	V <sub>IN</sub> = V <sub>CC</sub> or GND		6.0	_	_	4.0	_	40.0	μА	
Active-state supply	Icc	V V	a or CND	2.0	_	45	200	_	260	μА	
current			C or GND	4.5	_	400	500	_	650	μΑ	
(Note)		$Rx/Cx = 0.5 V_{CC}$		6.0	_	0.7	1.0	_	1.3	mA	

Note: Per circuit

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## Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 ~85°C	Unit	
			V <sub>CC</sub> (V)	Тур.	Limit	Limit	
	to a		2.0	_	75	95	
Minimum pulse width	tw (L)	_	4.5	_	15	19	ns
	t <sub>W (H)</sub>		6.0	_	13	16	
			2.0	_	75	95	
Minimum clear pulse width	t <sub>W (L)</sub>	_	4.5	_	15	19	ns
			6.0	_	13	16	
			2.0	_	5	5	
Minimum clear removal time	t <sub>rem</sub>	_	4.5	_	5	5	ns
			6.0	_	5	5	
		$Rx = 1 k\Omega$	2.0	325		_	
			4.5	108		_	ns
Minimum retrigger time	t <sub>rr</sub>	Cx = 100 pF	6.0	78	_	_	
willimidin redigger time	٠rr	$Rx = 1 k\Omega$	2.0	5.0	_	_	
		$Cx = 1 \text{ K}\Omega$ $Cx = 0.01 \mu\text{F}$	4.5	1.4	_	_	μS
		Oλ = 0.01 μι	6.0	1.2	_	_	

## AC Characteristics ( $C_L = 15 \text{ pF}$ , $V_{CC} = 5 \text{ V}$ , $Ta = 25 ^{\circ}\text{C}$ , input: $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Output transition time	t <sub>TLH</sub>			4	8	ns
Output transition time	t <sub>THL</sub>	_	_			115
Propagation delay time	t <sub>pLH</sub>			25	36	20
$(\overline{A}, B-Q, \overline{Q})$	$t_{pHL}$	_	_	23	30	ns
Propagation delay time	t <sub>pLH</sub>			16	27	
$(\overline{CL} - Q, \overline{Q})$	t <sub>pHL</sub>	_	_	10	21	ns



AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

	0	Test Condition			Ta = 25°C		Ta = -4	1.1	
Characteristics	Symbol		V <sub>CC</sub> (V)	Min	Тур.	Max	Min	Max	Unit
	t		2.0	_	30	75	_	95	
Output transition time	t <sub>TLH</sub>	_	4.5	_	8	15	_	19	ns
	t <sub>THL</sub>		6.0		7	13	_	16	
Propagation delay	t <sub>pLH</sub>		2.0		102	210	_	265	
time 	•	_	4.5	_	29	42	_	53	ns
$(\overline{A}\;,B\text{-Q},\;\overline{Q}\;)$	$t_{pHL}$		6.0	_	22	36	_	45	
Propagation delay	<b>4</b>		2.0	_	68	160	_	200	
time	t <sub>pLH</sub>	_	4.5	_	20	32	_	40	ns
$(\overline{CL} - Q, \overline{Q})$	$t_{pHL}$		6.0	_	16	27	_	34	
	twouT	Cx = 28 pF	2.0	_	700	2000	_	2500	
		$Rx = 6 k\Omega (V_{CC} = 2 V)$	4.5	_	250	400	_	500	ns
		$Rx = 2 k\Omega (V_{CC} = 4.5 V, 6 V)$	6.0	_	210	340	_	425	
		$Cx = 0.01 \mu F$ $Rx = 10 k\Omega$	2.0	90	110	130	90	130	
Output pulse width			4.5	95	105	115	95	115	μS
			6.0	95	105	115	95	115	
		Cv. 0.1E	2.0	0.9	1.0	1.2	0.9	1.2	
		$Cx = 0.1 \mu F$ $Rx = 10 k\Omega$	4.5	0.9	1.0	1.1	0.9	1.1	ms
		KX = 10 K22	6.0	0.9	1.0	1.1	0.9	1.1	
Output pulse width error between circuits	∆tw <sub>OUT</sub>	_	_	_	±1	_	_	_	%
(in same package)									
Input capacitance	C <sub>IN</sub>			_	5	10	_	10	pF
Power dissipation	$C_{PD}$	_			162				pF
capacitance	(Note)	_			102				ρι

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

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Average operating current can be obtained by the equation:

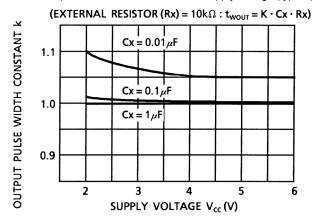
 $I_{CC}$  (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot duty/100 + I_{CC}/2$  (per circuit)

(I<sub>CC</sub>': active supply current)

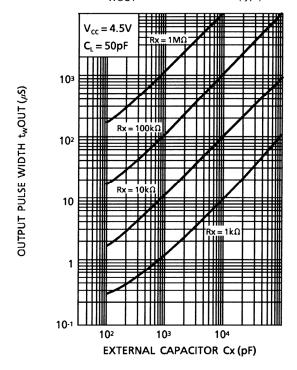
(duty: %)

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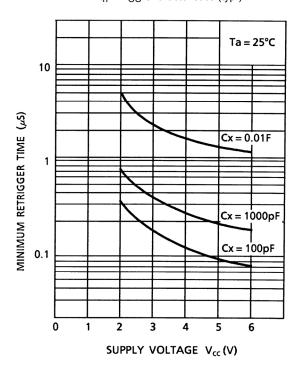
Output Pulse Width Constant K – Supply Voltage (typical)



tWOUT - Cx Characteristics (typ.)



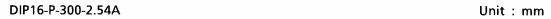
t<sub>rr</sub> – V<sub>CC</sub> Characteristics (typ.)

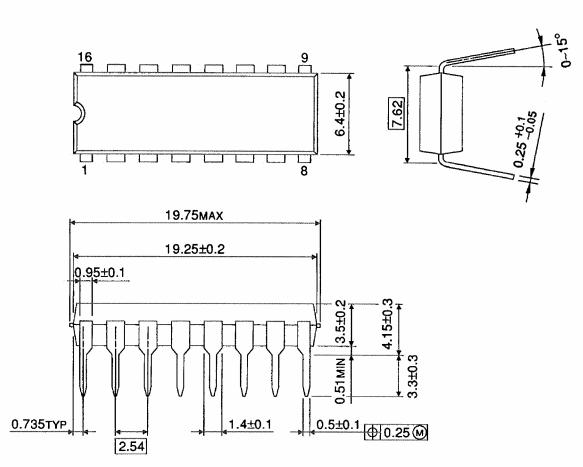


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## **Package Dimensions**

**TOSHIBA** 

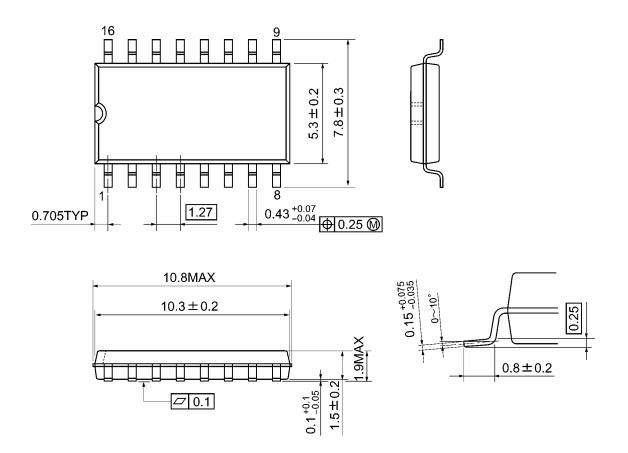




Weight: 1.00 g (typ.)

## **Package Dimensions**

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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20070701-EN GENERAL

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