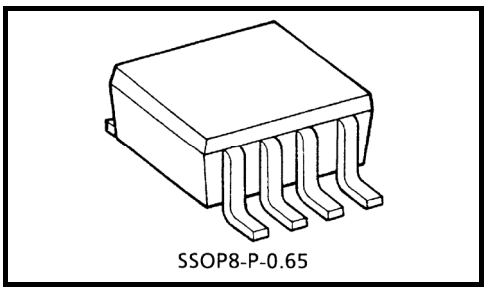
TOSHIBA CMOS Digital Integrated Circuits Silicon Monolithic

TC9WMB4FU

TC9WMB4FU: 4096-Bit (512 × 8-Bit) 2-Wire Serial EEPROM

The TC9WMB4FU is an electrically erasable/programmable nonvolatile memory (EEPROM).

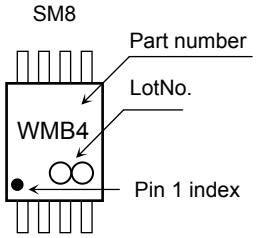


Weight: 0.02 g (typ.)

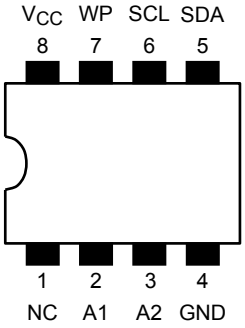
Features

- 2-wire serial interface (I^2C BUS)
- Single power supply
  Read: V_{CC} = 1.8 to 5.5 V
  Write: V_{CC} = 2.3 to 5.5 V
- Low power consumption: 5 μA (in standby state)
  0.5 mA (in read state)
- Operating frequency: 400 kHz (V_{CC} = 2.3 to 5.5 V)
- Byte write and page (16-byte) write
- Write protection
- Sequential read
- Write time: 10 ms (V_{CC} = 3.0 to 5.5 V)
  12 ms (V_{CC} = 2.3 to 2.7 V)
- Write endurance: 10^5 times
- Data retention: 10 years
- Wide operating temperature range: −40 to 85°C
- Package: SM8

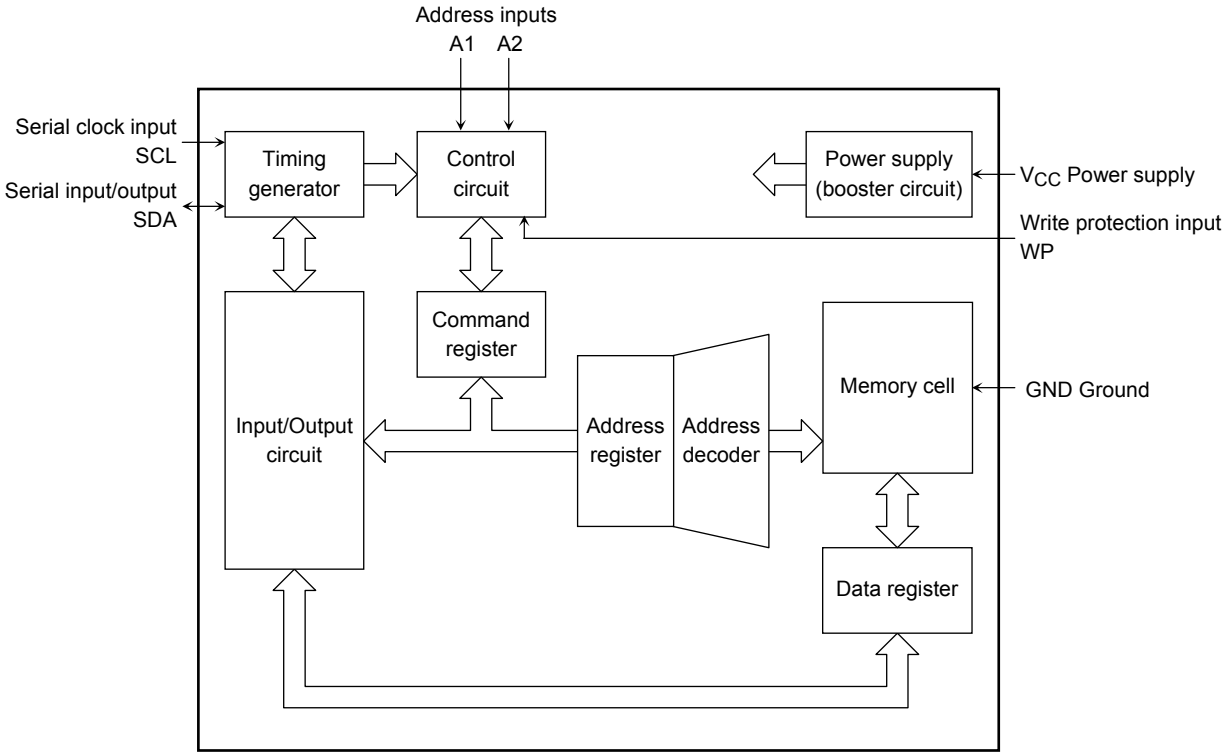
Product Marking



Pin Assignment (top view)



Block Diagram



Pin Function

Pin Name	Input/Output	Description
SCL	Input	Serial clock input Data is latched on the rising edge of SCL and transferred the falling edge of SCL.
SDA	Input/output	Serial input/output This pin must be pulled up with a resistor because it is configured as an N-ch open-drain pin for output.
WP	Input	Write protection input A high on this input disables writing. A low on this input enables writing.
A1, A2	Input	Address input This pin is used to configure the slave address.
NC	—	No connection (not connected internally)
V_{CC}	Power supply	1.8 to 5.5 V (for reading) 2.3 to 5.5 V (for writing)
GND		0 V (GND)

Functional Description

1. Start and Stop Conditions

When SCL is high, pulling SDA low produces a start condition and pulling SDA high produces a stop condition. Every instruction is started when a start condition occurs and terminated when a stop condition occurs.

During a read, a stop condition causes the read to terminate and the device to enter the standby state. During a write, a stop condition causes the fetching of write data to terminate, after which writing starts automatically. Upon the completion of writing, the device enters the standby state.

Start conditions of five times or more cannot be generated from stop condition to the next stop condition.

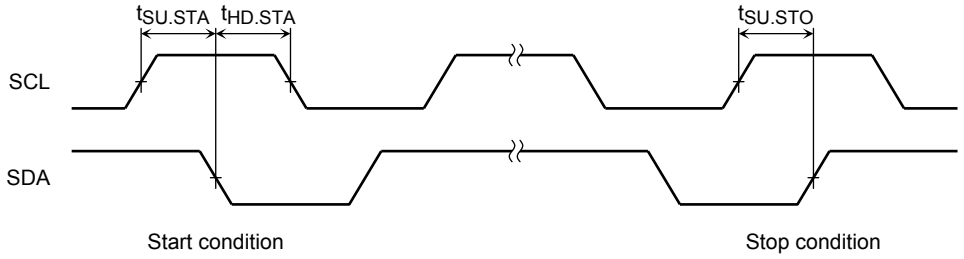


Figure 1

2. Modifying Data

Data on the SDA input can be modified while SCL is low. When SCL is high, modifying the SDA input means a start or stop condition.

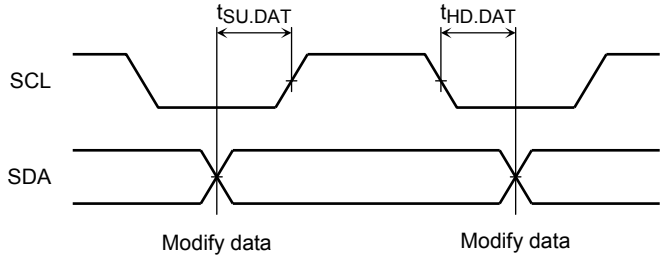


Figure 2

3. Acknowledge

Data is transmitted in 8-bit units. The device sends “low” of an acknowledge signal, by pulling SDA during the 9th clock cycle, indicating that it has received data normally. The host releases the bus in the 9th clock cycle to receive an acknowledge signal.

During a write operations, the device is always the receiver so that an acknowledge signal is sent each time it has received 8-bit of data.

During a read operations, the device sends an acknowledge signal after it receives an address following a start condition. Then, a read data is sent and releases the bus to wait for an acknowledge signal from the master. When an acknowledge signal is detected, next address data is sent if a stop condition is not detected. If the device does not detect an acknowledge signal, a read operations is stopped, and enters the standby mode when a stop condition occurs subsequently.

If the device does not detect an acknowledge signal nor a stop condition, it keeps the bus released.

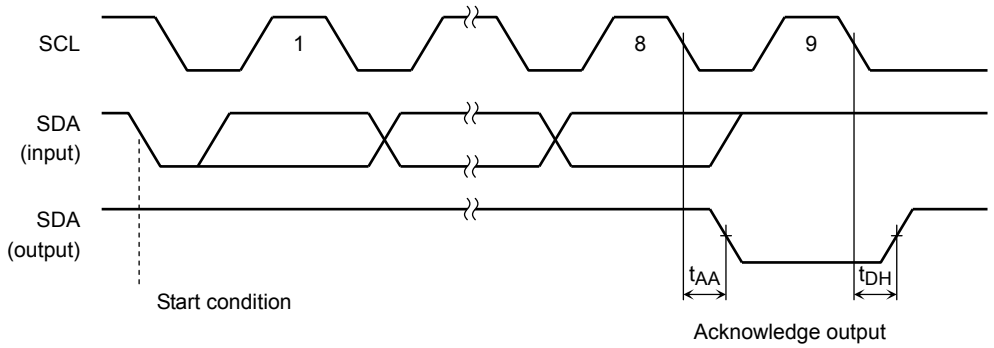


Figure 3

4. Device Addressing

After a start condition occurs, 7-bit device address and a 1-bit read/write instruction code are transferred to the device.

The first four bits are called device code, which must always be “1”, “0”, “1”,“0”. The next two bits are called slave address and are used to select a device on the bus. The slave address is compared to the value on the address inputs (A1 and A2). The next bit is called page address (P0). P0 on “0” selects the memory area of the first 2k-bit (000 to 0FF) and on “1” selects the memory area of the last 2k-bit (100 to 1FF).

The least significant bit (R/$\overline{W}$: READ/$\overline{WRITE}$) indicates a read instruction when set to “1” and a write instruction when set to “0”.

An instruction is not executed if the device address does not match the specified value.

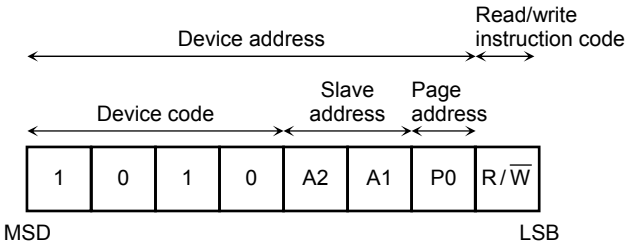


Figure 4

5. Write Operation

(1) Byte write

A data is written to the specified address at a byte write operation. After a start condition, a device address, R/$\overline{W}$ (= 0), a word address, and write data are received to the device.

When a stop condition is generated subsequently, write operation starts automatically, rewriting the data at the specified address with the input data. A next instruction cannot be received while write operation is in progress. Therefore, no acknowledge signal is returned. After writing the data, the device automatically enters the standby state.

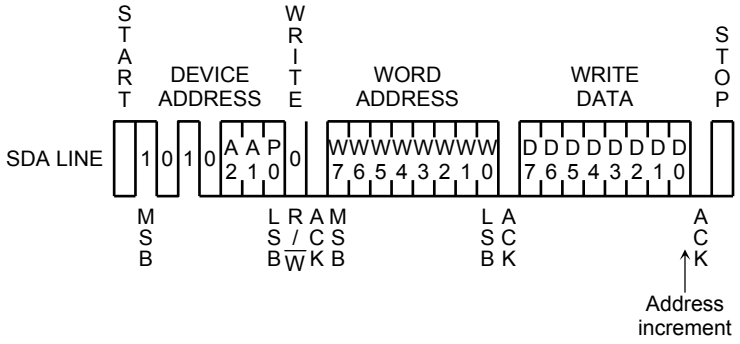


Figure 5

(2) Page write

A Data is written up to16 bytes to the specified page at a page write operation. After a start condition, a device address, R/$\overline{W}$ (= 0), a word address (n), and write data (n) are received to the device, in the same way as for a byte write operation. Then, write data (n + 1) is immediately received without entering a stop condition, while checking that an acknowledge signal is asserted (0).

The first four bits (W4 to W7) of the word address are the same and the lower four bits (W0 to W3) are automatically incremented so that up to 16 bytes of data can be written.

When the last address within the page is reached, the lower four bits (W0 to W3) of the word address are rolled over to the first address of the page. If more than 16 bytes of write data are transferred, the last 16 bytes are valid.

When a stop condition is generated subsequently, write operation starts automatically, rewriting the data at the specified addresses with the input data.

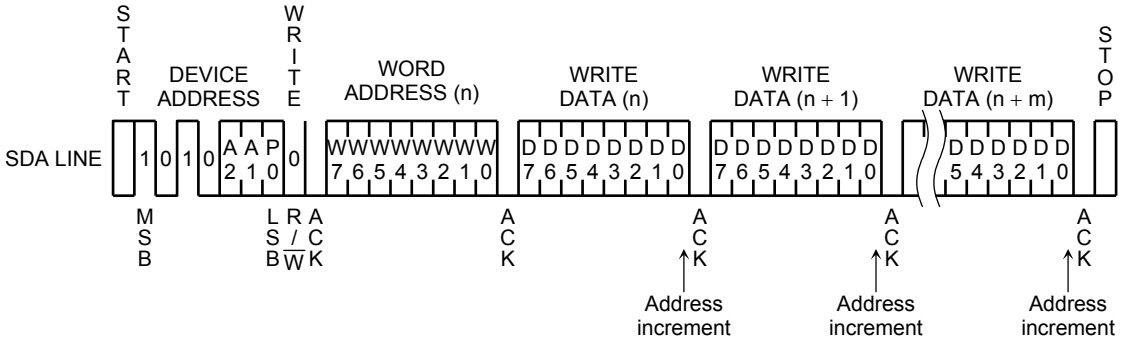


Figure 6

(3) Acknowledge polling

Acknowledge polling is a feature for determining whether rewrite operation is in progress. During rewrite operation, generate a start condition followed by a device address, and R/$\overline{W}$ (= 0 or 1). The acknowledge feature does not generate an acknowledge signal while rewrite operation is in progress. A low acknowledge signal is generated if rewriting has already completed.

If the next instruction is a write, supply a word address and write data subsequently. If the next instruction is a read, supply a stop condition and then start read operation.

(4) Write protection

When "high" is received to the write protection (WP) pin, the device caused to protect the bottom half (100h to 1FFh) of the memory area from being written. Rewriting is allowed when "low" is received to the write protection pin. While a write is in progress, driving the WP pin high does not stop write operation.

Reading is always enabled regardless of whether the WP pin is high or low.

6. Read Operation

Read operation is performed in one of three modes: current address read, random read, and sequential read.

For reading, a device receives a device address and R/$\overline{W}$ (= 1) after a start condition. After read data is sent, terminate a read operation by generating a high acknowledge signal (or releasing the bus without supplying an acknowledge signal) and then supplying a stop condition.

(1) Current address read

The internal address counter maintains the address that is next to the last accessed (read or written) word address (n). In current address read mode, data is read from address n + 1, as indicated by the address counter.

In current address read mode, supplying a device address and R/$\overline{W}$ (= 1) after a start condition, causes the device to generate a low acknowledge signal and send a data at the address indicated by the internal address counter. In this case, the page address bit (P0) is ignored and a data is read at the current address indicated by the internal address counter.

The address counter is incremented on the falling edge of the SCL pulse where a data at the eighth bit is sent. If the previous operation was reading data from the last address, the current address is rolled over to address 0. If the previous operation was writing data to the last address of the page, the address is rolled over to the first address of the page.

The current address is maintained in an internal register so that it is lost when the power is turned off. For the first read after power-up, specify an address by performing a random read.

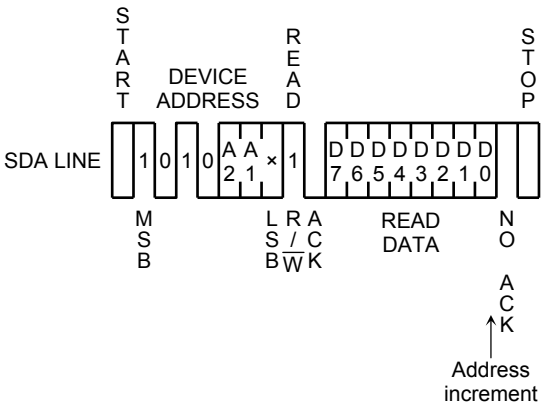


Figure 7

(2) Random read

A random read reads data at a specified address. A dummy write is necessary to specify an address.

In random read mode, supply a device address, R/$\overline{W}$ (= 0), and a word address after a start condition. Unlike a byte or page write, where write data is supplied immediately, a dummy write only specifies a word address. Then, supply a start condition and transfer a device address and R/$\overline{W}$ (= 1) in the same way as for a current address read, to read data from the specified address.

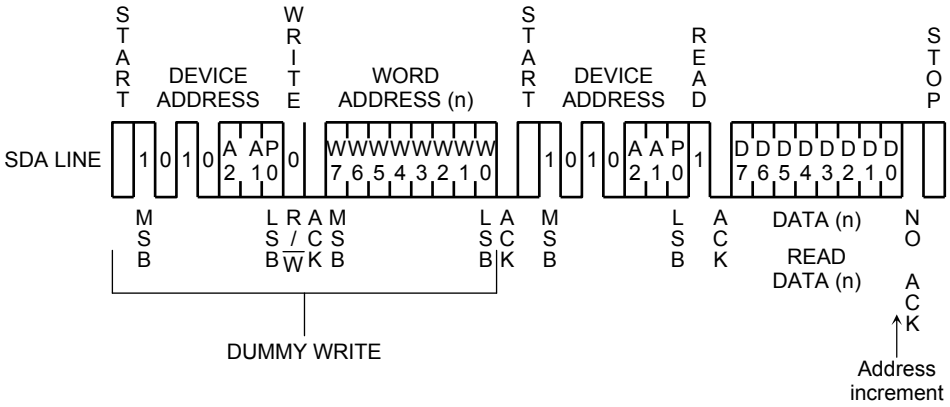


Figure 8

(3) Sequential read

A sequential read reads data sequentially from successive word addresses.

For either current address read or random read, upon receiving a start condition, a device address and R/W (= 1), an acknowledge (low) is placed on the SDA line, followed by the data at the address pointed to by the internal address counter. When an acknowledge (low) is then received, the word address is automatically incremented so that the next data is driven out.

After the last address is reached, the word address is rolled over to address 0.

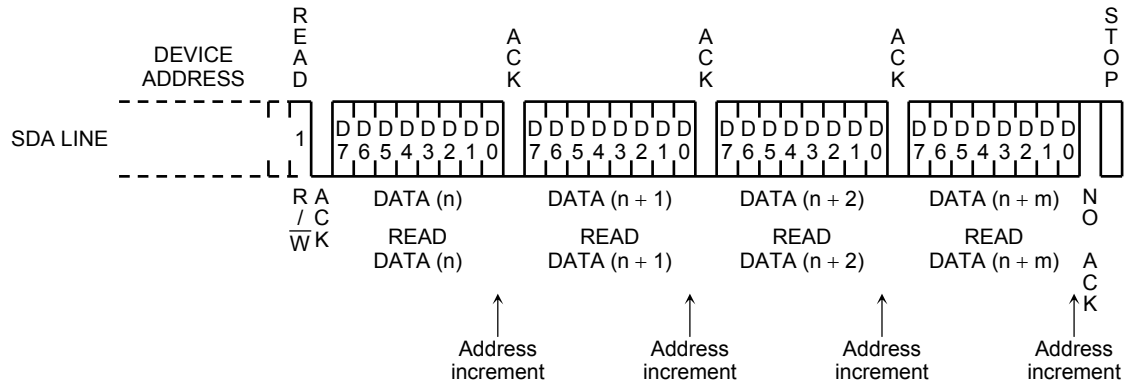


Figure 9

7. Notes on Use

(1) Powering up the device

This device contains a power-on clear circuit, which initializes the internal circuit of the device when the power is turned on. After initialization, the address counter returns to the first address 00H and the SDA pin goes to the high-impedance state (standby state). If initialization fails, the device may malfunction. When powering up the device, observe the following precautions to assure that the clear circuit will operate normally:

(a) Pull SCL and SDA high.
(b) The power rising time (t_R) must be 10 ms or less.
(c) After turning off the power, wait at least 100 ms (t_{OFF}) before attempting to power up the device again.
(d) The supply voltage must rise from a voltage lower than 0.1 V.
(e) After turning on the power, wait at least 10 ms before attempting to send an instruction to the device.

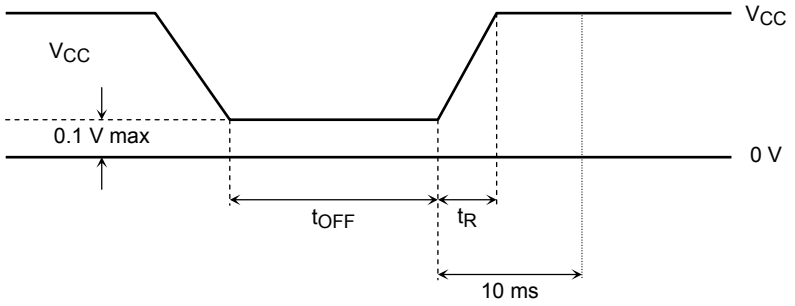


Figure 10

(2) Pulling up the SDA and SCL pins

The device requires the SDA and SCL pins to be pulled up with an external resistor. The recommended pull-up resistance range is 1 kΩ to 10 kΩ.

(3) Noise elimination time for the SDA and SCL pins

The device contains a low-pass filter for eliminating noise on the SDA and SCL pins. Its guaranteed value corresponds to the noise suppression time Ti, given in the AC characteristics table.

(4) Write operation

(a) The address counter is incremented when a write instruction is received successfully. It is incremented on the falling edge of the SCL pulse where the least significant bit of data is received.

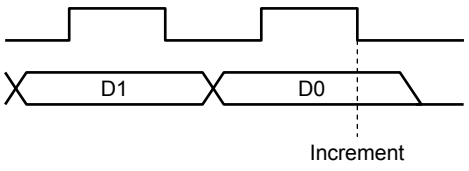
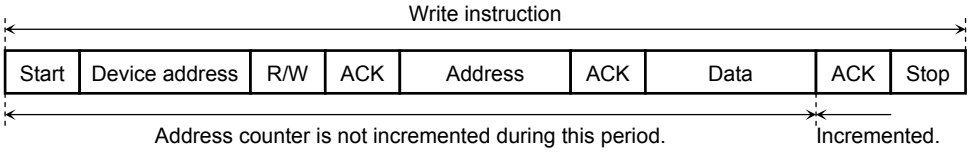
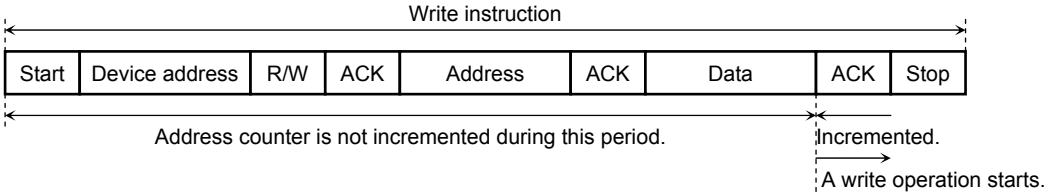


Figure 11 Increment Timing Diagram

(b) If a start condition is issued while the device is receiving a write instruction (device address, R/W, address, and data), this write instruction is discarded and the next instruction is accepted. (A byte write is given below as an example. This is the same as a page write.)



(c) If a stop condition is issued while the device is receiving a write instruction (device address, R/W, address, and data), the device enters the standby state. However, the device ignores the stop condition while sending an acknowledge signal after it receives the D0 bit. (A write operation starts.)
(A byte write is given below as an example. This is the same as a page write.)



(d) No instruction is accepted while a write operation is in progress (after a stop condition for a write instruction is received).
(The device does not receive a start or stop condition during this time.)

(5) Read operation

(a) The address counter is incremented when a read instruction is received successfully. It is incremented on the falling edge of the SCL pulse where the least significant bit of data is driven.

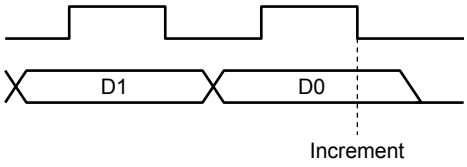
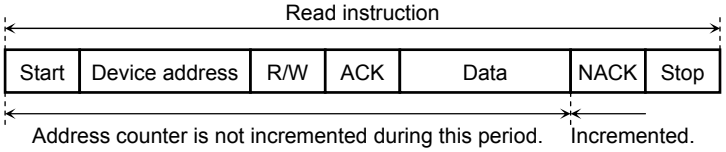
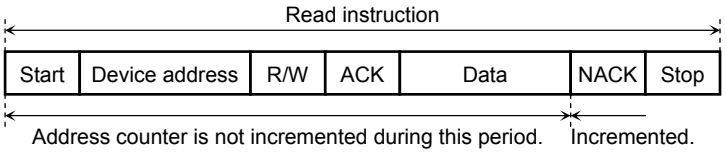


Figure 12 Increment Timing Diagram

(b) If a start condition is issued while the device is receiving a read instruction (device address, R/W, address, or data), this read instruction is discarded and the next instruction is accepted. (A start condition is accepted even during data transfer.)
(A current address read is given below as an example. This is the same as the other read modes.)



(c) If a stop condition is issued while data is read (device address, R/W, address, and data), the device enters the standby state.
(A stop condition is accepted even during data transfer.)
(A current address read is given below as an example. This is the same as the other read modes.)



(d) If a start condition is issued while data is read, the SDA pin changes from output to input mode and the device is ready to accept the next instruction.

(6) Software reset

The device cannot be reset externally because it does not incorporate a RESET pin. Instead, the device is reset by software. The software resets the device to the same state using the power-on clear circuit. The address counter returns to the first address 00H and the SDA pin goes to the high-impedance state (standby state).

The software reset is invoked when a start condition is generated followed by nine SCL clock pulses (dummy cycles). While a dummy cycle is inserted, the SDA line must be pulled high. This reset operation stops an acknowledge output and data transfer. The reset is completed by generating another start condition. Issue a stop condition before starting a new transfer.

Start conditions of five times or more cannot be generated from stop condition to the next stop condition.

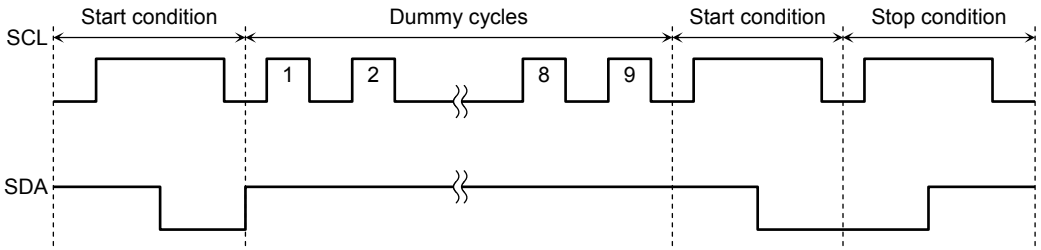


Figure 13 Software reset

Absolute Maximum Ratings (Note) (GND = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to 7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Power dissipation	P_D	300 (25°C)	mW
Storage temperature	T_{stg}	−55 to 125	°C
Operating temperature	T_{opr}	−40 to 85	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note) (GND = 0 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Max	Unit
Supply voltage (for reading)	V_{CC}	—	1.8	5.5	V
Supply voltage (for writing)	V_{CC}	—	2.3	5.5	V
High-level input voltage	V_{IH}	2.3 V ≤ V_{CC} ≤ 5.5 V	0.7 × V_{CC}	V_{CC}	V
		1.8 V ≤ V_{CC} < 2.3 V	0.8 × V_{CC}	V_{CC}	
Low-level input voltage	V_{IL}	2.3 V ≤ V_{CC} ≤ 5.5 V	0	0.3 × V_{CC}	V
		1.8 V ≤ V_{CC} < 2.3 V	0	0.2 × V_{CC}	
Operating frequency	f_{SCL}	2.3 V ≤ V_{CC} ≤ 5.5 V	0	400	kHz
		1.8 V ≤ V_{CC} < 2.3 V	0	100	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics (GND = 0 V, T_{opr} = −40 to 85°C)

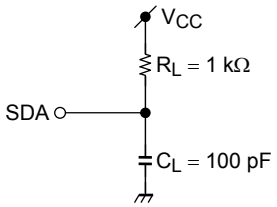
Characteristics	Symbol	Test Condition	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} ≤ 3.6 V		4.5 ≤ V_{CC} ≤ 5.5 V		Unit
			Min	Max	Min	Max	Min	Max	
Input current	I_{LI}	—	—	±1	—	±1	—	±1	μA
Output leakage current	I_{LO}	—	—	±1	—	±1	—	±1	μA
Low-level output voltage	V_{OL}	I_{OL} = 3.2 mA	—	—	—	0.4	—	0.4	V
		I_{OL} = 1.5 mA	—	0.5	—	—	—	—	
Quiescent supply current	I_{CC1}	—	—	5	—	5	—	5	μA
Supply current during read	I_{CC2}	f = 400 kHz	—	0.2*	—	0.3	—	0.5	mA
Supply current during write	I_{CC3}	f = 400 kHz	—	—	—	1.5	—	2.5	mA

*: f = 100 kHz

AC Characteristics (GND = 0 V, T_{opr} = −40 to 85°C)

Test Conditions

Input rise/fall time	20 ns
Input/output testing voltage	0.5 × V_{CC}
Output load	100 pF + 1 kΩ pull-up resistor



Characteristics	Symbol	1.8 ≤ V_{CC} < 2.3 V		2.3 ≤ V_{CC} ≤ 3.6 V		4.5 ≤ V_{CC} ≤ 5.5 V		Unit
		Min	Max	Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	0	400	kHz
SCL clock low time	t_{LOW}	4.7	—	1.2	—	1.2	—	μs
SCL clock high time	t_{HIGH}	4.0	—	0.6	—	0.6	—	μs
Noise suppression time	t_I	—	100	—	50	—	50	ns
SDA output delay	t_{AA}	0.1	4.5	0.1	0.9	0.1	0.9	μs
Bus free time	t_{BUF}	4.7	—	1.2	—	1.2	—	μs
Start condition hold time	$t_{HD.STA}$	4.0	—	0.6	—	0.6	—	μs
Start condition setup time	$t_{SU.STA}$	4.7	—	0.6	—	0.6	—	μs
Data input hold time	$t_{HD.DAT}$	0	—	0	—	0	—	ns
Data input setup time	$t_{SU.DAT}$	250	—	200	—	200	—	ns
SCL, SDA input rise time	t_R	—	1.0	—	0.3	—	0.3	μs
SCL, SDA input fall time	t_F	—	0.3	—	0.3	—	0.3	μs
Stop condition setup time	$t_{SU.STO}$	4.7	—	0.6	—	0.6	—	μs
SDA output hold time	t_{DH}	100	—	50	—	50	—	ns

EEPROM Characteristics (GND = 0 V, 2.3 V ≤ V_{CC} ≤ 2.7 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Write time	t_{WR}	—	—	—	12	ms
Rewrite endurance	N_{EW}	—	1×10^5	—	—	Times
Data retention time	t_{RET}	—	10	—	—	Years

EEPROM Characteristics (GND = 0 V, 2.7 V < V_{CC} ≤ 5.5 V, T_{opr} = −40 to 85°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Write time	t_{WR}	—	—	—	10	ms
Rewrite endurance	N_{EW}	—	1×10^5	—	—	Times
Data retention time	t_{RET}	—	10	—	—	Years

Capacitance Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		Typ.	Unit
			V_{CC} (V)		
Input capacitance	C_{IN}	—	5	4	pF
Output capacitance	C_O	—	5	3	pF

AC Characteristics Timing Charts

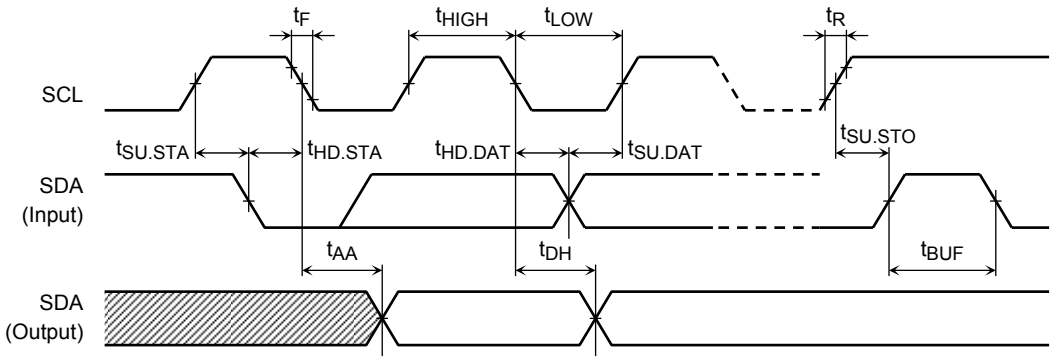


Figure 14 Bus Timing

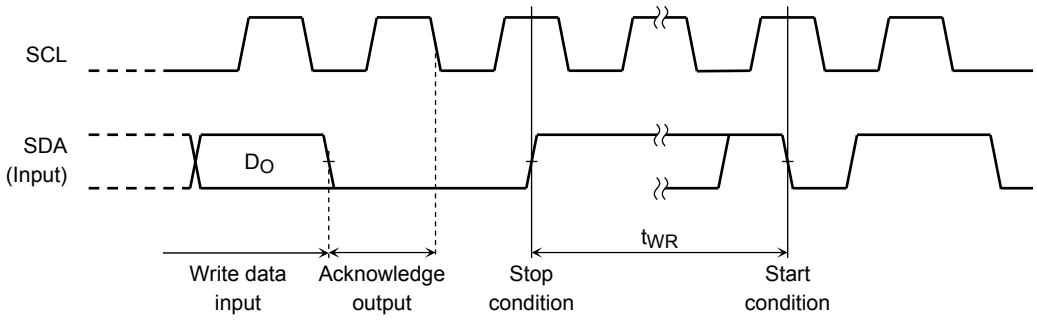
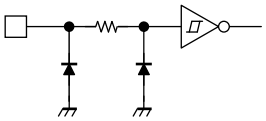
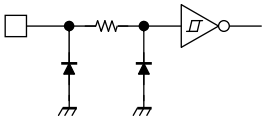
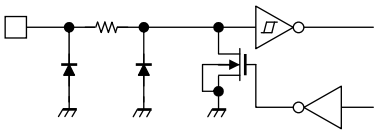


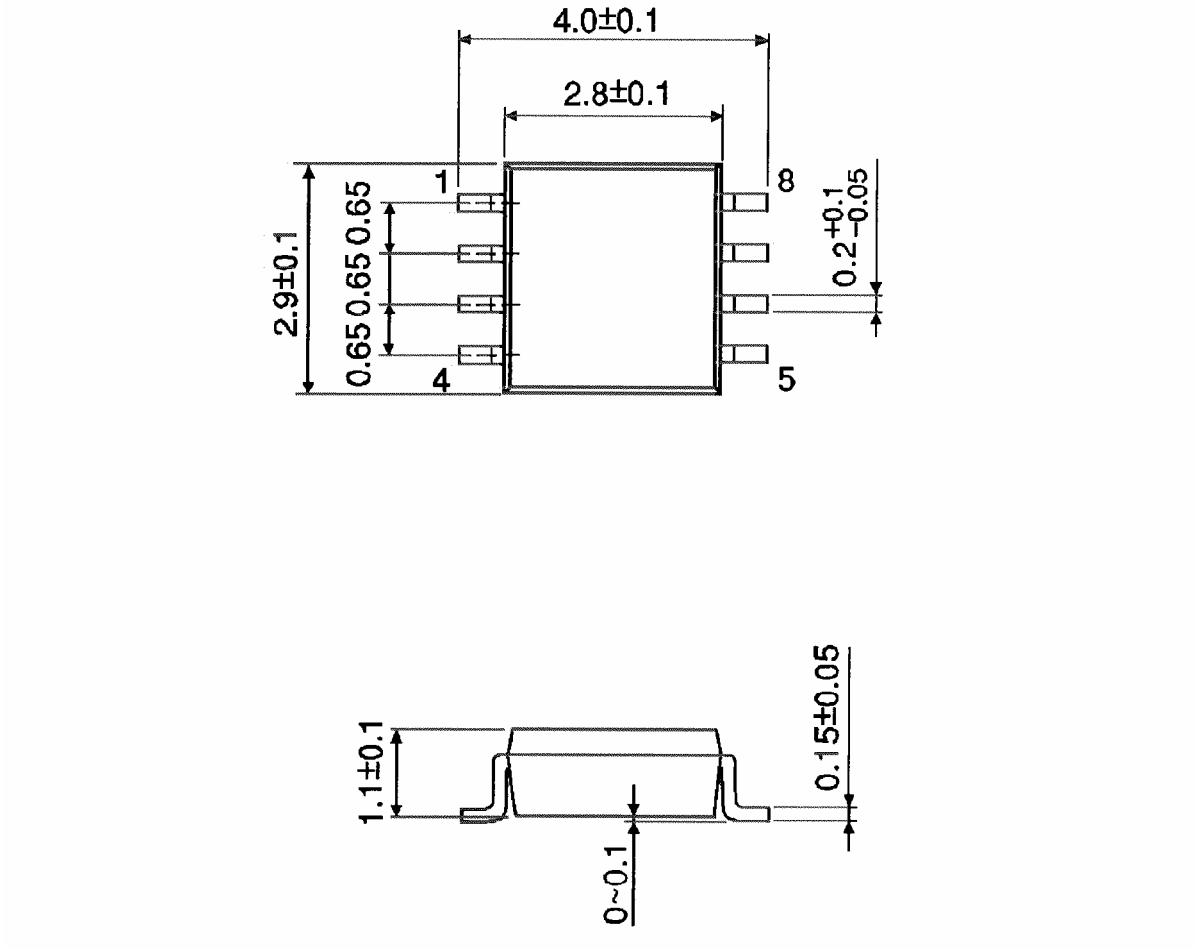
Figure 15 Write Cycle Timing

Input/Output Circuits of Pins

Pin	Type	Input/Output Circuit	Remarks
WP A1/A2	Input		—
SCL	Input		—
SDA	Input/output		Open-drain output

Package Dimensions

SSOP8-P-0.65 Unit : mm



Weight: 0.02 g (typ.)

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

- The information contained herein is subject to change without notice.
- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc.
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.).These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in his document shall be made at the customer’s own risk.
- The products described in this document shall not be used or embedded to any downstream products of which manufacture, use and/or sale are prohibited under any applicable laws and regulations.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patents or other rights of TOSHIBA or the third parties.
- Please contact your sales representative for product-by-product details in this document regarding RoHS compatibility. Please use these products in this document in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances. Toshiba assumes no liability for damage or losses occurring as a result of noncompliance with applicable laws and regulations.