OVERVIEW

The CF5707CG is a 32.768kHz reference frequency crystal oscillator CMOS LSI for stepping motor drives in low-current consumption analog watches.

FEATURES

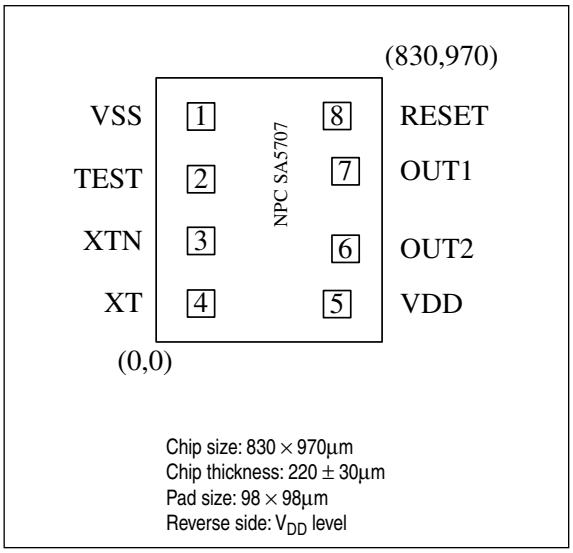
- 32.768kHz crystal oscillator circuit
  - C_G = 5pF, C_D = 17pF built-in
- −1.2 to −2.0V operating supply voltage range
- 150nA (typ) to 250nA (max) operating current consumption
- Reset function
  - Reset in 4Hz frequency steps

ORDERING INFORMATION

Device	Package
CF5707CG	Chip form

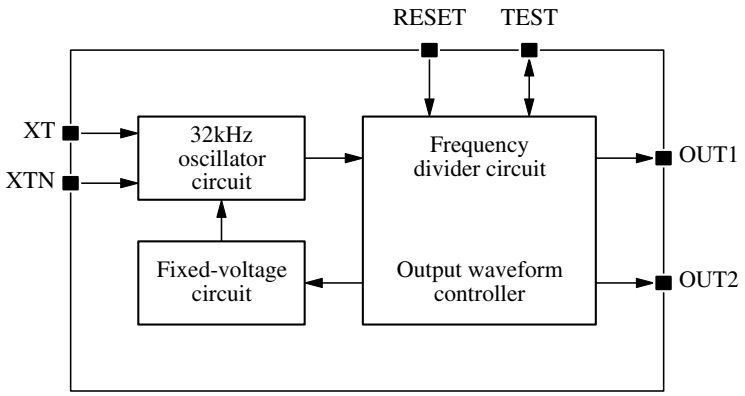
PAD LAYOUT

(Top view)



Chip size: 830 × 970µm
Chip thickness: 220 ± 30µm
Pad size: 98 × 98µm
Reverse side: V_{DD} level

BLOCK DIAGRAM



PAD DESCRIPTION/DIMENSIONS

Number	Name	Description	Dimensions [μm]	
			X	Y
1	VSS	Negative supply voltage	165	828
2	TEST	Test mode switch control. 512Hz clock output during normal operation	165	598
3	XTN	Crystal oscillator circuit output	165	371
4	XT	Crystal oscillator circuit input	165	141
5	VDD	Positive supply voltage	665	139
6	OUT2	Stepping motor driver output 2	696	342
7	OUT1	Stepping motor driver output 1	696	627
8	RESET	Reset input	665	830

SPECIFICATIONS

Absolute Maximum Ratings

V_{DD} = 0V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	–5.0 to 0.3	V
Input voltage range	V_{IN}	V_{SS} – 0.3 to 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage	V_{SS}	–2.0 to –1.2	V
Operating temperature	T_{opr}	–20 to 75	°C

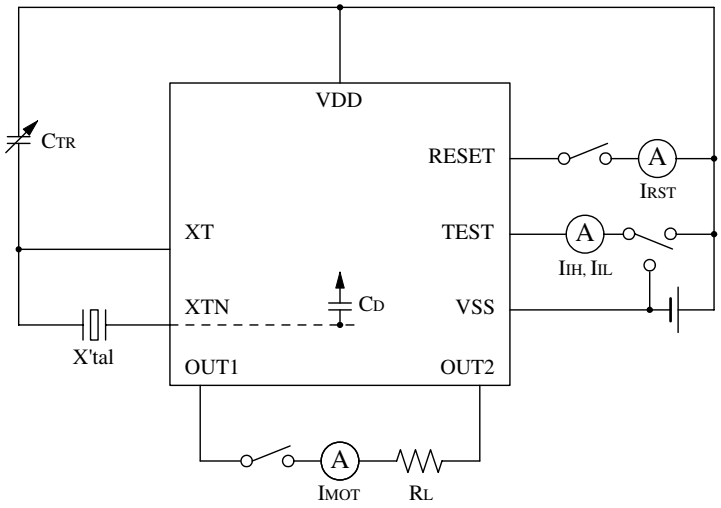
Electrical Characteristics

V_{DD} = 0V, V_{SS} = –1.55V, Ta = 25°C, (C_{TR} + C_G) = 16pF, C_D = 17pF (including parasitic capacitance), X'tal C_L = 8pF, C_I = 55kΩ max

Parameter		Symbol	Condition	Rating			Unit
				min	typ	max	
Operating supply voltage[1]		V_{SS}		–2.0	–1.55	–1.2	V
Operating current consumption		I_{DD}	No load	–	0.15	0.25	µA
Reset input current[2]		I_{RST}	V_{RST} = V_{DD}	–	6	–	nA
Reset input resistance		R_{RST}	V_{RST} = –1.35V	15	35	60	kΩ
Test input current[3]		I_{IH}	V_{IH} = 0V	–	1	3	µA
		I_{IL}	V_{IL} = –1.55V	–	1	3	µA
Motor output current[1]		I_{MOT}	R_L = 2kΩ, V_{SS} = –1.55V	± 0.7	–	–	mA
Movement period	Normal mode	T_{CY}		–	2	–	sec
	Test mode	t_{CY}		–	62.5	–	msec
Motor pulsewidth		T_{PW}		–	3.9	–	msec
Oscillator startup voltage		V_{STA}		–1.3	–	–	V
Oscillator startup time[4]		T_{STA}		–	2	5	sec
Frequency voltage deviation		Δf/f	V_{SS} = –1.2 to –2.0V, C_{TR} = 5pF	–	0.2	1	ppm/0.1V
Frequency deviation[5]		ε'		–8	–	8	ppm
Internal capacitance[6]		C_G	(C_G + C_D) < 62pF, C_G, C_D min 5pF	–	5	–	pF
		C_D		–	17	–	pF

1. Parameters measured using the following measurement circuits.
2. The current flowing from the V_{DD} pin into the RESET pin.
3. I_{IH}, I_{IL} are the input current values with clock stopped when TEST is H, L, respectively.
4. The time interval from when power is applied until the 512Hz output on the TEST pin.
5. ε' = [f (1.55V) – f'$_0$] / f'$_0$
   where f'$_0$ is the oscillator center frequency under the same measurement conditions.
6. C_G is measured between V_{DD} – XT, and C_D is measured between V_{DD} – XTN. Measurement conditions: f = 40kHz, 50mVp-p

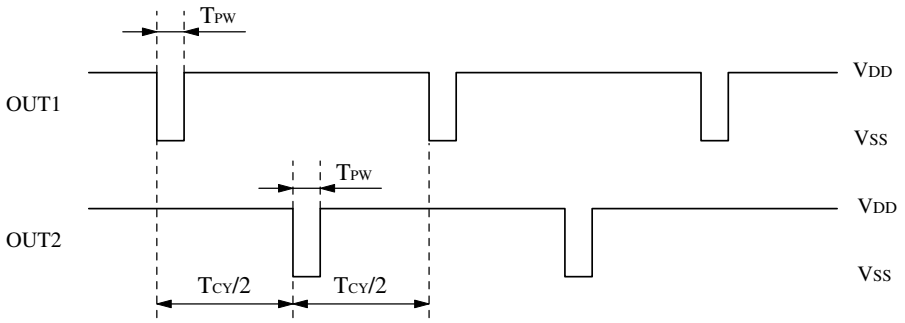
Measurement Circuit



X' tal parameters: f = 32.768kHz, CI = 20kΩ, C0 = 1.3pF, C1 = 2.6fF

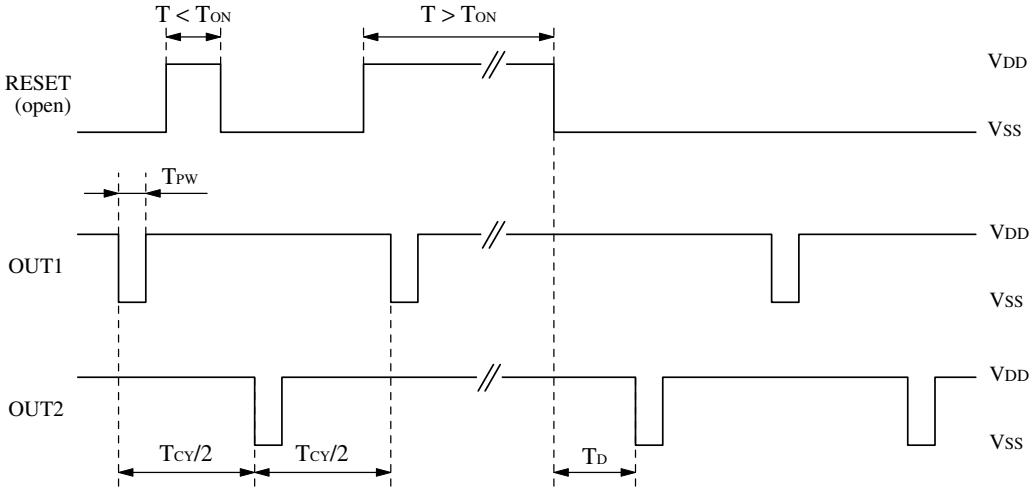
FUNCTIONAL DESCRIPTION

Motor Output Waveform



Watch movement period Tcy = 2s, Pulsewidth Tpw = 3.9ms

Reset Function



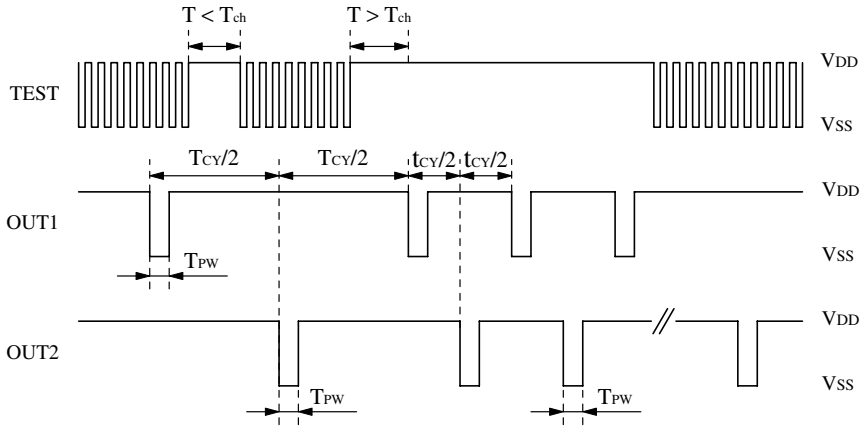
Reset operation

The device reset condition occurs when the RESET pin goes HIGH (V_{DD}), and the circuits are reset in 4Hz frequency divider steps. Note, however, that RESET must stay HIGH for 93.7ms or longer, otherwise the reset input is ignored.

Reset release operation

If the last pulse before reset was output on OUT1, then the first pulse after reset is released is output on OUT2, and vice versa. The time interval, T_D, after reset is released until the first pulse output occurs is $T_{CY}/2 - 0.125$s to $T_{CY}/2$.

Test Function



Test mode 1

Normal mode (TEST = open)

A 512Hz rectangular waveform is output on the TEST pin. Note that the load resistance is 10MΩ or greater and capacitance is 20pF or less. Normal watch movement waveforms are output on OUT1 and OUT2.

Test mode 1 (TEST = V_{DD})

The device switches to test mode 1 when the TEST pin goes HIGH (V_{DD}). Note, however, that the TEST must stay HIGH for 2 cycles of the 512Hz clock (T_{CH} > 3.9ms), otherwise the input is ignored. In test mode 1, high-speed watch movement period (T_{CY} = 62.5ms) is selected.

Test mode 2 (TEST = V_{SS})

(Note. IC test mode only)

The device switches to test mode 2 when the TEST pin goes LOW (V_{SS}). In test mode 2, operation occurs at 32-times speed. Furthermore, if an input on RESET occurs, all internal registers are cleared and circuit operation stops. Once in this condition, the circuit remains stopped until the TEST pin becomes open circuit or HIGH level (V_{DD}).

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