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### Description

The CXG1194XR is a high power SP4T antenna switch for GSM/UMTS applications. The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level. On chip logic reduces component count and simplifies the PCB layout by allowing direct connection of the switch to digital baseband control lines with CMOS logic levels. This switch is SP4T, one antenna can be routed to either of the 2Tx or 2Rx ports. It requires 2 CMOS control lines. The Sony GaAs JPHEMT MMIC process is used for low insertion loss.

(Applications: GSM dual-band handsets, GSM/UMTS dual-mode handsets)

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### Features

- ◆ Insertion loss (Tx) : 0.35dB (Typ.) at 34dBm (GSM900)  
0.45dB (Typ.) at 32dBm (GSM1800)

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### Package

Small and Low height package size: 14-pin XQFN (2.5mm × 2.5mm × 0.35mm (Typ.))

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### Structure

GaAs JPHEMT MMIC

This IC is ESD sensitive device. Special handling precautions are required.  
The actual ESD test data will be available later.

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**Absolute Maximum Ratings**

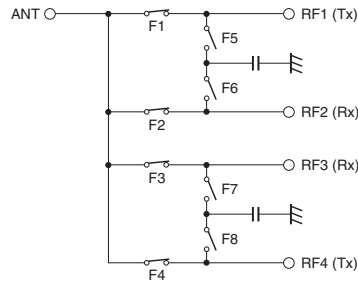
(Ta = 25°C)

◆ Bias Voltage	V <sub>DD</sub>	7	V
◆ Control Voltage	V <sub>ctl</sub>	5	V
◆ Input power max. [ANT, RF1, RF4]		35	dBm (Duty cycle = 12.5 to 50%)
◆ Input power max. [RF2, RF3]		13	dBm
◆ Operating temperature	T <sub>opr</sub>	-35 to +85	°C
◆ Maximum power dissipation	PD	500	mW

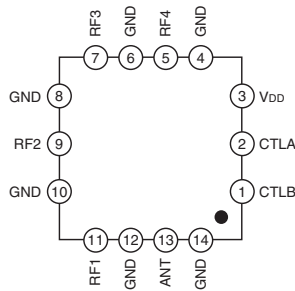
• Copper-clad lamination of glass board (4 layers) : 30mm square, t = 0.8mm, FR-4.

Note) Use this product without exceeding the PD value specified in this specification.  
 If it is used with exceeding the PD value even for a moment, the heat generated by the operation may cause the degradation or breakdown of the product.

**Block Diagram**



**Pin Configuration**



**Truth Table**

ON Path	CTLA	CTLB	F1	F2	F3	F4	F5	F6	F7	F8
ANT – RF1	L	L	ON	OFF	OFF	OFF	OFF	ON	ON	ON
ANT – RF2	H	L	OFF	ON	OFF	OFF	ON	OFF	ON	ON
ANT – RF3	L	H	OFF	OFF	ON	OFF	ON	ON	OFF	ON
ANT – RF4	H	H	OFF	OFF	OFF	ON	ON	ON	ON	OFF

## Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	ANT – RF1	824 to 960MHz		0.35	0.50	dB
			1710 to 1990MHz		0.45	0.65	dB
		ANT – RF2	824 to 960MHz		0.45	0.60	dB
			1710 to 1990MHz		0.55	0.70	dB
		ANT – RF3	824 to 960MHz		0.45	0.60	dB
			1710 to 1990MHz		0.55	0.70	dB
ANT – RF4	824 to 960MHz		0.35	0.50	dB		
	1710 to 1990MHz		0.45	0.65	dB		
Isolation	ISO.	ANT – RF1	824 to 960MHz	25	30		dB
			1710 to 1990MHz	22	26		dB
		ANT – RF2	824 to 960MHz	30	35		dB
			1710 to 1990MHz	25	30		dB
		ANT – RF3	824 to 960MHz	30	35		dB
			1710 to 1990MHz	25	30		dB
ANT – RF4	824 to 960MHz	30	35		dB		
	1710 to 1990MHz	25	30		dB		
VSWR	VSWR		824 to 960MHz		1.2		—
			1710 to 1990MHz		1.2		—
Harmonics*1	2fo	ANT – RF1	*2		-33	-28	dBm
	3fo				-34	-28	dBm
	2fo		*3		-35	-30	dBm
	3fo				-37	-33	dBm
	2fo	ANT – RF4	*2		-34	-30	dBm
	3fo				-35	-30	dBm
	2fo		*3		-35	-30	dBm
	3fo				-38	-34	dBm
P <sub>1dB</sub> compression input power	P <sub>1dB</sub>	ANT – RF1, 4	*2	35			dBm
		ANT – RF1, 4	*3	33			dBm
Control current	I <sub>ctl</sub>		V <sub>ctl</sub> = 2.8V		15	40	μA
Supply current	I <sub>DD</sub>		V <sub>DD</sub> = 2.8V		0.12	0.23	mA

Note) Electrical Characteristics are measured with all RF ports terminated in 50Ω.

\*1 Harmonics measured with Tx inputs harmonically matched. The use of harmonic matching is recommended to ensure optimum performance.

\*2 Power incident on Tx, Pin = 34dBm, 824 to 915MHz, V<sub>DD</sub> = 2.8V, RF1 or RF4 enabled

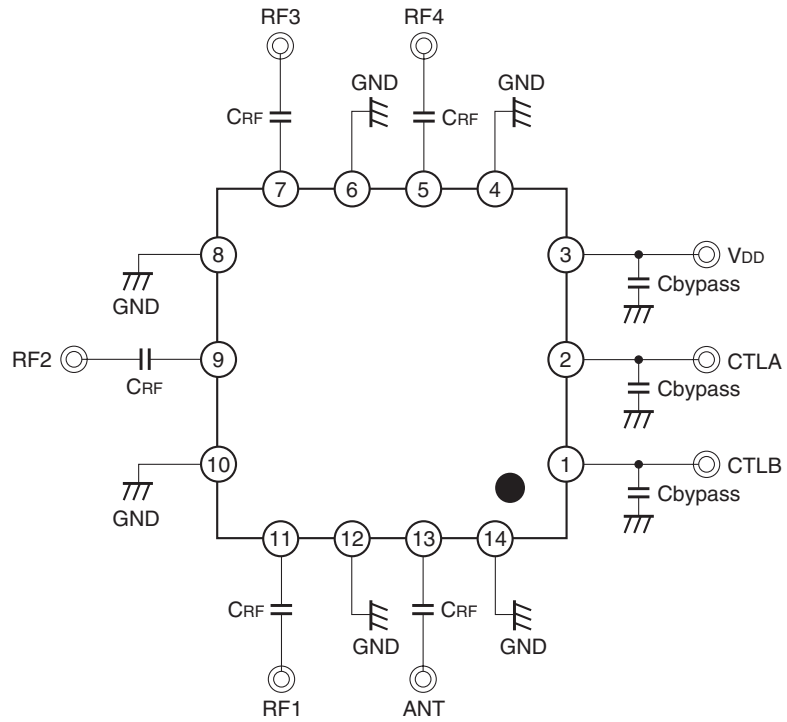
\*3 Power incident on Tx, Pin = 32dBm, 1710 to 1910MHz, V<sub>DD</sub> = 2.8V, RF1 or RF4 enabled

**DC Bias Condition**

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	2.8	3.6	V
Vctl (L)	0	—	0.4	V
VDD	2.6	2.8	3.6	V

**Recommended Circuit**

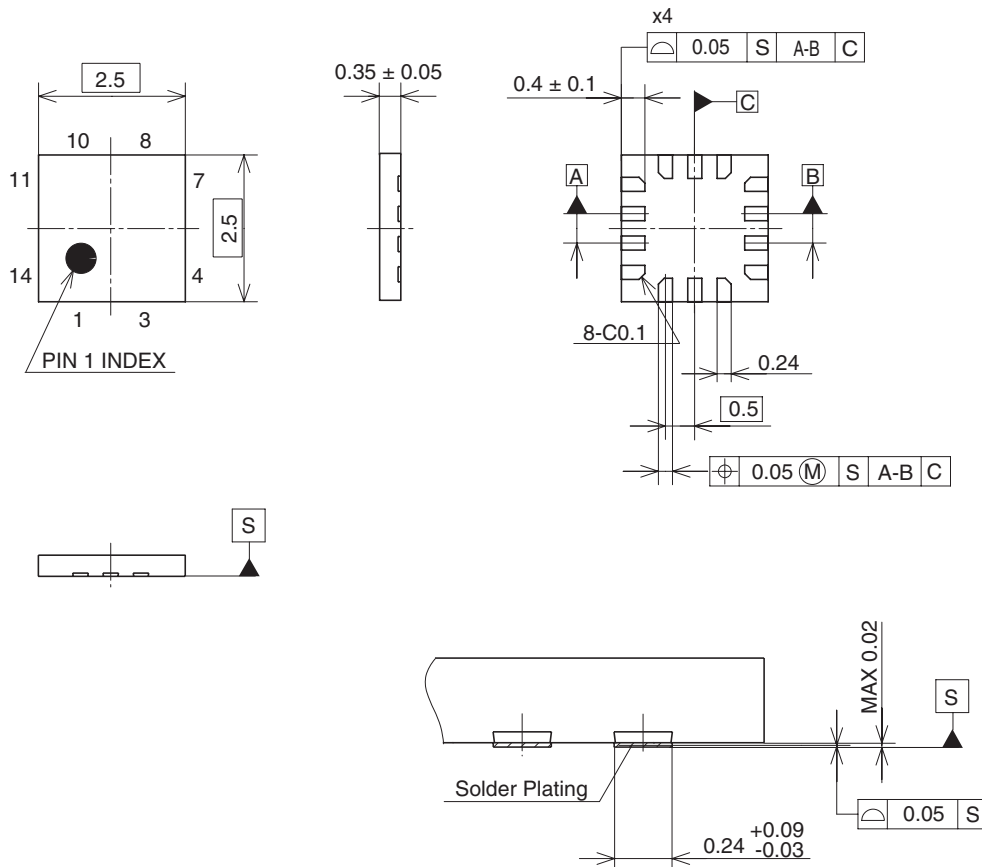


When using this IC, the following external components should be used:  
 CRF: This capacitor is used for RF decoupling and must be used for all applications.  
 Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Package Outline

(Unit: mm)

14PIN XQFN (PLASTIC)



TERMINAL SECTION

Note: Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-14P-01
EIAJ CODE	—
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm