DF6811CPU

8-bit FAST Microcontrollers Family

ver 2.17

OVERVIEW

Document contains brief description of DF6811CPU core functionality. The DF6811CPU is a advanced 8-bit MCU IP Core with highly sophisticated, on chip peripheral capabilities. DF6811CPU soft core is binary-compatible with the industry standard 68HC11 8-bit microcontroller and can achieve a performance **45-100 million instructions** per second. There are two configurations of DF6811CPU: **Harvard** where data and program buses are separated, and **von Neumann** with common program and data bus DF6811CPU has FAST architecture that is 4.4 times faster compared to original implementation.

Self-monitoring circuitry is included on-chip to protect against system errors. An illegal opcode detection circuit provides a non-maskable interrupt when illegal opcode detected.

Two software-controlled power-saving modes, WAIT and STOP, are available to conserve additional power. These modes make the DF6811CPU IP Core especially attractive for automotive and battery-driven applications.

The DF6811CPU have built in the development support features designed into DF6811. The LIR signal is intended as a debugging aid. This signal is driven to active low for the first bus cycle of each new instruction, making it easy to reverse assemble (disassemble) instructions from the display of a logic analyzer.

DF6811CPU is **fully customizable**, which means it is delivered in the exact configuration to meet users requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

FEATURES

- FAST architecture, 4,4 times faster than the original implementation
- Software compatible with industry standard 68HC11
- Configurable Harvard or Von Neumann architectures
- 10 times faster multiplication
- 16 times faster division
- 256 bytes of remapped System Function Registers space (SFRs)
- Up to 16M bytes of Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Two power saving modes: STOP, WAI
- Ready pin allows Core to operate with slow program and data memories
- Fully synthesizable, static synchronous design with no internal tri-states

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- No internal reset generator or gated clock
- Scan test ready
- Technology independent HDL source code
- Core can be fully customized
- 1 GHz virtual clock frequency compared to original implementation
- DoCD™ on Chip Debugger
  - *Processor execution control*
  - *Read, write all processor contents*
  - *Hardware execution breakpoints*
  - *Three wire communication interface*

DESIGN FEATURES

♦ ONE GLOBAL SYSTEM CLOCK

♦ SYNCHRONOUS RESET

The DF6811 has 3 reset vectors sources, which easy identify a cause of system reset.

♦ ALL ASYNCHRONOUS INPUT SIGNALS ARE SYNCHRONIZED BEFORE INTERNAL USE

✓ DATA MEMORY:

The DF6811 can address up to 16M bytes of Data Memory via the function interconnect signals. The 256 bytes of Data Memory in every 64k page is reserved for the Function Registers. Extra DPP (Data Page Pointer) register is used for segments swapping. Data Memory can be implemented as synchronous or asynchronous RAM.

✓ SYSTEM FUNCTION REGISTERS:

Up to 256 System Function Registers(SFRs) may be implemented to the DF6811 design. SFRs are memory mapped into Data Memory within any 64k bytes address space.

✓ PROGRAM MEMORY:

Up to 64kB of Program Memory may be implemented to the DF6811 design. Program Memory can be implemented as synchronous or asynchronous ROM.

DELIVERABLES

- Source code:
  - ◊ VHDL Source Code or/and
  - ◊ VERILOG Source Code or/and
  - ◊ Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - ◊ Active-HDL automatic simulation macros
  - ◊ ModelSim automatic simulation macros
  - ◊ Tests with reference responses
- Technical documentation
  - ◊ Installation notes
  - ◊ HDL core specification
  - ◊ Datasheet
- Synthesis scripts
- Example application
- Technical support
  - ◊ IP Core implementation support
  - ◊ 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

CONFIGURATION

The following parameters of the DF6811CPU core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• DoCD™ Hardware Debugger	- used - unused
• Architecture type	- Harvard - Von Neumann
• Memories type	- Synchronous - Asynchronou
• Data Memory size	- 64 kB - 16 MB
• Data Memory wait-states	- used - unused
• Power saving STOP mode	- used - unused
• Support for DIV Instructions	- used - unused
• Support for MUL Instruction	- used - unused

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

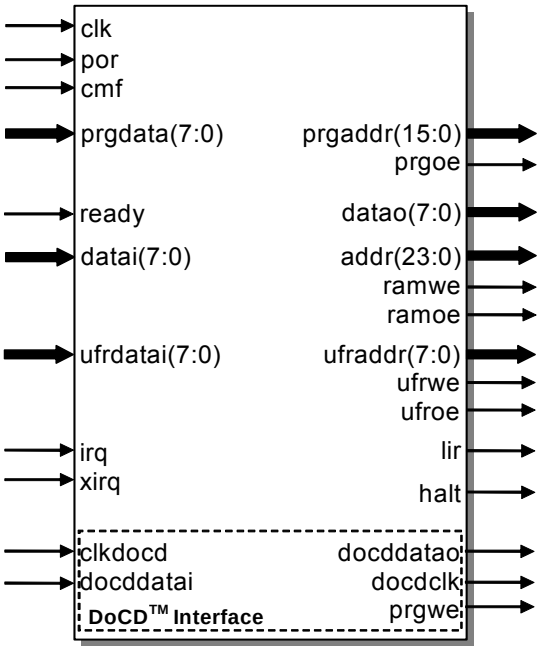
Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL



PINS DESCRIPTION

PIN	ACTIVE	TYPE	DESCRIPTION
clk	-	input	Global system clock
por	Low	input	Power on Reset indicator
cmf	Low	input	Clock Monitor Fail Reset ID
prgdata[7:0]	-	input	Program memory bus input
ready	Low	input	Non-maskable interrupt input
datai[7:0]	-	input	External memory bus input
ufrdatai[7:0]	-	input	UFRs data bus input
irq	Low	input	Ready pin for CODE & DATA
xirq	Low	input	Non-maskable interrupt input
prgaddr[15:0]	-	output	Program memory address bus
prgoe	-	output	Program memory output enable
datao[7:0]	-	output	Data memory & UFR bus output
addr[23:0]	-	output	Data memory address bus
ramwe	Low	output	Data memory write enable
ramoe	Low	output	Data memory output enable
ufraddr[7:0]	-	output	FR address bus
ufrwe	Low	output	UFRs write enable
ufroe	Low	output	UFRs output enable
lir	Low	output	Load instruction register
halt	High	output	Halt clock system (STOP inst.)

clkdocd	-	input	Separate DoCD™ Clock input
docddatai	-	input	DoCD™ serial Data input
docddatao	-	output	DoCD™ Serial Data Output
docdclk	-	output	DoCD™ Serial Clock Output
prgwe	-	output	DoCD™ Program Memory Write

*** Kind of activity is configurable**

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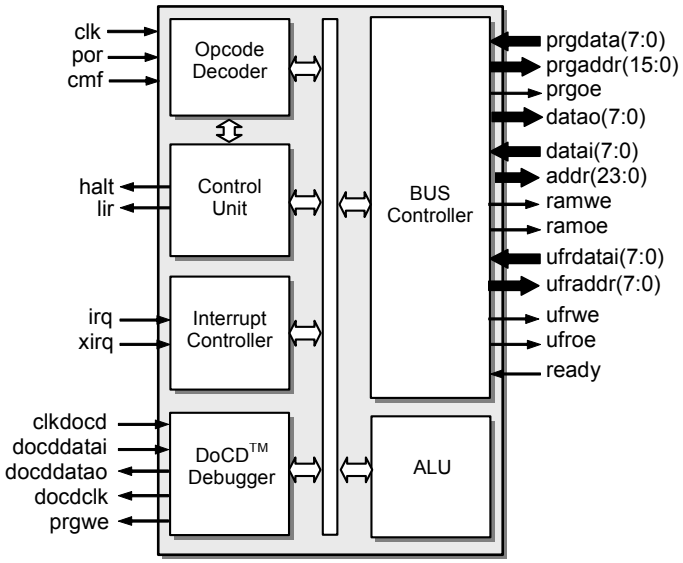
BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and waking-up the processor from the STOP mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks**.**

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), and related logic like arithmetic unit, logic unit, multiplier and divider.

Bus Controller – Program Memory, Data Memory & SFR's (Special Function Register) interface controls access into the program and data memories and special registers. It contains Program Counter (PC), Stack Pointer (SP) register, INIT register (INIT), Data Page Pointer (DPP), Stretch register (ST) and related logic.



Interrupt Controller - DF6811CPU has implemented only an external interrupts from pins IRQ and XIRQ. The interrupts are activated at low level (XIRQ,IRQ pins) or falling edge (IRQ pin) and are sampled each 1 system clock at the rising edge of CLK.

DoCD™ - Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

OPTIONAL MODULES

There are also available an optional peripherals, not included in presented DF6811CPU Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- Four 8-bit I/O Ports
- Interrupt Controller
  - *20 interrupt sources*
  - *17 priority levels*
  - *Dedicated Interrupt vector for each interrupt source*
- Main16-bit timer/counter system
  - *16 bit free running counter*
  - *Four stage programmable prescaller*
  - *Timer clocked by internal source*
  - *Real Time Interrupt*
- 16-bit Compare/Capture Unit
  - *Three independent input-capture functions*
  - *Five output-compare channels*
  - *Events capturing*
  - *Pulses generation*
  - *Digital signals generation*
  - *Gated timers*
  - *Sophisticated comparator*

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- *Pulse width modulation*
- *Pulse width measuring*

- 8-bit Pulse accumulator
  - *Two major modes of operation*
    - *Simple event counter*
    - *Gated time accumulation*
  - *Clocked by internal source or external pin*
- Full-duplex UART - SCI
  - *Standard Nonreturn to Zero format (NRZ)*
  - *8 or 9 bit data transfer*
  - *Integrated baud rate generator*
  - *Enhanced receiver data sampling technique*
  - *Noise, Overrun and Framing error detection*
  - *IDLE and BREAK characters generation*
  - *Wake-up block to recognize UART wake-up from IDLE condition*
  - *Three SCI related interrupts*
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- PWM – Pulse Width Modulation Timer
  - *4 independent 8-bit PWM channels, concatenated on two 16-bit PWM channel*
  - *Software-selectable duty from 0% to 100% and pulse period*
  - *Software-selectable polarity of output waveform*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*
- Programmable Watchdog Timer
- Fixed-Point arithmetic coprocessor
  - *Multiplication - 16bit * 16bit*
  - *Division - 32bit / 16bit*
  - *Division - 16bit / 16bit*
  - *Left and right shifting - 1 to 31 bits*
  - *Normalization*

- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
  - *FADD, FSUB - addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM - compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
  - *FADD, FSUB- addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM- compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
  - *FSIN, FCOS- sine, cosine*
  - *FTAN, FATAN – tangent arcs tangent*

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	1834	58 MHz
STRATIX	-5	1834	60 MHz
MERCURY	-5	1808	61 MHz
APEX II	-7	1849	50 MHz
APEX20KC	-7	1809	46 MHz
APEX20KE	-1	1809	42 MHz
ACEX1K	-1	1785	34 MHz
FLEX10KE	-1	1785	32 MHz

Core performance in ALTERA® devices

IMPROVEMENT

For user the most important is application speed improvement. The most commonly used arithmetic functions and theirs improvement are shown in table below. Improvement was computed as {M68HC11 clock periods} divided by {DF6811CPU clock periods} required to execute an identical function. More details are available in core documentation.

Function	Improvement
8-bit addition (*immediate data*)	**4**
8-bit addition (*direct addressing*)	**4**
8-bit addition (*indirect addressing*)	**4**
8-bit subtraction (*immediate data*)	**4**
8-bit subtraction (*direct addressing*)	**4**
8-bit subtraction (*indirect addressing*)	**4**
16-bit addition (*immediate data*)	**5,3**
16-bit addition (*direct addressing*)	**5**
16-bit addition (*indirect addressing*	**4,8**
16-bit subtraction (*immediate data*)	**5,3**
16-bit subtraction (*direct addressing*)	**5**
16-bit subtraction (*indirect addressing*	**4,8**
Multiplication	**10**
Fractional division	**14,9**
Integer division	**16.4**

DF68XX FAMILY OVERVIEW

The main features of each DF68XX family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Speed acceleration	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	READY for Prg. and Data memories	Compare\Capture	Main Timer System	SCI (UART)	I\O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs	DoCD Debugger	Size – ASIC gates
DF6805	4.1	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	+	✓*	-	✓	✓	6 700
DF6808	3.2	64k	64k	-	7	7	-	-	*	2/2*	1*	✓*	4	✓	✓*	-	✓	✓	8 900
DF6811	4.4	64k	16M	-	20	17	✓	1*	*	5/3*	1*	✓*	4	✓*	✓*	✓*	✓	✓	12 000
DF6811CPU	4.4	64k	16M	-	3	3	+	1*	*	+	+	+	+	+	+	+	✓	✓	6 500

DF68XX family of High Performance Microcontroller Cores

\+ optional
* configurable

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CONTACTS

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