# NPC

**SM5816AF**

## 6-channel DSD-PCM Converter

## OVERVIEW

The SM5816AF is a 6-channel DSD data to 6-channel 8fs or 2fs PCM data converter IC. During conversion, decimation filtering is performed using a filter with selectable fixed coefficients (4 sets) or optional filter coefficients that are written to the built-in RAM. Also, DSD input/outputs and PCM outputs are available for use in master/slave clock mode operation, in a wide range of system configurations, making it easy to construct a multi-channel DSD/PCM reproduction system.

## FEATURES

- 512fs master clock (22.5792MHz, fs = 44.1kHz)
- DSD inputs connected directly to outputs in through mode
- Clock master/slave switching for DSD input/outputs and PCM outputs
- 2-system external data inputs (3-wire), with 2fs output data BCK and LRCK pins switchable between external inputs and internal filter outputs
- Decimation filter characteristics
  - Fixed coefficients: 4 sets (8fs), 1 set (2fs)
  - Rewritable coefficients: 1 set (29 bit × 240 word)
- Dither rounding function in 8fs/24-bit output mode, with switchable ON/OFF and summing position
- PCM/DSD output independent muting operation
- 8fs output format: [MSB-first left-justified 32-bit] or [MSB-first right-justified 24-bit]
- 2fs output format: [MSB-first left-justified 32-bit] or [IIS 32-bit]
- +6dB DSD gain switching function
- System clock output switchable between external system clock and internal system clock
- 3.3V ± 10% supply voltage
- 5V tolerant inputs for direct connection to 5V logic outputs
- −20 to 70°C operating temperature range
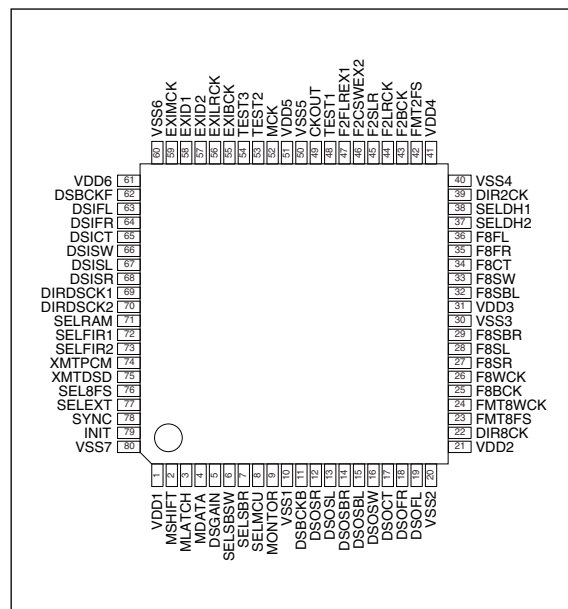- 80-pin QFP package

## APPLICATIONS

- Multi-channel SA-CD players
- SA-CD-compatible AV amplifiers

## ORDERING INFORMATION

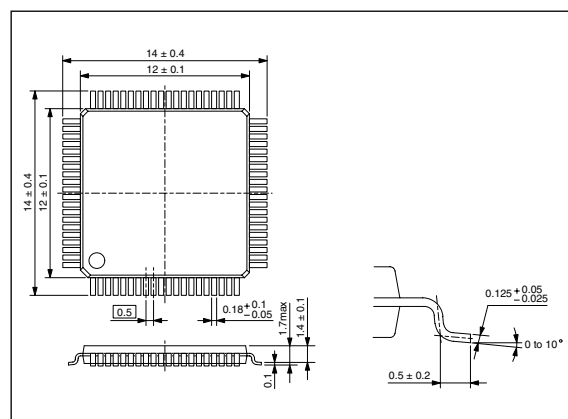| Device | Package |
|--------|---------|
| SM5816AF | 80-pin QFP |

## PINOUT

(Top view)



## PACKAGE DIMENSIONS

(Unit: mm)

## PIN DESCRIPTION

| No. | Name | I/O | Property[1] | Output current | Input voltage | Description |
|-----|------|-----|-------------|----------------|---------------|-------------|
| 1 | VDD1 | – | – | – | – | Supply pin 1 |
| 2 | MSHIFT | I | S | – | 3.3/5 | Serial control: shift clock |
| 3 | MLATCH | I | S | – | 3.3/5 | Serial control: latch clock |
| 4 | MDATA | I | S | – | 3.3/5 | Serial control: command data |
| 5 | DSGAIN | I | PD | – | 3.3/5 | DSD signal gain setting<br>L: 100% modulation = 0dB, H: 50% modulation = 0dB |
| 6 | SELSBSW | I | PD | – | 3.3/5 | DSD-SW input to SW/(SBL, SBR) output select<br>L: SW input to SW output, H: SW input to (SBL, SBR) output<br>Note. It effects both of DSD and 8fs outputs. |
| 7 | SELSBR | I | PD | – | 3.3/5 | DSD 8fs-(SBL, SBR) output select<br>L: SBL output only, H: both SBL, SBR output<br>Note: Valid only when SELSBSW is HIGH. |
| 8 | SELMCU | I | PD | – | 3.3/5 | Control method select<br>L: pin control, H: serial interface data control |
| 9 | MONTOR | O | – | 2mA | – | Parameter change monitor output |
| 10 | VSS1 | – | – | – | – | Ground pin 1 |
| 11 | DSBCKB | I/O | S | 6mA | 3.3/5 | DSD through-mode data output: bit clock, controlled by DIRDSCK1, 2 |
| 12 | DSOSR | O | – | 2mA | – | DSD through-mode data output: surround right-channel |
| 13 | DSOSL | O | – | 2mA | – | DSD through-mode data output: surround left-channel |
| 14 | DSOSBR | O | – | 2mA | – | DSD through-mode data output: surround back right-channel |
| 15 | DSOSBL | O | – | 2mA | – | DSD through-mode data output: surround back left-channel |
| 16 | DSOSW | O | – | 2mA | – | DSD through-mode data output: subwoofer channel |
| 17 | DSOCT | O | – | 2mA | – | DSD through-mode data output: center channel |
| 18 | DSOFR | O | – | 2mA | – | DSD through-mode data output: front right-channel |
| 19 | DSOFL | O | – | 2mA | – | DSD through-mode data output: front left-channel |
| 20 | VSS2 | – | – | – | – | Ground pin 2 |
| 21 | VDD2 | – | – | – | – | Supply pin 2 |
| 22 | DIR8CK | I | PD | – | 3.3/5 | 8fs output F8BCK, F8WCK input/output select<br>L: output (master mode), H: Input (slave mode) |
| 23 | FMT8FS | I | PD | – | 3.3/5 | 8fs PCM format (MSB-first)<br>L: MSB-first left-justified 32-bit, H: MSB-first right-justified 24-bit<br>Note: In 8fs right-justified 24-bit format, there are a fixed 32 bit clock (F8BCK) cycles per word clock (F8WCK) cycle.<br>Note: In 8fs right-justified 24-bit format, the upper empty bits are for sign extension. |
| 24 | FMT8WCK | I | PD | – | 3.3/5 | 8fs PCMWCK format<br>L: "H" → "L" (rising-edge word boundary)<br>H: "L" → "H" (falling edge word boundary) |
| 25 | F8BCK | I/O | S | 6mA | 3.3/5 | 8fs PCM BCK (bit clock) |
| 26 | F8WCK | I/O | S | 6mA | 3.3/5 | 8fs PCM WCK (word clock) |
| 27 | F8SR | O | – | 2mA | – | 8fs PCM data output: surround right-channel |
| 28 | F8SL | O | – | 2mA | – | 8fs PCM data output: surround left-channel |
| 29 | F8SBR | O | – | 2mA | – | 8fs PCM data output: surround back right-channel |
| 30 | VSS3 | – | – | – | – | Ground pin 3 |
| 31 | VDD3 | – | – | – | – | Supply pin 3 |
| 32 | F8SBL | O | – | 2mA | – | 8fs PCM data output: surround back left-channel |
| 33 | F8SW | O | – | 2mA | – | 8fs PCM data output: subwoofer channel |
| 34 | F8CT | O | – | 2mA | – | 8fs PCM data output: center channel |

| No. | Name | I/O | Property[1] | Output current | Input voltage | Description |
|---|---|---|---|---|---|---|
| 35 | F8FR | O | – | 2mA | – | 8fs PCM data output: front right-channel |
| 36 | F8FL | O | – | 2mA | – | 8fs PCM data output: front left-channel |
| 37 | SELDH2 | I | PD | – | 3.3/5 | Output dither rounding ON/OFF and summing position select |
| 38 | SELDH1 | I | PD | – | 3.3/5 | <table><tr><td>SELDH (2, 1)</td><td>(L, L)</td><td>(L, H)</td><td>(H, L)</td><td>(H, H)</td></tr><tr><td>Dither</td><td>OFF</td><td>1LSB</td><td>2LSB</td><td>4LSB</td></tr></table> |
| 39 | DIR2CK | I | PD | – | 3.3/5 | 2fs output F2BCK, F2LRCK input/output select<br>L: output (master mode), H: input (slave mode)<br>Note: In 2fs-PCM output, when external inputs (EXID1, EXID2) are selected for output (SELEXT = "H"), the DIR2CK setting is inactive, and EXILRCK and EXIBCK are output as-is on F2LRCK and F2BCK, respectively. |
| 40 | VSS4 | – | – | – | – | Ground pin 4 |
| 41 | VDD4 | – | – | – | – | Supply pin 4 |
| 42 | FMT2FS | I | PD | – | 3.3/5 | 2fs PCM format<br>L: MSB-first left-justified 32-bit, H: IIS 32-bit<br>Note: In 2fs IIS 32-bit format, there are 64 F2BCK clock cycles per F2LRCK clock cycle. |
| 43 | F2BCK | I/O | S | 6mA | 3.3/5 | 2fs or external data BCK |
| 44 | F2LRCK | I/O | S | 6mA | 3.3/5 | 2fs or external data LRCK |
| 45 | F2SLR | O | – | 2mA | – | 2fs PCM data output: surround left/right-channel |
| 46 | F2CSWEX2 | O | – | 2mA | – | 2fs PCM data output: center/subwoofer channel or external data 2 output |
| 47 | F2FLREX1 | O | – | 2mA | – | 2fs PCM data output: front left/right-channel or external data 1 output |
| 48 | TEST1 | I | PD, S | – | 3.3/5 | Test pin 1 (must be open or tie LOW for normal operation) |
| 49 | CKOUT | O | – | 12mA | – | System clock output. Clock output selected by SELEXT. |
| 50 | VSS5 | – | – | – | – | Ground pin 5 |
| 51 | VDD5 | – | – | – | – | Supply pin 5 |
| 52 | MCK | I | – | – | 3.3/5 | Master clock input: 512fs (22.5792MHz, fs = 44.1kHz) |
| 53 | TEST2 | I | PD | – | 3.3/5 | Test pin 2 (must be open or tie LOW for normal operation) |
| 54 | TEST3 | I | PD | – | 3.3/5 | Test pin 3 (must be open or tie LOW for normal operation) |
| 55 | EXIBCK | I | S | – | 3.3/5 | External PCM data BCK input |
| 56 | EXILRCK | I | S | – | 3.3/5 | External PCM data LRCK input |
| 57 | EXID2 | I | – | – | 3.3/5 | External PCM data input 2 |
| 58 | EXID1 | I | – | – | 3.3/5 | External PCM data input 1 |
| 59 | EXIMCK | I | – | – | 3.3/5 | External system clock input |
| 60 | VSS6 | – | – | – | – | Ground pin 6 |
| 61 | VDD6 | – | – | – | – | Supply pin 6 |
| 62 | DSBCKF | I/O | S | 6mA | 3.3/5 | DSD data input bit clock. Controlled by DIRDSCK1, 2 |
| 63 | DSIFL | I | – | – | 3.3/5 | DSD data input: front left-channel |
| 64 | DSIFR | I | – | – | 3.3/5 | DSD data input: front right-channel |
| 65 | DSICT | I | – | – | 3.3/5 | DSD data input: center channel |
| 66 | DSISW | I | – | – | 3.3/5 | DSD data input: subwoofer channel |
| 67 | DSISL | I | – | – | 3.3/5 | DSD data input: surround left-channel |
| 68 | DSISR | I | – | – | 3.3/5 | DSD data input: surround right-channel |
| 69 | DIRDSCK1 | I | PD | – | 3.3/5 | DSBCKF I/O select<br>L: input (slave), H: output (master) |
| 70 | DIRDSCK2 | I | PD | – | 3.3/5 | DSBCKB I/O select<br>L: output (master), H: input (slave) |

| No. | Name | I/O | Property[1] | Output current | Input voltage | Description |
|-----|------|-----|----------|----------------|---------------|-------------|
| 71 | SELRAM | I | PD | – | 3.3/5 | FIR coefficient ROM/RAM select<br>L: ROM, H: RAM |
| 72 | SELFIR1 | I | PD | – | 3.3/5 | FIR coefficient (ROM) select |
| 73 | SELFIR2 | I | PD | – | 3.3/5 | <table><tr><td>SELFIR (2, 1)</td><td>(L, L)</td><td>(L, H)</td><td>(H, L)</td><td>(H, H)</td></tr><tr><td>FIR coeff</td><td>coeff 1</td><td>coeff 2</td><td>coeff 3</td><td>coeff 4</td></tr></table> |
| 74 | XMTPCM | I | PD | – | 3.3/5 | PCM output mute control input<br>L: mute-ON, H: mute-OFF |
| 75 | XMTDSD | I | PD | – | 3.3/5 | DSD output mute control input<br>L: mute-ON, H: mute-OFF |
| 76 | SEL8FS[2, 3] | I | PD | – | 3.3/5 | PCM output rate select<br>L: 2fs, H: 8fs |
| 77 | SELEXT[2, 3] | I | PD | – | 3.3/5 | 2fs output/external data output select<br>L: 2fs data, H: external data (EXID1, EXID2) |
| 78 | SYNC[4] | I | S | – | 3.3/5 | Forced sync control. Sync on rising edge |
| 79 | INIT[4, 5] | I | S | – | 3.3/5 | Initialization control.<br>Active-LOW. Resync on "L" → "H" |
| 80 | VSS7 | – | – | – | – | Ground pin 7 |

1. S = Schmitt, PD = pull-down resistor
2. The SEL8FS setting takes precedence over the SELEXT setting. In other words, 8fs PCM output is selected when SEL8FS is HIGH, and the SELEXT settings are not effective. The SELEXT also selects relevant clock pins (F2LRCK, F2BCK, CKOUT).
3. Outputs not selected by SEL8FS and SELEXT are treated as described below:
   - Data signals are tied LOW.
   - When I/O pins F8WCK, F8BCK, F2LRCK, F2WCK are set as outputs, they function as outputs.
   When they are set as inputs, they are ignored in input mode.
4. The output data is synchronized each time by event-driven operation despite the clock input/output. The resynchronization operation occurs to avoid reading DSD input data at the falling edge of DSBCKF.
5. The internal flip-flops are all initialized in response to an active level on INIT, and outputs are tied HIGH or LOW during INIT active level input.

# BLOCK DIAGRAM
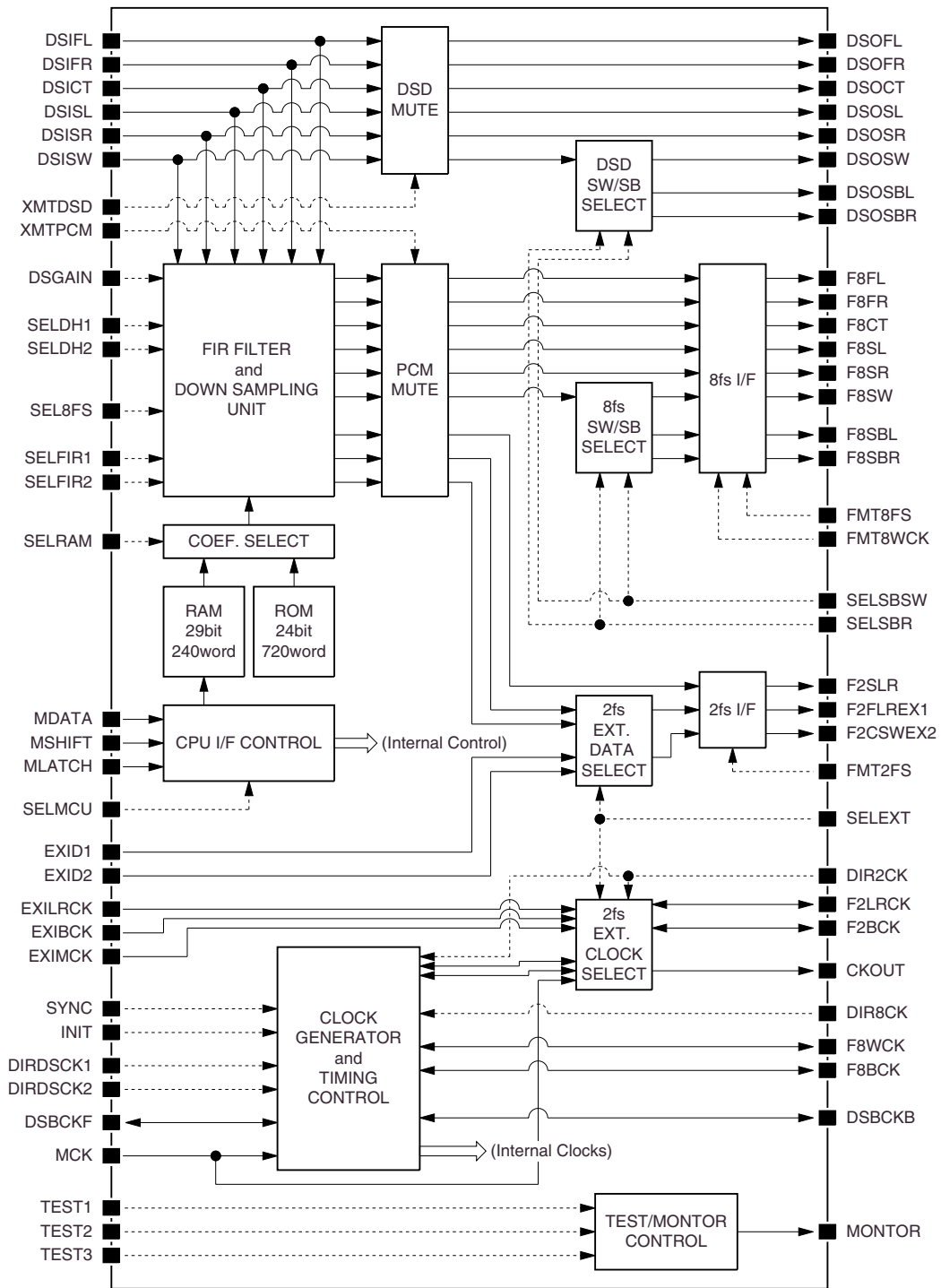
# SPECIFICATIONS

## Absolute Maximum Ratings

$V_{SS} = 0V$

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | − 0.3 to 4.0 | V |
| Input voltage 1 (3.3V) | $V_{IN1}$ | − 0.3 to $V_{DD}$ + 0.5 | V |
| Input voltage 2 (3.3V/5V)[1] | $V_{IN2}$ | − 0.3 to 7.0 | V |
| Power dissipation | $P_W$ | 300 | mW |
| Storage temperature | $T_{STG}$ | − 55 to 125 | °C |

1. Input voltage 2 applies to pins with 5V input rating.

## Recommended Operating Conditions

$V_{SS} = 0V$

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 to 3.6 | V |
| Operating temperature | $T_{OPR}$ | − 20 to 70 | °C |

## DC Electrical Characteristics

$V_{DD}$ = 3.0 to 3.6V, $V_{SS}$ = 0V, $T_{OPR}$ = − 20 to 70°C unless otherwise noted.

| Parameter | | Pin | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | min | typ | max | |
| Current consumption | | VDD | $I_{DD}$ | All pins no load | – | – | 80 | mA |
| Input voltage | "H" level | (*1) | $V_{IH}$ | $V_{DD}$ = 3.6V | 2.0 | – | – | V |
| | "L" level | (*1) | $V_{IL}$ | $V_{DD}$ = 3.0V | – | – | 0.8 | V |
| Schmitt-trigger voltage | Positive | (*2) | $V_{T+}$ | | 1.1 | – | 2.4 | V |
| | Negative | (*2) | $V_{T-}$ | | 0.6 | – | 1.8 | V |
| Hysteresis voltage | | (*2) | $V_H$ | | 0.1 | – | – | V |
| Output voltage | "H" level | (*3) | $V_{OH}$ | $I_{OH}$ = − 2mA (Type1) $I_{OH}$ = − 6mA (Type2) $I_{OH}$ = − 12mA (Type3) | $V_{DD}$ − 0.4 | – | – | V |
| | "L" level | (*3) | $V_{OL}$ | $I_{OL}$ = 2mA (Type1) $I_{OL}$ = 6mA (Type2) $I_{OL}$ = 12mA (Type3) | – | – | 0.4 | V |
| Input leakage current | | (*1, 2) | $I_{LI}$ | | − 1 | – | 1 | µA |
| Pull-down resistance | | (*4) | $R_{PD}$ | $V_I = V_{DD}$ | 40 | 100 | 240 | kΩ |

## Pin summary

| | |
|---|---|
| (*1) | Input pins and bidirectional (input/output) pins in input mode |
| (*2) | Inputs with Schmitt characteristic and bidirectional (input/output) pins in input mode |
| (*3) | Output pins and bidirectional (input/output) pins in output mode Type 3: CKOUT Type 2: DSBCKB, DSBCKF, F8BCK, F8WCK, F2BCK, F2LRCK Type 1: Outputs excluding those above |
| (*4) | Inputs with pull-down resistor |

## AC Electrical Characteristics

$V_{DD}$ = 3.0 to 3.6V, $V_{SS}$ = 0V, $T_{OPR}$ = – 20 to 70°C, fs = 44.1kHz unless otherwise noted.
If DSBCKF, DSBCKB, F8WCK, F2LRCK clocks are input externally, by frequency division the clock input on MCK has the following relationships.

(DSBCKF, DSBCKB) cycle = 8 × MCK cycle (64fs)
(F8WCK) cycle = 64 × MCK cycle (8fs)
(F2LRCK) cycle = 256 × MCK cycle (2fs)

### System clock

■ MCK pin

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| "H"-level pulsewidth | $t_{MCWH}$ | 13 | – | – | ns |
| "L"-level pulsewidth | $t_{MCWL}$ | 13 | – | – | ns |
| Pulse cycle | $t_{MCY}$ | 40 | 44.29 (1/512fs) | – | ns |
| Rise/fall time | $t_r$ , $t_f$ | – | – | 10 | ns |
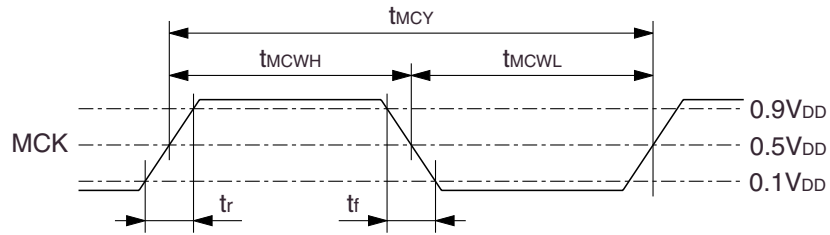


### External system clock

■ EXIMCK pin

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| "H"-level pulsewidth | $t_{ECWH}$ | 13 | – | – | ns |
| "L"-level pulsewidth | $t_{ECWL}$ | 13 | – | – | ns |
| Pulse cycle | $t_{ECY}$ | 40 | – | – | ns |
| Rise/fall time | $t_{er}$ , $t_{ef}$ | – | – | 10 | ns |
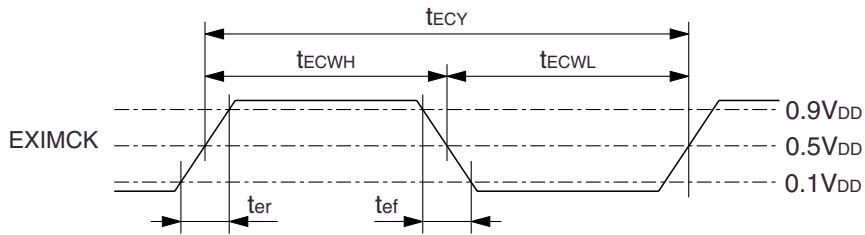
## DSD input/output

■ DSBCKF, DSBCKB pins
■ DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins
■ DSOFL, DSOFR, DSOSL, DSOSR, DSOCT, DSOSW, DSOSBL, DSOSBR pins

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| DSD clock pulsewidth | $t_{DSCW}$ | 150 | 177.16 | – | ns |
| DSD clock pulse cycle | $t_{DSCY}$ | 300 | 354.31 (1/64fs) | – | ns |
| DSD data setup time | $t_{DSS}$ | 50 | – | – | ns |
| DSD data hold time | $t_{DSH}$ | 50 | – | – | ns |
| DSD data delay time | $t_{DSDLY}$ | 0 | – | 15 | ns |
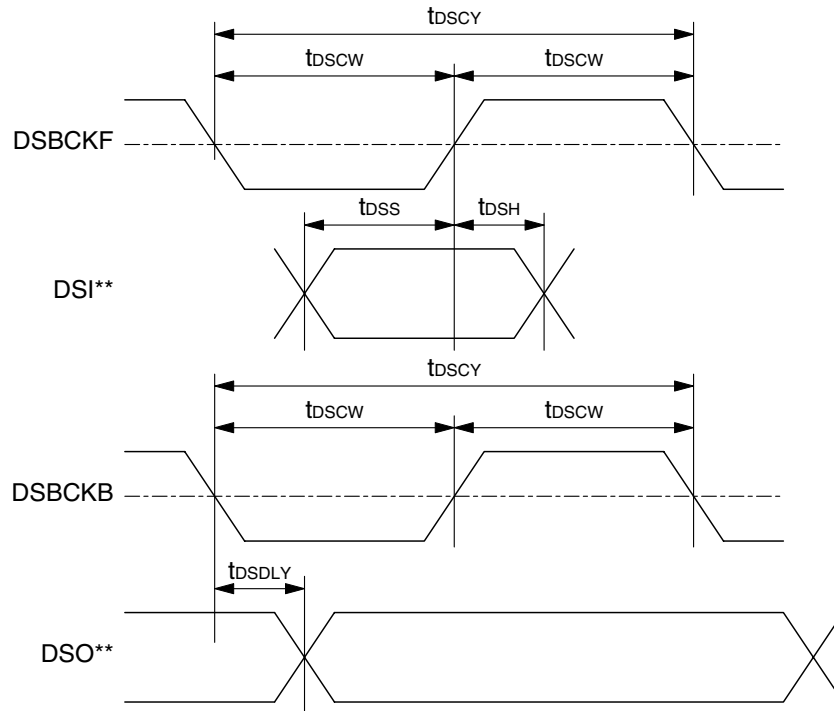
DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins
DSO**: DSOFL, DSOFR, DSOSL, DSOSR, DSOCT, DSOSW, DSOSBL, DSOSBR pins

Note. The DSD clock pulsewidth and clock pulse cycle are with both DSBCKF and DSBCKB in input mode.

Note. Data is read internally using the falling edge of MCK, using the DSBCKF timing above as the base. When the timing changes, resynchronization must be performed using INIT or SYNC.

## PCM output

- F8WCK, F8BCK, F8FL, F8FR, F8SL, F8SR, F8CT, F8SW, F8SBL, F8SBR pins
- F2LRCK, F2BCK, F2SLR, F2FLREX1, F2CSWEX2 pins

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| 8fs BCK clock pulsewidth | $t_{F8BCW}$ | 40 | 44.29 | – | ns |
| 8fs BCK clock pulse cycle | $t_{F8BCY}$ | 80 | 88.58 (1/256fs) | – | ns |
| 2fs BCK clock pulsewidth | $t_{F2BCW}$ | 40 | 88.58 | – | ns |
| 2fs BCK clock pulse cycle | $t_{F2BCY}$ | 80 | 177.15 (1/128fs) | – | ns |
| Word CK setup time | $t_{PLBS}$ | 30 | – | – | ns |
| Word CK hold time | $t_{PLBH}$ | 10 | – | – | ns |
| Bit CK data delay time | $t_{PBDLY}$ | 0 | – | 15 | ns |
| Word CK data delay time | $t_{PLDLY}$ | 0 | – | 15 | ns |
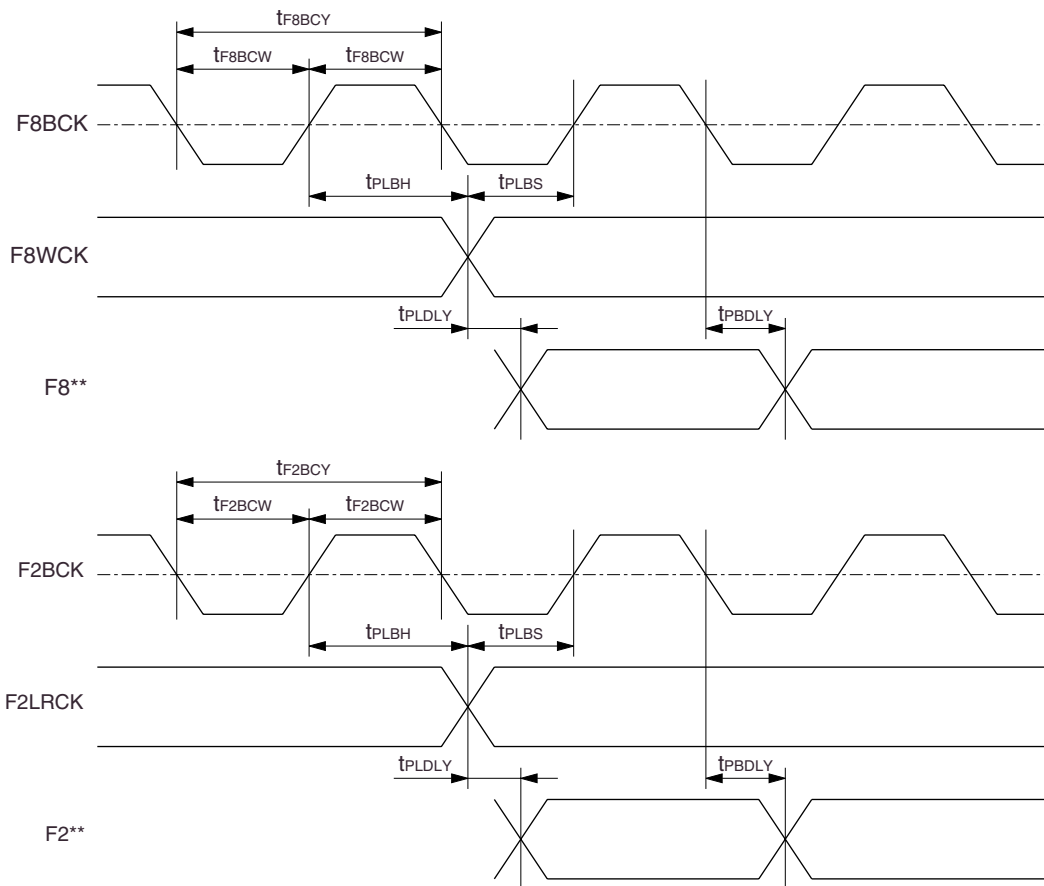


F8**: F8FL, F8FR, F8SL, F8SR, F8CT, F8SW, F8SBL, F8SBR pins
F2**: F2SLR, F2FLREX1, F2CSWEX2 pins

Note. The 2fs PCM output rating excludes external inputs (EXI**) in through mode.

Note. The 2fs/8fs bit clock and word clock relationship applies when F8BCK, F8WCK, F2BCK, F2LRCK pins are in input mode only.

## Clock outputs

■ CKOUT, DSBCKF, DSBCKB, F8WCK, F8BCK, F2LRCK, F2BCK pins

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| CKOUT output delay time | $t_{CKODLY}$ | 0 | – | 10 | ns |
| Clock output delay time | $t_{CKDLY}$ | 0 | – | 10 | ns |
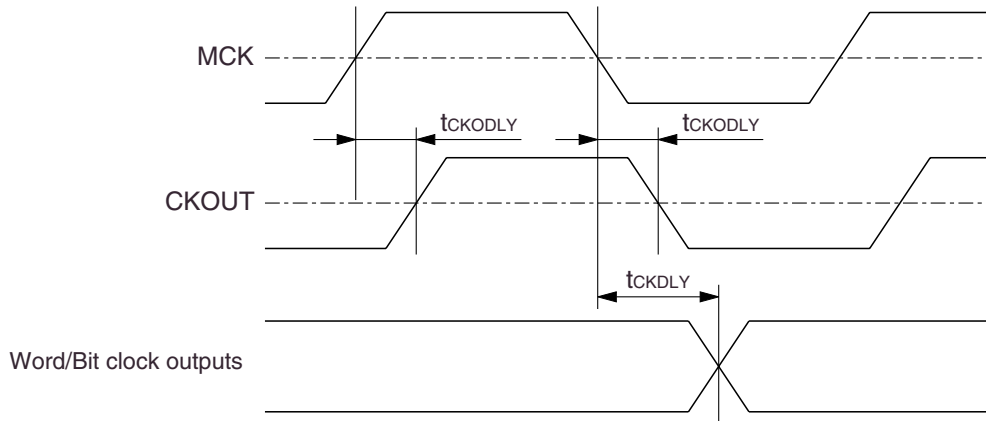


Note. Rating with MCK, in through mode, output on CKOUT.

Note. The word/bit clocks in output mode on pins F8BCK, F8WCK, F2BCK, F2LRCK, and DSBCKF, DSBCKB bidirectional pins in output mode.

## Through-mode output

■ DSBCKF, DSBCKB, CKOUT, F2BCK, F2LRCK, F2FLREX1, F2CSWEX2 pins

| Through inputs | Through outputs | Conditions | $t_{THDLY}$ MAX | Unit |
|---|---|---|---|---|
| DSBCKF | DSBCKB | DSBCKF in input mode, DSBCKB in output mode | 10 | ns |
| DSBCKB | DSBCKF | DSBCKF in output mode, DSBCKB in input mode | 10 | ns |
| EXIMCK | CKOUT | | 10 | ns |
| EXIBCK | F2BCK | | 10 | ns |
| EXIWCK | F2LRCK | 2fs PCM outputs with external inputs selected | 10 | ns |
| EXID1 | F2FLREX1 | | 15 | ns |
| EXID2 | F2CSWEX2 | | 15 | ns |
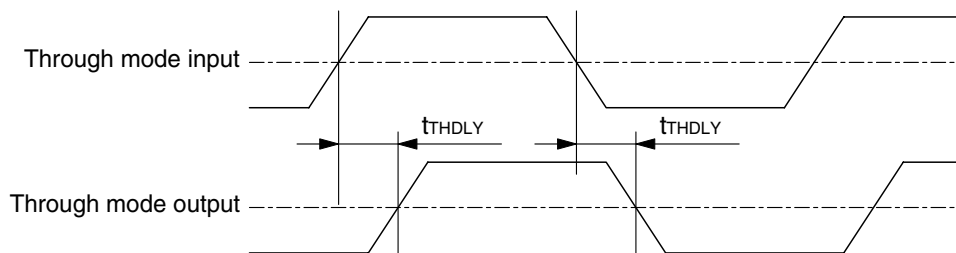
## CPU serial control interface

■ MSHIFT, MDATA, MLATCH pins

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| MSHIFT clock pulse frequency | $f_{MSCK}$ | – | – | 1 | MHz |
| MSHIFT clock pulsewidth | $t_{MSCW}$ | 480 | – | – | ns |
| MDATA setup time | $t_{MSDS}$ | 200 | – | – | ns |
| MDATA hold time | $t_{MSDH}$ | 200 | – | – | ns |
| MLATCH wait time | $t_{MLWT}$ | 200 | – | – | ns |
| MLATCH pulsewidth | $t_{MLPW}$ | $10 \times t_{MCY}$ | – | – | ns |
| MSHIFT wait time | $t_{MSWT}$ | 0 | – | – | ns |
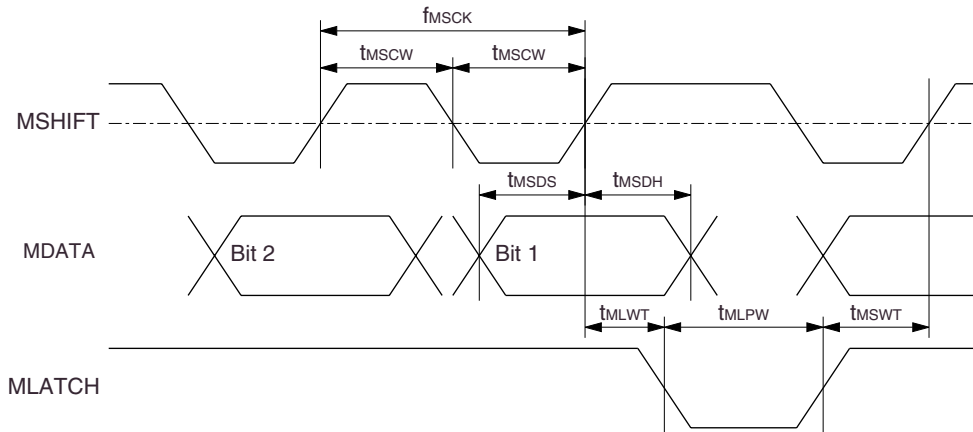


## Initialization and resynchronization

■ INIT, SYNC pins

| Parameter | Symbol | Rating | | | Unit |
|---|---|---|---|---|---|
| | | min | typ | max | |
| Initialization time | $t_{INTM}$ | $6 \times t_{MCY}$ | – | – | ns |
| Resynchronization pulsewidth | $t_{SYCW}$ | $6 \times t_{MCY}$ | – | – | ns |
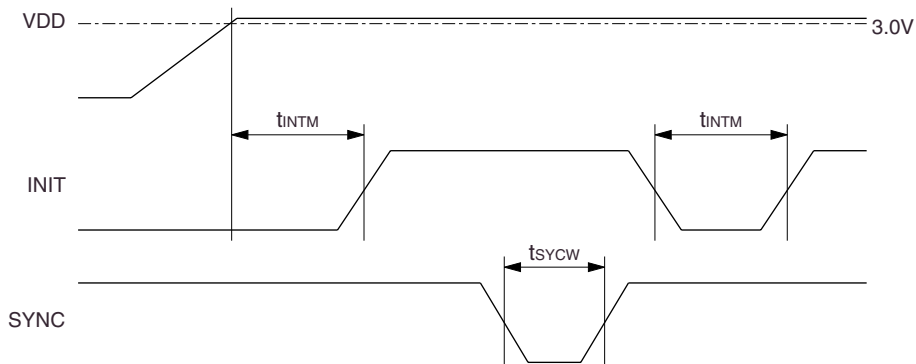
# FUNCTIONAL DESCRIPTION

## Data Input/Output Formats

### DSD input/output format

DSD input data is read on the rising edge of the bit clock, and output data is output on the falling edge.
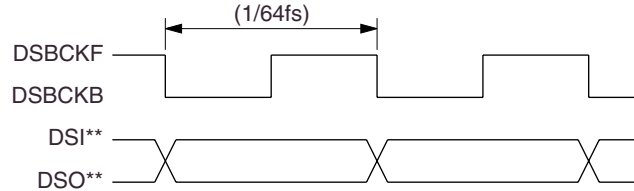


DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins
DSO**: DSOFL, DSOFR, DSOSL, DSOSR, DSOCT, DSOSW, DSOSBL, DSOSBR pins

### 8fs output format

There are two 8fs output formats that can be set using FMT8FS. Also, the F8WCK polarity can be inverted using FMT8WCK.

### (1) MSB-first left-justified 32-bit (FMT8FS = "L")
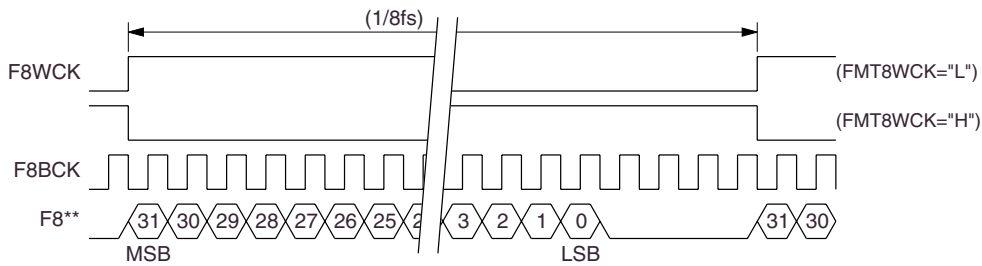


F8**: F8FL, F8FR, F8SL, F8SR, F8CT, F8SW, F8SBL, F8SBR pins

- If more than 32 bit clock cycles are input during each word clock cycle, data following the 32nd bit are output as "0".
- When F8WCK and F8BCK are set as outputs, there are 32 fixed bit clock cycles per word clock cycle.
- Output data is in 32-bit 2s complement format.

### (2) MSB-first right-justified 24-bit (FMT8FS = "H")
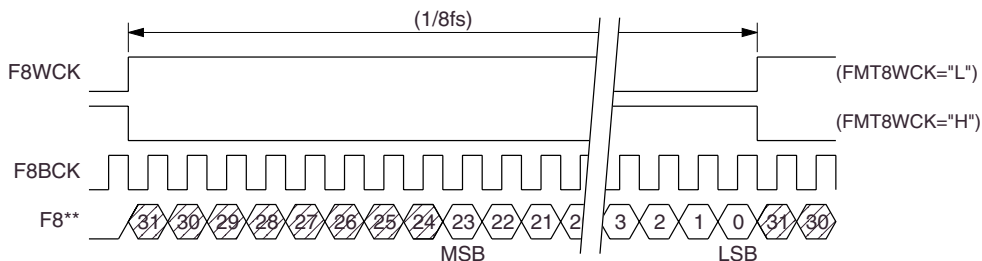


F8**: F8FL, F8FR, F8SL, F8SR, F8CT, F8SW, F8SBL, F8SBR pins

- In this format, there are 32 bit clock cycles per word clock cycle regardless of the input/output settings.
- The code bits are comprised by the 24-bit output data. The output data is output in 32-bit sign extended format (data bits are shown as slash lines)
- Output data is in 24-bit 2s complement format.

## 2fs output format

There are two 2fs output formats that can be set using FMT2FS. The output data is in 32-bit 2s complement format.
However, when external inputs (EXID1, EXID2, EXILRCK, EXIBCK) are selected, the signals are output as-is in through mode regardless of the format setting.

### (1) MSB-first left-justified 32-bit (FMT2FS = "L")
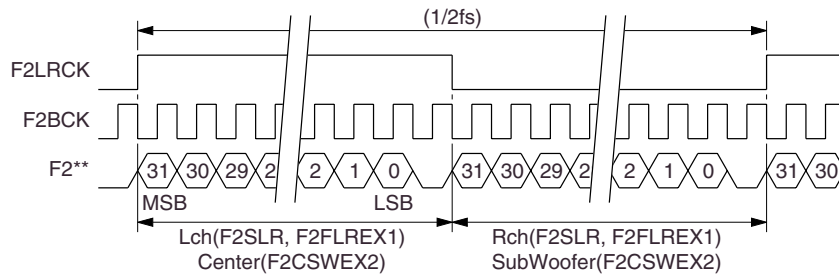


F2**: F2SLR, F2FLREX1, F2CSWEX2 pins

- If more than 32 bit clock cycles are input during each word clock cycle HIGH-level or LOW-level interval, data following the 32nd bit are output as "0".
- When F2LRCK and F2BCK are set as outputs, there are 32 fixed bit clock cycles per word clock cycle HIGH-level or LOW-level interval.

### (2) IIS 32-bit (FMT2FS = "H")
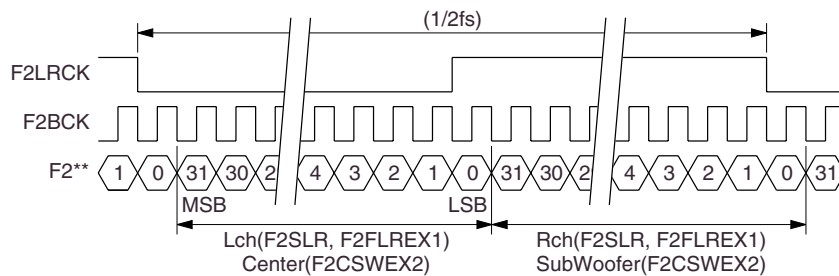


F2**: F2SLR, F2FLREX1, F2CSWEX2 pins

- In this format, there are 32 bit clock cycles per word clock cycle regardless of the input/output settings.

## Data Output Selection

### PCM output selection

The PCM output and decimation filter processing is set using SEL8FS and SELEXT, as shown in the following table.

| Setting | | PCM output system | | | | | | Clock output | Filter processing |
|---|---|---|---|---|---|---|---|---|---|
| | | 8fs output | | 2fs output | | | | | |
| SEL8FS | SELEXT | F8** | F8WCK F8BCK | F2SLR | F2FLREX1 | F2CSWEX2 | F2LRCK F2BCK | CKOUT | |
| L | L | "0" | invalid | DSISL DSISR | DSIFL DSIFR | DSICT DSISW | 2fs valid | MCK | 2fs 480th-order |
| L | H | "0" | invalid | "0" | EXID1 | EXID2 | EXILRCK EXIBCK | EXIMCK | invalid |
| H | L or H | DSI** | 8fs valid | "0" | "0" | "0" | invalid | MCK | 8fs 240th-order |

Note. F8**: F8FL, F8FR, F8SL, F8SR, F8CT, F8SW, F8SBL, F8SBR pins
DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins

■ The 8fs/2fs select setting (SEL8FS) takes precedence over the 2fs output external data setting (SELEXT).
■ The 8fs/2fs word clock (F8WCK, F2LRCK) and bit clock (F8BCK, F2BCK) are output, even when not selected ("invalid"), in output mode when external input is not selected.

### 8-channel subwoofer/surround back output switching

The DSD output and 8fs PCM output are set using SELSBSW and SELSBR, and the subwoofer output can be switched between surround back left and right channels.

| Setting | | PCM output system | | | | | |
|---|---|---|---|---|---|---|---|
| | | DSD output | | | 8fs PCM output | | |
| SELSBSW | SELSBR | DSOSW | DSOSBL | DSOSBR | F8SW | F8SBL | F8SBR |
| L | L or H | DSOSW | Mute Pattern | Mute Pattern | F8SW | "0" | "0" |
| H | L | Mute Pattern | DSOSW | Mute Pattern | "0" | F8SW | "0" |
| H | H | Mute Pattern | DSOSW | DSOSW | "0" | F8SW | F8SW |

■ The DSD mute output has a 50% duty "55h" continuous mute pattern.

## Clock Input/Output Selection and Synchronization Operation

### DSD clock input/output switching

The DSD input bit clock (DSBCKF) and DSD output bit clock (DSBCKB) are switched using DIRDSCK1, 2 as shown in the following table.
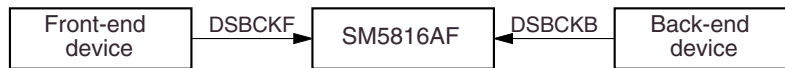
| Setting | | I/O state | |
|---|---|---|---|
| **DIRDSCK1** | **DIRDSCK2** | **DSBCKF** | **DSBCKB** |
| L | L | IN (Slave) | OUT (Master) |
| L | H | IN (Slave) | IN (Slave) |
| H | L | OUT (Master) | OUT (Master) |
| H | H | OUT (Master) | IN (Slave) |

### Reference connection diagram

(1) DIRDSCK1, 2 = (L, L)
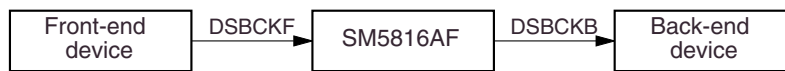


(2) DIRDSCK1, 2 = (L, H)



(3) DIRDSCK1, 2 = (H, L)



(4) DIRDSCK1, 2 = (H, H)
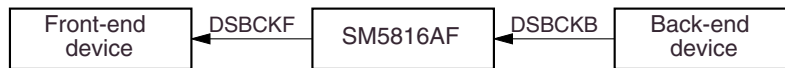


Note. In mode (1) and (4) in the diagram above, the input clocks are output as-is in through mode.

### PCM clock input/output switching

The 8fs and 2fs word/bit input/output clocks can be switched using DIR8CK and DIR2CK.

Note when external data is selected using SEL8FS and SELEXT, F2LRCK and F2BCK become outputs despite the state of DIR2CK, so care must be taken with external connections.

The I/O settings for the data output mode selected are shown in the following table.

| Mode | Mode setting | | 2fs clock I/O state | | 8fs clock I/O state | |
|---|---|---|---|---|---|---|
| | **SEL8FS** | **SELEXT** | **DIR2CK** | **F2LRCK F2BCK** | **DIR8CK** | **F8WCK F8BCK** |
| 2fs | L | L | L | OUT (Master) | L | OUT (clock output) |
| | | | H | IN (Slave) | H | IN (invalid) |
| EXT | L | H | L | OUT (EXILRCK, EXIBCK) | L | OUT (clock output)[1] |
| | | | H | OUT (EXILRCK, EXIBCK) | H | IN (invalid) |
| 8fs | H | L or H | L | OUT (clock output) | L | OUT (Master) |
| | | | H | IN (invalid) | H | IN (Slave) |

1. When external data is output in 2fs mode, MCK stops and the 8fs clock output stays stopped.

## Input clock sync operation and resynchronization

The data output internal operation and interface processing occur as event driven operations using the word clock word boundary as the event trigger, hence the output signals are always synchronized regardless of the word clock and bit clock I/O state.

As regards DSD input, the data (BUF_A) on the rising edge of bit clock (DSBCKF) and data (BUF_B) one half of the bit clock period later are selected and read in when the DSD output and PCM output event starts, to avoid the transitions in the DSD input signal.

At this time, the sync operation that determines which data was read in, after the INIT and SYNC rising edge, occurs when the word clock word boundary is detected after the first DSBCKF falling edge.
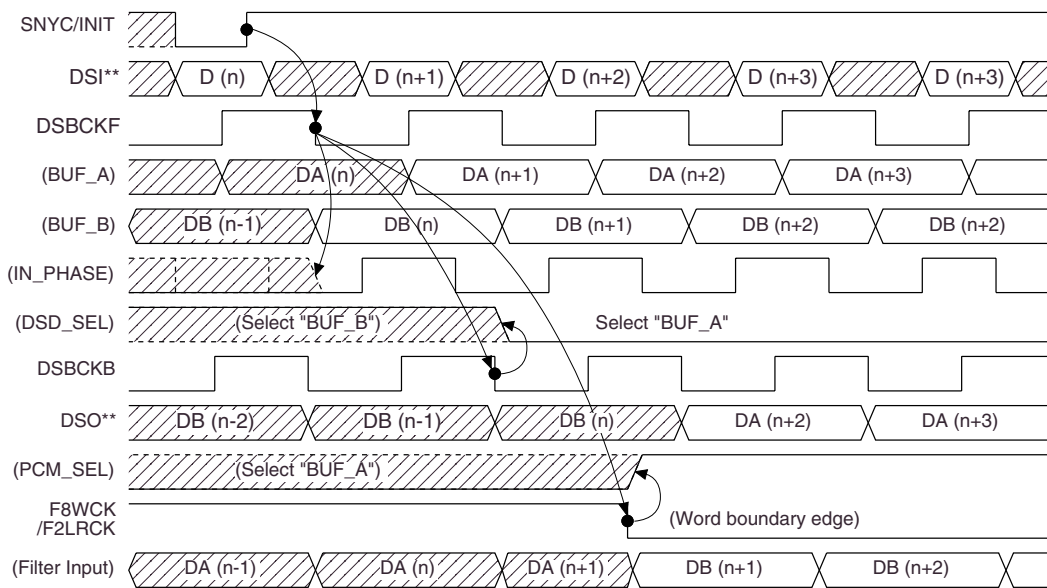


DSI**: DSIFL, DSIFR, DSISL, DSISR, DSICT, DSISW pins
DSO**: DSOFL, DSOFR, DSOSL, DSOSR, DSOCT, DSOSW, DSOSBL, DSOSBR pins

Figure 1. Input timing sync operation due to INIT, SYNC

1) After the SYNC/INIT rising edge is detected, the phase reference signal (IN_PHASE) for the input data buffer selected is determined on the first DSBCKF falling edge.

2) Then, after the IN_PHASE transition, the subsequent data buffer is determined on the first DSBCKB edge and F8WCK/F2LRCK word boundary edge.
   (The input data buffer selection for DSD output and PCM output is independent.)

Synchronization adjustment due to INIT/SYNC edge may cause 1 DSD data bit to be lost or made redundant due to input/output clock phase difference. If this would be problem, individual outputs should be muted for the following intervals.

[DSD output]      4 DSBCKB (64fs) clock cycles

[8fs PCM output]  34 F8WCK (8fs) clock cycles

[2fs PCM output]  18 F2LRCK (2fs) clock cycles

**2fs PCM select external input data and external system clock output switching**

(1) Switching to external input data

When SELEXT goes from LOW to HIGH, F2FLREX1 and F2CSWEX2 PCM data outputs are directly switched from EXID1 and EXID2 inputs.
Similarly, F2LRCK and F2BCK are directly switched, regardless of the DIR2CK setting, from EXILRCK and EXIBCK inputs.

(2) Switching to external system clock

The CKOUT output is switched from MCK or EXIMCK inputs, according to the state of SELEXT

SELEXT = "L": MCK output

SELEXT = "H": EXIMCK output

However, both MCK and EXIMCK should not be stopped during the switching interval to avoid a momentary pulse from occurring when switching.
Also, the switching interval, from initial setting until both clocks have each switched 4 times, has a LOW-level pulse that continues longer than the clock pulsewidth of each input clock.
After the switching operation finishes, the unused clock input may be stopped.
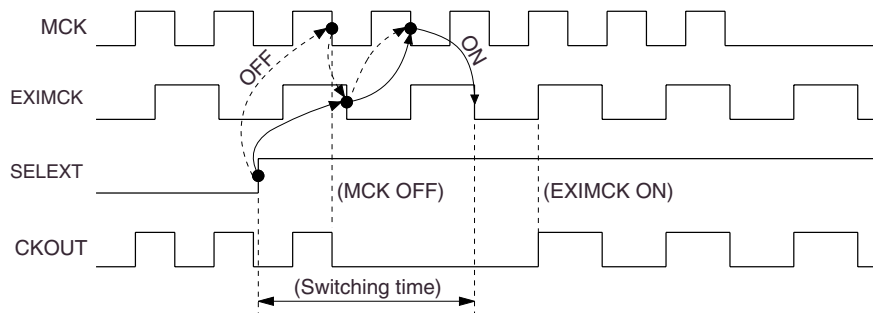
Figure 2. MCK → EXIMCK switching
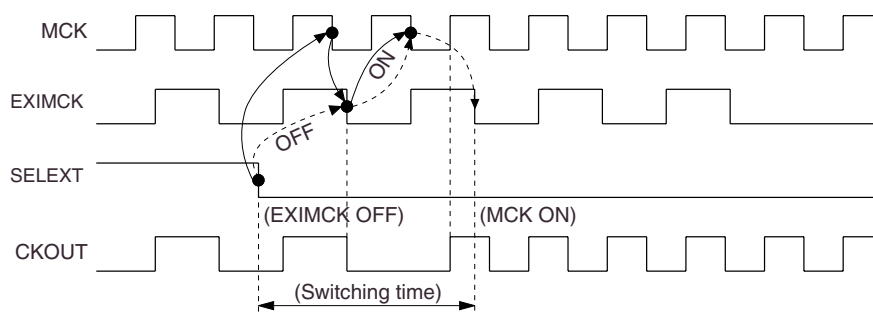
Figure 3. EXIMCK → MCK switching

## Decimation Filter Selection

The decimation filter coefficient set can be selected from 5 sets of fixed coefficients (8fs: 4 sets, 2fs: 1 set) and 1 set of programmable coefficients (8fs or 2fs). The coefficient set is selected using SELRAM and SELFIR1,2.

### Fixed coefficient selection

The fixed coefficients are selected when SELRAM = "L". The filter characteristic is 240th-order for 8fs, and 480th-order for 2fs. When 8fs PCM output is selected, 4 sets of characteristic filter coefficients are available for selection using SELFIR1, 2.

| SELFIR2 | SELFIR1 | Filter characteristic | |
|---------|---------|----------|----------------------|
| L | L | coeff1 | NPC standard filter |
| L | H | coeff2 | 40kHz cutoff filter |
| H | L | coeff3 | 50kHz cutoff filter |
| H | H | coeff4 | 70kHz cutoff filter |

### RAM coefficient selection

A RAM coefficient set is selected when SELRAM = "H".

Initially, the data in RAM is indeterminate, so coefficient data must first be written to the RAM. While data is being written to RAM, the result of any RAM coefficient operation is not guaranteed, hence a fixed coefficient set should be used before switching to RAM coefficients or the PCM outputs should be muted.

The RAM supports 29-bit $\times$ 240 words for combined 8fs and 2fs output. The filter characteristic is 240th-order for 8fs, and 480th-order for 2fs. The filter structure uses an even number order of symmetrical coefficients, reducing by half the number of coefficients to write to RAM. The coefficient data for 8fs and 2fs is in 29-bit 2s complement format.

Details about writing coefficient data are described in "RAM coefficient write mode".

## DSD Gain Switching

The DSD signal 50% level can be set to 0dB, in 8fs/2fs output modes, using DSGAIN.

DSGAIN = "L" : 100% modulation = 0dB (PCM)

DSGAIN = "H" : 50% modulation = 0dB (PCM)   *+ 6dB internal amplification
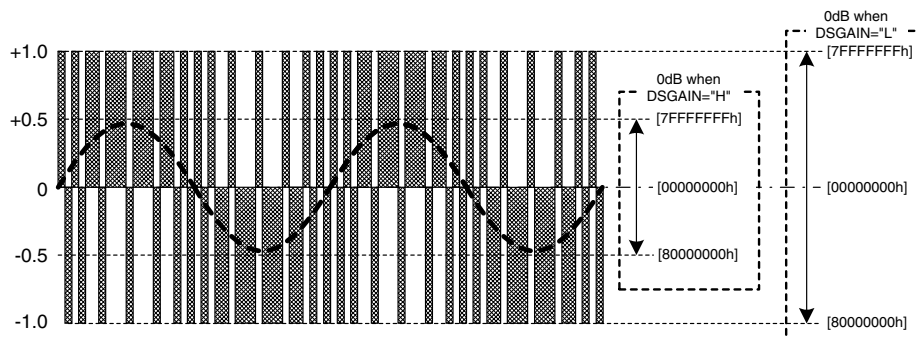


Figure 4. DSD modulation level

Note. With DSGAIN = "H" and 50% DSD modulation or greater, a limiter is needed to prevent output signal clipping.

## Dither Rounding Function

In 8fs PCM output mode with 24-bit right-justified format only, a dither function (TPDF)* can be added to the output. The dither ON/OFF and rounding bit position are set by SELDH1 and SELDH2. After the initial setting is made, rounded data is output 2 words later.

*: Triangular Probability Density Function

| SELDH2 | SELDH1 | Function |
|--------|--------|----------|
| L | L | Dither OFF |
| L | H | Dither ON: 1 LSB (Bit 0) |
| H | L | Dither ON: 2 LSB (Bit 1) |
| H | H | Dither ON: 4 LSB (Bit 2) |

## Mute Function

The DSD outputs and PCM outputs can be muted independently. Muting is applied directly to the outputs.

(1) DSD mute

The DSD outputs are directly muted by a 50% duty (55h) pattern.
XMTDSD = "L" : all DSD outputs with muting ON
XMTDSD = "H" : all DSD outputs with muting OFF

(2) PCM mute

The PCM outputs are directly muted with value "0".
XMTPCM = "L" : all PCM outputs muting ON
XMTPCM = "H" : all PCM outputs muting OFF

## Monitor Function

The internal status changes can be monitored using the monitor pin. The MONTOR pin goes HIGH whenever any of the following parameter conditions occur.

- SEL8FS changes state
- SELEXT changes state
- SELRAM, SELFIR1, 2 changes state

The MONTOR pin is reset to LOW using the INIT or SYNC inputs.

## CPU Interface

### Timing diagrams

The CPU interface comprises 3-wire serial inputs MDATA, MSHIFT, and MLATCH.

■ MDATA bit data is read into an internal interface buffer on the rising edge of MSHIFT.
■ When MLATCH goes LOW, data is latched and processed.

At this point, the data read on the previous MSHIFT rising edge is treated as bit 1, and the most recently input data bits are valid bits.

■ The internal processing mode is determined by the state of bit 1.
  • Bit 1 = "L": system set mode (16 valid bits)
  • Bit 1 = "H": RAM coefficient write mode (40 valid bits)
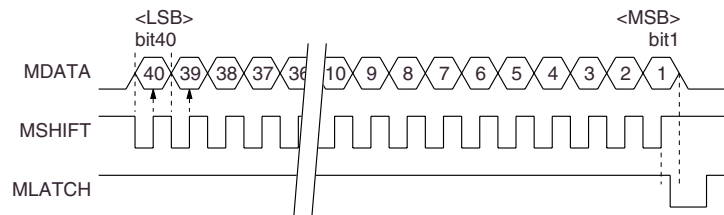


Figure 5. Timing diagram

### System setting mode (bit 1 = "L")

In system set mode, each bit represents a function set flag, with the first 16 bits being valid. Each flag function, when SELMCU is HIGH, performs the same function as the pin with the same name, while the state of those pins is ignored.

Table 1. Flag set function table

| Bit | Flag name | Function | "H" | "L" | Default |
|-----|-----------|----------|-----|-----|---------|
| 1 | MODE | System set mode select | – | Tied "L" | – |
| 2 | SEL8FS | PCM output data select | 8fs PCM output | 2fs PCM output | "L" |
| 3 | SELEXT | 2fs PCM external data output select | External data select | 2fs PCM output | "L" |
| 4 | (Reserved) | (Reserved) | – | Tied "L" | "L" |
| 5 | (Reserved) | (Reserved) | – | Tied "L" | "L" |
| 6 | SELSBSW | Subwoofer output select | Surround back output | Subwoofer output | "L" |
| 7 | SELSBR | Surround back Rch output select | Both Lch, Rch outputs | Lch output only | "L" |
| 8 | SELRAM | Fixed/RAM coefficient select | RAM coefficient | Fixed coefficient | "L" |
| 9 | SELFIR1 | 8fs FIR fixed coefficient 1-4 select | SELFIR (2, 1) / FIR coeff | (L, L) / coeff 1 — (L, H) / coeff 2 — (H, L) / coeff 3 — (H, H) / coeff 4 | "L" |
| 10 | SELFIR2 | | | | "L" |
| 11 | SELDH1 | Dither rounding setting | SELDH (2, 1) / Dither | (L, L) / OFF — (L, H) / 1LSB — (H, L) / 2LSB — (H, H) / 4LSB | "L" |
| 12 | SELDH2 | | | | "L" |
| 13 | DSGAIN | DSD signal gain setting | 50% modulation = 0dB | 100% modulation = 0dB | "L" |
| 14 | MTPCM | PCM signal mute | Mute-OFF | Mute-ON | "L" |
| 15 | MTDSD | DSD signal mute | Mute-OFF | Mute-ON | "L" |
| 16 | SYNC | Forced sync | Resync when "L" → "H" | | "L" |

Note. All 16 bits need to be written even when only changing one portion of the data.

## RAM coefficient write mode (bit 1 = "H")

In RAM coefficient write mode, the bit represent a RAM write address and coefficient write data, with the first 40 bits of data being valid.

Table 2. Flag function table

| Bit | Flag name | Function | Value or state |
|---|---|---|---|
| 1 | MODE | RAM coefficient write mode | Tied "H" |
| 2 | (Reserved) | Reserved flag | Tied "L" |
| 3 | (Reserved) | Reserved flag | Tied "L" |
| 4 | COEF28 | Coefficient data (MSB) | |
| 5 | COEF27 | Coefficient data | |
| 6 | COEF26 | Coefficient data | |
| 7 | COEF25 | Coefficient data | |
| 8 | COEF24 | Coefficient data | |
| 9 | COEF23 | Coefficient data | |
| 10 | COEF22 | Coefficient data | |
| 11 | COEF21 | Coefficient data | |
| 12 | COEF20 | Coefficient data | |
| 13 | COEF19 | Coefficient data | |
| 14 | COEF18 | Coefficient data | |
| 15 | COEF17 | Coefficient data | |
| 16 | COEF16 | Coefficient data | Coefficient data must conform with the following conditions. |
| 17 | COEF15 | Coefficient data | * Coefficient word length = 29 bits ($\pm$ 1.0) |
| 18 | COEF14 | Coefficient data | * Coefficient sum total not to exceed 0.5 |
| 19 | COEF13 | Coefficient data | (18000000)h to (07FFFFFF)h |
| 20 | COEF12 | Coefficient data | * Depending on the coefficient, the result may pass the overflow limit. |
| 21 | COEF11 | Coefficient data | * RAM initial state is indeterminate, thus address-field data must be written before use. |
| 22 | COEF10 | Coefficient data | |
| 23 | COEF9 | Coefficient data | |
| 24 | COEF8 | Coefficient data | |
| 25 | COEF7 | Coefficient data | |
| 26 | COEF6 | Coefficient data | |
| 27 | COEF5 | Coefficient data | |
| 28 | COEF4 | Coefficient data | |
| 29 | COEF3 | Coefficient data | |
| 30 | COEF2 | Coefficient data | |
| 31 | COEF1 | Coefficient data | |
| 32 | COEF0 | Coefficient data (LSB) | |
| 33 | RA7 | RAM write address (MSB) | |
| 34 | RA6 | RAM write address | Coefficient address should be assigned as follows. |
| 35 | RA5 | RAM write address | * Even-order symmetrical coefficients restriction means that only half need be written from the edges to the center. |
| 36 | RA4 | RAM write address | * For 2fs, half 480th-order implies to address 240. |
| 37 | RA3 | RAM write address | RA = (00)h is the edge, RA = (EF)h is the center. |
| 38 | RA2 | RAM write address | * For 8fs, half 240th-order implies to address 120. |
| 39 | RA1 | RAM write address | RA = (00)h, the edge, to RA = (3B)h are the first 60 addresses |
| 40 | RA0 | RAM write address (LSB) | RA = (80)h to RA = (BB)h are the last 60 addresses. |

Note. Writing RAM coefficients always takes precedence. As a result, coefficient writing while a RAM coefficient is selected, will mean the coefficients are read incorrectly, generating an output noise. To prevent this problem, the outputs should be muted when writing RAM coefficients or a ROM coefficient should be temporarily selected.
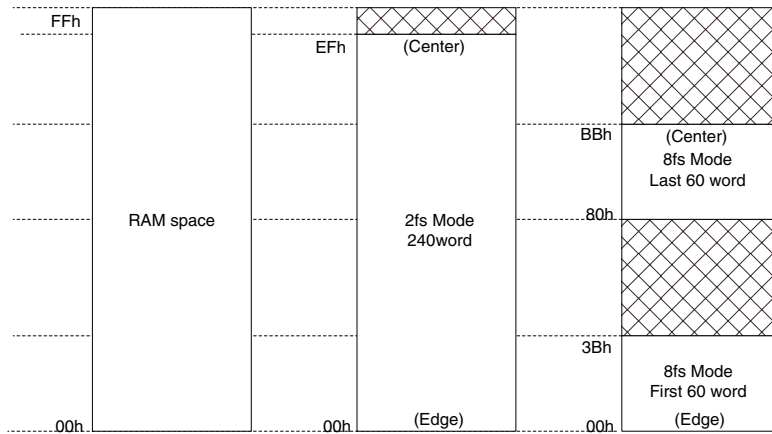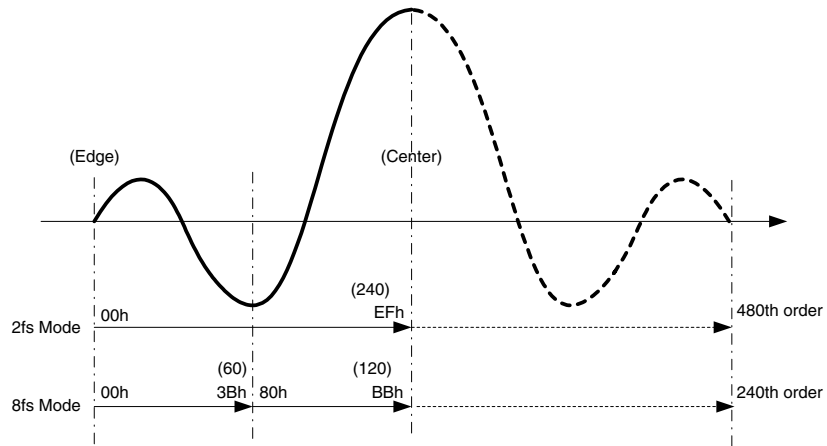
Figure 6. Usable address space diagram



Figure 7. Filter coefficient example of RAM address (RA) assignment

Note that in 8fs mode, the usable address area is separated into 2 portions.

## Pin-control/Flag-control Relation Table

| System setting Description | | | Pin control | | Serial I/F control | | |
|---|---|---|---|---|---|---|---|
| **Function** | **"H"** | **"L"** | **Pin name** | **No.** | **Flag name** | **Bit** | **Default** |
| Control method select | Serial I/F control | Pin control | SELMCU | 8 | – | – | – |
| Initialization control | Normal operation | Initialize and resync | INIT | 79 | – | – | – |
| DSD data input clock (DSBCKF) I/O select | Output (Master) | Input (Slave) | DIRDSCK1 | 69 | – | – | – |
| DSD data output clock (DSBCKB) I/O select | Input (Slave) | Output (Master) | DIRDSCK2 | 70 | – | – | – |
| 8fs data output clock (F8BCK, F8WCK) I/O select | Input (Slave) | Output (Master) | DIR8CK | 22 | – | – | – |
| 2fs data output clock (F2BCK, F2LRCK) I/O select | Input (Slave)[1] | Output (Master) | DIR2CK | 39 | – | – | – |
| 8fs PCM data format select | MSB-first right-justified 24-bit | MSB-first left-justified 32-bit | FMT8FS | 23 | – | – | – |
| 8fs PCM word clock format select | "L" → "H" (falling edge word boundary) | "H" → "L" (rising edge word boundary) | FMT8WCK | 24 | – | – | – |
| 2fs PCM data format select | IIS 32bit | MSB-first left-justified 32-bit | FMT2FS | 42 | – | – | – |
| PCM output data select | 8fs PCM output | 2fs PCM output | SEL8FS | 76 | SEL8FS | 2 | "L" |
| 2fs PCM external data output select | External data select | 2fs PCM output | SELEXT | 77 | SELEXT | 3 | "L" |
| Subwoofer output select | Surround Back output | Subwoofer output | SELSBSW | 6 | SELSBSW | 6 | "L" |
| Surround Back Rch output select | Both Rch, Lch select | Lch output only | SELSBR | 7 | SELSBR | 7 | "L" |
| Fixed/RAM coefficient select | RAM coefficient | Fixed coefficient | SELRAM | 71 | SELRAM | 8 | "L" |
| 8fs FIR fixed coefficient 1-4 select | SELFIR (2, 1) / (L, L) / (L, H) / (H, L) / (H, H) — FIR coeff / coeff 1 / coeff 2 / coeff 3 / coeff 4 | | SELFIR1 | 72 | SELFIR1 | 9 | "L" |
| | | | SELFIR2 | 73 | SELFIR2 | 10 | "L" |
| Dither rounding setting | SELDH (2, 1) / (L, L) / (L, H) / (H, L) / (H, H) — Dither / OFF / 1LSB / 2LSB / 4LSB | | SELDH1 | 38 | SELDH1 | 11 | "L" |
| | | | SELDH2 | 37 | SELDH2 | 12 | "L" |
| DSD signal gain setting | 50% modulation = 0dB | 100% modulation = 0dB | DSGAIN | 5 | DSGAIN | 13 | "L" |
| PCM signal mute | Mute-OFF | Mute-ON | XMTPCM | 74 | MTPCM | 14 | "L" |
| DSD signal mute | Mute-OFF | Mute-ON | XMTDSD | 75 | MTDSD | 15 | "L" |
| Forced sync | Resync when "L" → "H" | | SYNC | 78 | SYNC | 16 | "L" |

1. In 2fs PCM mode, when external inputs are selected for output(SELEXT="H"), the DIR2CK setting is inactive, and F2BCK, F2LRCK are output.

## Initialization Operation

When power is applied, the INIT pin must be held LOW for the rated time to initialize the device. Initialization sets all the CPU interface system control registers to their default values, and the outputs have the states as described below.

| Pin | State |
|---|---|
| DSD data outputs | All "L" |
| 8fs PCM data outputs | All "L" |
| 2fs PCM data outputs | In internal 2fs output mode, all "L"<br>In external data output mode, output as-is in through mode |
| DSBCKF, DSBCKB | When both output modes are set, "H"<br>When one input mode is set, through mode output |
| F8BCK | In output mode, "H" |
| F8WCK | In output mode using FMT8WCK = "L", "L"<br>In output mode using FMT8WCK = "H", "H" |
| F2BCK | In internal data output mode, "H"<br>In external data output mode, external bit clock is output in through mode |
| F2LRCK | In left-justified 32-bit output mode, "L"<br>In IIS output mode, "H"<br>In external data output mode, external word clock is output in through mode |
| CKOUT | MCK or EXIMCK, whichever is selected, is output in through mode |
| MONTOR | Cleared to "L" |

When INIT goes "H", the sync adjustment operation described in section "Input clock sync operation and resynchronization" starts. Also, if DSD or PCM output is muted, the mute condition continues as-is until released.

## BUILT-IN FILTER CHARACTERISTICS

### 64fs → 2fs Mode
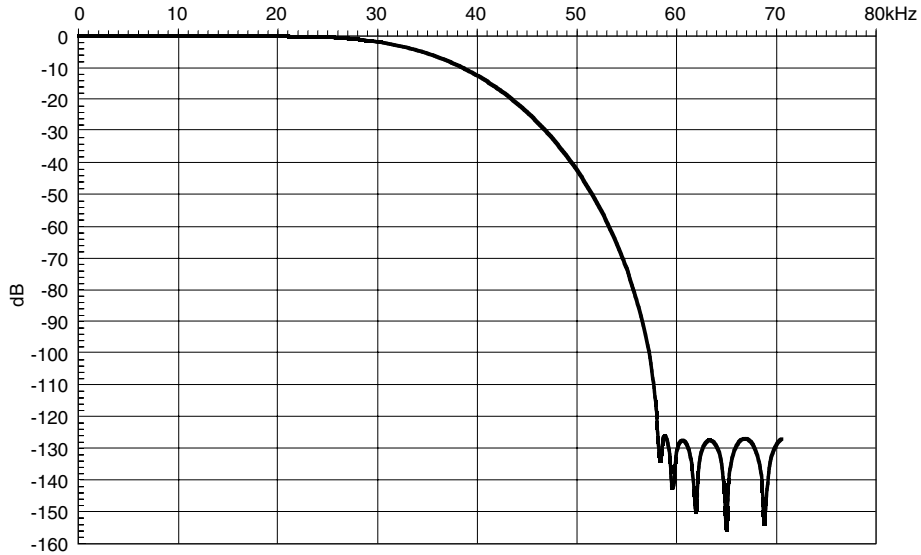


### 64fs → 8fs Mode
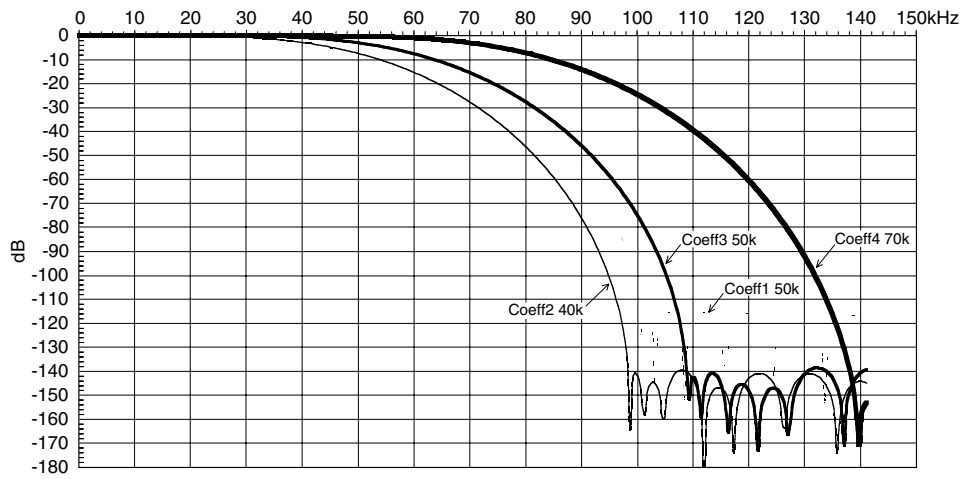


Note. These characteristics were obtained by simulation.

# TYPICAL APPLICATION CIRCUITS

## Surround Processor

2fs-32bit/IIS

| Multi-channel SA-CD Decoder CXD2752R | → | DSD-PCM converter **SM5816** | → | DSP (Surround Processing etc.) | → | DAC | → | Analog LPF | → | ∿ |
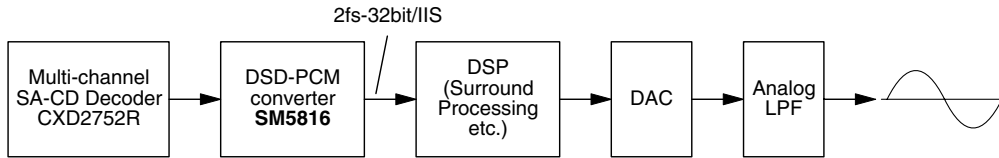
## DSD-to-PCM Conversion Reproduction

8fs-24bit/32bit

| Multi-channel SA-CD Decoder CXD2752R | → | DSD-PCM converter **SM5816** | → | 8fs Processing (Volume etc.) | → | DAC | → | Analog LPF | → | ∿ |