TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91CY22IFG

TOSHIBA CORPORATION

Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

CAUTION

How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to 4, INTRTC) which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 5 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2 is not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

CMOS 16-Bit Microcontrollers

TMP91CY22IFG

1. Outline and Features

TMP91CY22I is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91CY22I comes in a 100-pin flat package.

Listed below are the features.

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction mnemonics are upward-compatible with TLCS-90/900
- 16 Mbytes of linear address space
- General-purpose registers and register banks
- 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
- Micro DMA: 4-channels (593 ns/2 bytes at 27 MHz)

(2) Minimum instruction execution time: 148 ns (at 27 MHz)

(3) Built-in RAM: 16 Kbytes
Built-in ROM: 256 Kbytes

(4) External memory expansion
- Expandable up to 16 Mbytes (shared program/data area)
- Can simultaneously support 8-/16-bit width external data bus
  ··· Dynamic data bus sizing

(5) 8-bit timers: 8 channels

(6) 16-bit timer/event counter: 2 channels

(7) General-purpose serial interface: 2 channels
UART/ Synchronous mode: 2 channels
IrDA ver1.0 (115.2 kbps) supported

(8) Serial bus interface: 1 channel
- I^2C bus mode/clock synchronous Select mode

(9) 10-bit AD converter: 8 channels

(10) Watchdog timer

(11) Special timer for CLOCK

(12) Chip Select/Wait controller: 4 channels

(13) Interrupts: 45 interrupts
- 9 CPU interrupts: Software interrupt instruction and illegal instruction
- 26 internal interrupts: ┐
- 10 external interrupts: ┘ Seven selectable priority levels

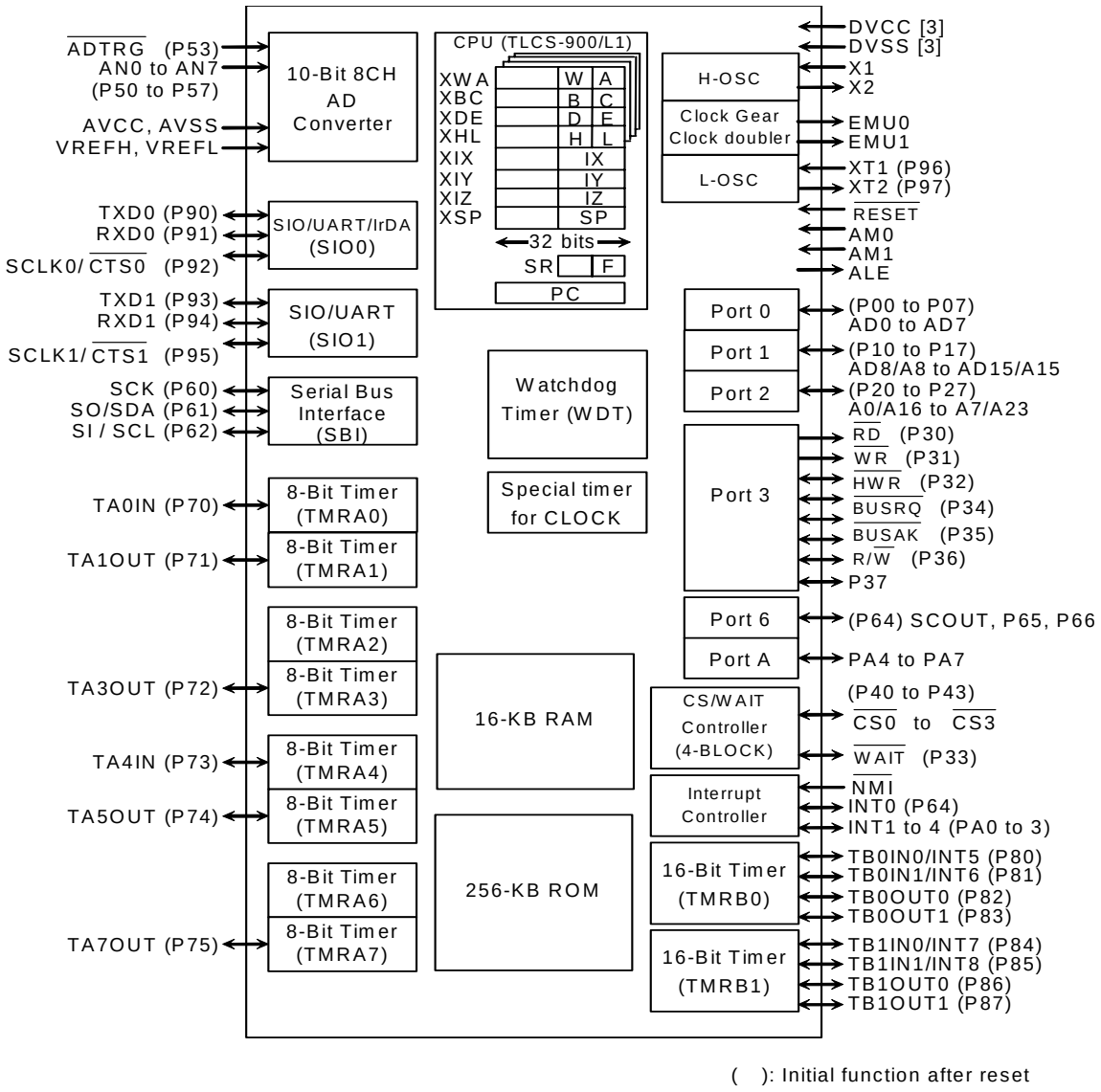
(14) Input/Output ports: 81 pins

(15) Standby function
Three HALT modes: IDLE2 (programmable), IDLE1, STOP

(16) Triple-clock controller
- Clock Doubler (DFM)
- Clock Gear (fc to fc/16)
- SLOW mode (fs = 32.768 kHz)

(17) Operating voltage
- V_{CC} = 2.7 V to 3.6 V (fc max = 27 MHz)
- V_{CC} = 1.8 V to 3.6 V (fc max = 10 MHz)

(18) Package
- 100-pin QFP: P-LQFP100-1414-0.50F



( ): Initial function after reset

Figure 1.1 TMP91CY22I Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91CY22I, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91CY22I.

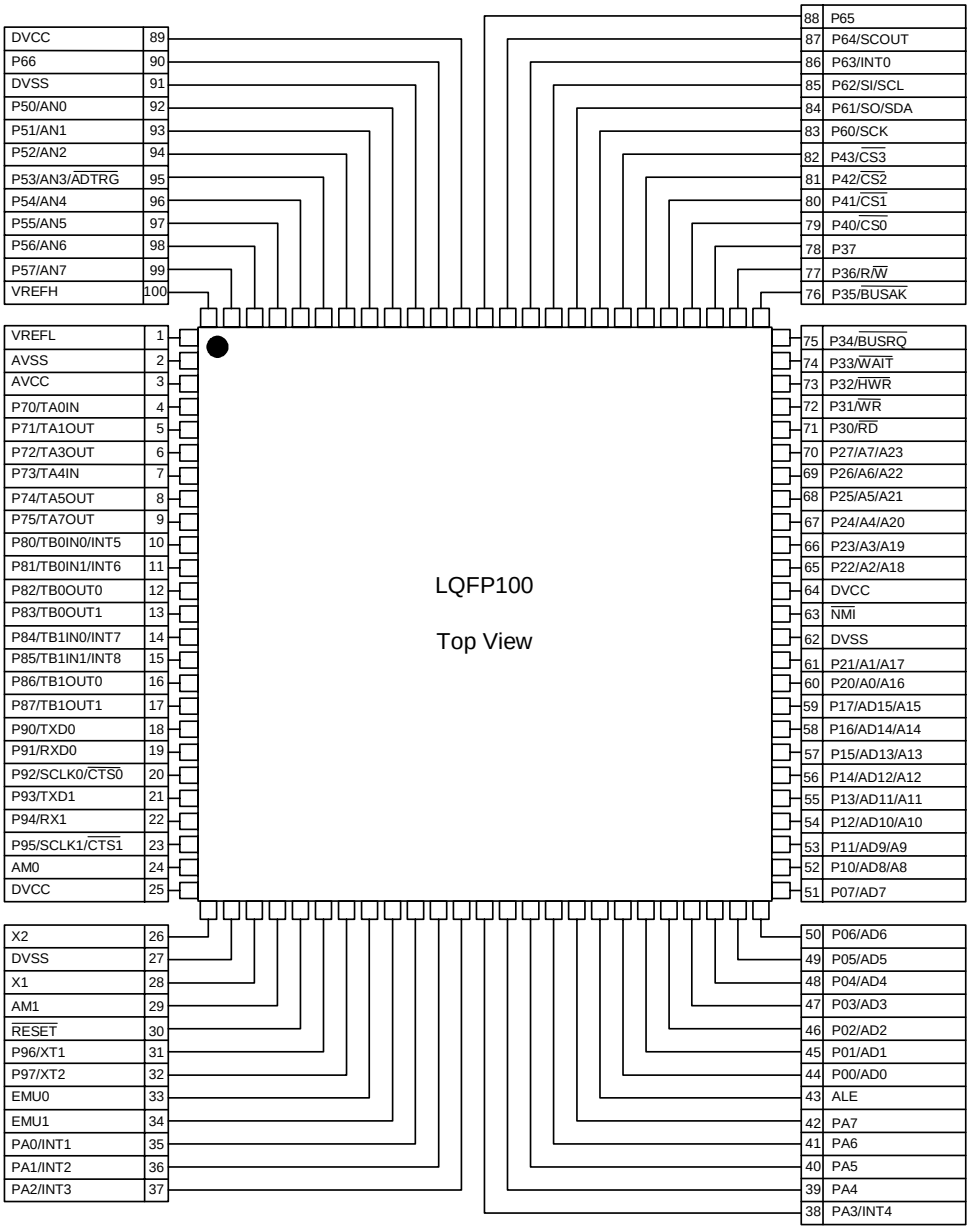


Figure 2.1.1 Pin assignment diagram (100-pin LQFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.
Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin names and functions (1/4)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 of address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory RD is outputted by setting P3 <P30> = 0 and P3FC < P30F> = 1, when reading internal area.
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data to pins AD0 to AD7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins AD8 to AD15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait ((1 + N) wait mode)
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request that set AD0~15, A0~23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$ ~ $\overline{CS3}$ pins to High impedance. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge that AD0~15, A0~23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{CS0}$ ~ $\overline{CS3}$ pins are set to High impedance by receiving $\overline{BUSRQ}$. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37	1	I/O	Port 37: I/O port (with pull-up resistor)
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 if address is within specified address area
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip Select 2: Outputs 0 if address is within specified address area
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip Select 3: Outputs 0 if address is within specified address area

Table 2.2.1 Pin names and functions (2/4)

Pin Name	Number of Pins	I/O	Functions
P50 to P57	8	Input	Port 5: Pin used to input port
AN0 to AN7		Input	Analog input: Pin used to input to AD converter
$\overline{\text{ADTRG}}$		Input	AD Trigger: Signal used to request start of AD converter (Shared with P53)
P60	1	I/O	Port 60: I/O port
SCK		I/O	Serial bus interface clock in SIO Mode
P61	1	I/O	Port 61: I/O port
SO		Output	Serial bus interface output data in SIO Mode
SDA		I/O	Serial bus interface data in I^2C bus Mode. (programmable open-drain)
P62	1	I/O	Port 62: I/O port
SI		Input	Serial bus interface input data in SIO Mode
SCL		I/O	Serial bus interface clock in I^2C bus Mode. (programmable open-drain)
P63	1	I/O	Port 63: I/O port
INT0		Input	Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64	1	I/O	Port 64: I/O port
SCOUT		Output	System Clock Output: Outputs f_{FPH} or fs clock.
P65	1	I/O	Port 65: I/O port
P66	1	I/O	Port 66: I/O port
P70	1	I/O	Port 70: I/O port
TA0IN		Input	8-bit timer 0 input: Timer A0 Input
P71	1	I/O	Port 71: I/O port
TA1OUT		Output	8-bit timer 1 output:Timer A1 Output
P72	1	I/O	Port 72: I/O port
TA3OUT		Output	8-bit timer 3 output: Timer A3 Output
P73	1	I/O	Port 73: I/O port
TA4IN		Input	8-bit timer 4 input:Timer A4 Input
P74	1	I/O	Port 74: I/O port
TA5OUT		Output	8-bit timer 5 output:Timer A5 Output
P75	1	I/O	Port 75: I/O port
TA7OUT		Output	8-bit timer 7 output:Timer A7 Output
P80	1	I/O	Port 80: I/O port
TB0IN0		Input	16-bit timer 0 input0:Timer B0 count/capture trigger Input 0
INT5		Input	Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge.
P81	1	I/O	Port 81: I/O port
TB0IN1		Input	16-bit timer 0 input1: Timer B0 count/capture trigger Input 1
INT6		Input	Interrupt Request Pin 6: Interrupt request on rising edge
P82	1	I/O	Port 82: I/O port
TB0OUT0		Output	16-bit timer 0 output 0: Timer B0 Output 0
P83	1	I/O	Port 83: I/O port
TB0OUT1		Output	16-bit timer 0 output 1: Timer B0 Output 1
P84	1	I/O	Port 84: I/O port
TB1IN0		Input	16-bit timer 1 input0: Timer B1 count/capture trigger Input 0
INT7		Input	Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge.
P85	1	I/O	Port 85: I/O port
TB1IN1		Input	16-bit timer 1 input 1: Timer B1 count/capture trigger Input 1
INT8		Input	Interrupt Request Pin 8: Interrupt request on rising edge
P86	1	I/O	Port 86: I/O port
TB1OUT0		Output	16-bit timer 1 output 0: Timer B1 Output 0
P87	1	I/O	Port 87: I/O port
TB1OUT1		Output	16-bit timer 1 output 1: Timer B1 Output 1

Table 2.2.1 Pin names and functions (3/4)

Pin Name	Number of Pins	I/O	Functions
P90	1	I/O	Port 90: I/O port
TXD0		Output	Serial Send Data 0 (programmable open-drain)
P91	1	I/O	Port 91: I/O port
RXD0		Input	Serial Receive Data 0
P92	1	I/O	Port 92: I/O port
SCLK0		I/O	Serial Clock I/O 0
$\overline{CTS0}$		Input	Serial Data Send Enable 0 (Clear to Send)
P93	1	I/O	Port 93: I/O port
TXD1		Output	Serial Send Data 1 (programmable open-drain)
P94	1	I/O	Port 94: I/O port
RXD1		Input	Serial Receive Data 1
P95	1	I/O	Port 95: I/O port
SCLK1		I/O	Serial Clock I/O 1
$\overline{CTS1}$		Input	Serial Data Send Enable 1 (Clear to Send)
P96	1	I/O	Port 96: I/O port (open-drain output)
XT1		Input	Low-frequency oscillator connection pin

Table 2.2.1 Pin names and functions (4/4)

Pin Name	Number of Pins	I/O	Functions
P97 XT2	1	I/O Output	Port 97: I/O port (open-drain output) Low-frequency oscillator connection pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Ports A0 to A3: I/O ports Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge.
PA4 to PA7	4	I/O	Ports A4 to A7: I/O ports
ALE	1	Output	Address Latch Enable (Can be disabled to reduce noise.)
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge.
AM0 to AM1	2	Input	Operation mode: Fixed to AM1 = "1", AM0 = "1".
EMU0/EMU1	1	Output	Set to Open pins
$\overline{\text{RESET}}$	1	Input	Reset: initializes TMP91CY22. (with pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1		Power supply pin for AD converter
AVSS	1		Power GND pin for AD converter (0 V)
X1/X2	2	I/O	High frequency oscillator connection pins
DVCC	3		Power supply pins (All DVCC pins should be connected with the power supply pin.)
DVSS	3		GND pins (0 V) (All DVSS pins should be connected with the GND (0V) pin.)

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

3. Operation

This device is a version of expanding its internal mask ROM size to 256 Kbytes and RAM size to 16 Kbytes. The configuration and the functionality of this device are the same as those of the TMP91CW12A. For the functions of this device that are not described here, refer to the TMP91CW12A data sheet.

3.1 Memory Map

Figure 3.1.1 is a memory map of the TMP91CY22I.

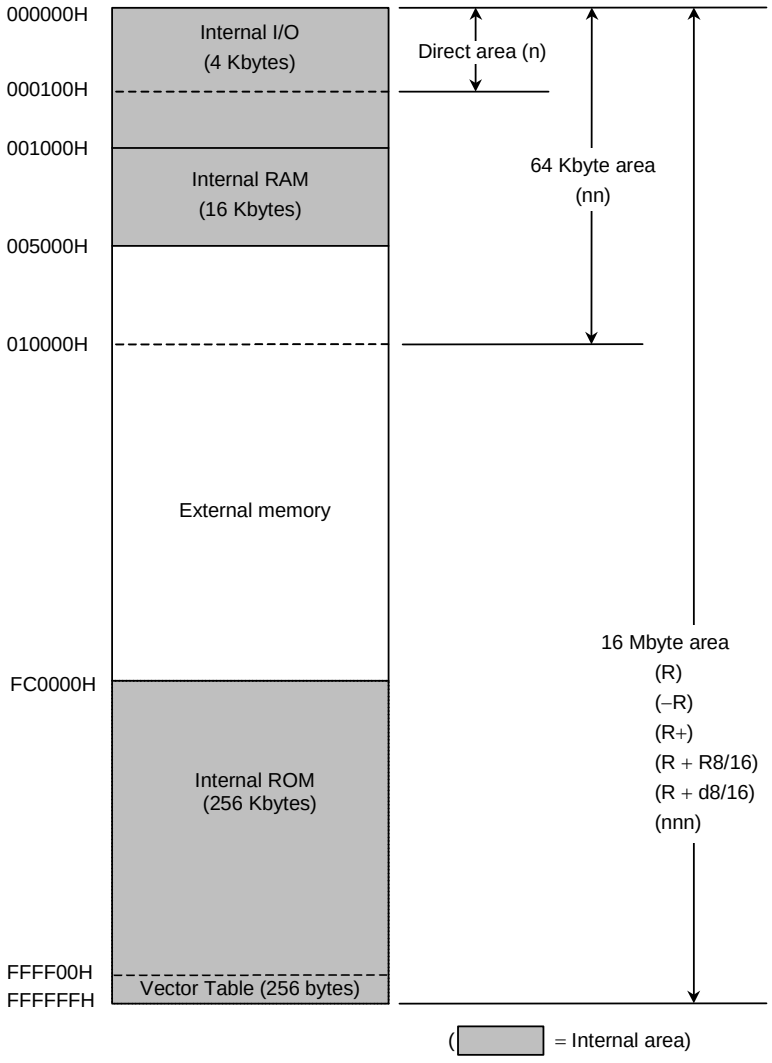


Figure 3.1.1 Memory Map

4. Electrical Characteristics

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	Vcc	−0.5 to 4.0	V
Input Voltage	VIN	−0.5 to Vcc + 0.5	V
Output Current	IOL	2	mA
Output Current	IOH	−2	mA
Output Current (total)	ΣIOL	80	mA
Output Current (total)	ΣIOH	−80	mA
Power Dissipation (Ta = 85°C)	PD	600	mW
Soldering Temperature (10 s)	TSOLDER	260	°C
Storage Temperature	TSTG	−65 to 150	°C
Operating Temperature	TOPR	−40 to 85	°C

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

Point of note about solderability of lead free products (attach “G” to package name)

Test parameter	Test condition	Note
Solderability	(1) Use of Sn-63Pb solder Bath Solder bath temperature =230°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux	Pass: solderability rate until forming ≥ 95%
	(2) Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature =245°C, Dipping time = 5 seconds The number of times = one, Use of R-type flux (use of lead free)	

4.2 DC Characteristics (1/2)

Parameter		Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power Supply Voltage (AVcc = DVcc) (AVss = DVss = 0 V)		VCC	fc = 4 to 27 MHz	fs = 30 to 34 kHz	2.7		3.6	V
			fc = 2 to 10 MHz		1.8			
Input Low Voltage	P00 to P17 (AD0 to 15)	V_{IL}	Vcc ≥ 2.7 V		−0.3		0.6	V
			Vcc < 2.7 V				0.2Vcc	
	P20 to PA7 (except P63)	V_{IL1}	Vcc ≥ 2.7 V				0.3Vcc	
			Vcc < 2.7 V				0.2Vcc	
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IL2}	Vcc ≥ 2.7 V				0.25Vcc	
			Vcc < 2.7 V				0.15Vcc	
	AM0, 1	V_{IL3}	Vcc ≥ 2.7 V				0.3	
			Vcc < 2.7 V				0.3	
	X1	V_{IL4}	Vcc ≥ 2.7 V				0.2Vcc	
			Vcc < 2.7 V				0.1Vcc	
Input High Voltage	P00 to P17 (AD0 to AD15)	V_{IH}	Vcc ≥ 2.7 V		2.0		Vcc + 0.3	
			Vcc < 2.7 V		0.7Vcc			
	P20 to PA7 (except P63)	V_{IH1}	Vcc ≥ 2.7 V		0.7Vcc			
			Vcc < 2.7 V		0.8Vcc			
	$\overline{RESET}$, $\overline{NMI}$, P63 (INT0)	V_{IH2}	Vcc ≥ 2.7 V		0.75Vcc			
			Vcc < 2.7 V		0.85Vcc			
	AM0, 1	V_{IH3}	Vcc ≥ 2.7 V		Vcc − 0.3			
			Vcc < 2.7 V		Vcc − 0.3			
	X1	V_{IH4}	Vcc ≥ 2.7 V		0.8Vcc			
			Vcc < 2.7 V		0.9Vcc			
Output Low Voltage		V_{OL}	IOL = 1.6 mA	Vcc ≥ 2.7 V			0.45	V
			IOL = 0.4 mA	Vcc < 2.7 V			0.15Vcc	
Output High Voltage		V_{OH}	IOH = −400 μA	Vcc ≥ 2.7 V	2.4			
			IOH = −200μA	Vcc < 2.7 V	0.8Vcc			

Note: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Input Leakage Current	ILI	$0.0 \leq V_{IN} \leq Vcc$		0.02	±5	μA
Output Leakage Current	ILO	$0.2 \leq V_{IN} \leq Vcc - 0.2$		0.05	±10	
Power Down Voltage (at STOP, RAM back-up)	VSTOP	V IL2 = 0.2 Vcc, V IH2 = 0.8 Vcc	1.8		3.6	V
$\overline{RESET}$ Pull-up Resistor	RRST	Vcc = 3 V ± 10%	100		400	kΩ
		Vcc = 2 V ± 10%	200		1000	
Pin Capacitance	CIO	fc = 1 MHz			10	pF
Schmitt Width $\overline{RESET}$, $\overline{NMI}$, INT0	VTH	Vcc ≥ 2.7 V	0.4	1.0		V
		Vcc < 2.7 V	0.3	0.8		
Programmable Pull-up Resistor	RKH	Vcc = 3 V ± 10%	100		400	kΩ
		Vcc = 2 V ± 10%	200		1000	
NORMAL (Note 2)	Icc	Vcc = 3 V ± 10% fc = 27 MHz		10.0	13.0	mA
IDLE2				2.5	3.5	
IDLE1				1.0	1.8	
NORMAL (Note 2)		Vcc = 2 V ± 10 % fc = 10 MHz (Typ.: Vcc = 2.0 V)		1.7	2.5	mA
IDLE2				0.6	0.9	
IDLE1				0.25	0.4	
SLOW (Note 2)		Vcc = 3 V ± 10 % fs = 32.768 kHz		11.6	30	μA
IDLE2				5.2	19	
IDLE1		Ta ≤ 70°C		3.0	8	
		Ta ≤ 85°C			15	
SLOW (Note 2)		Vcc = 2 V ± 10 % fs = 32.768 KHz (Typ.: Vcc = 2.0 V)		7.7	20	μA
IDLE2				3.5	13	
IDLE1				2.0	10	
STOP		Vcc = 1.8 to 3.3V		0.1	10	μA

Note 1: Typical values are for when Ta = 25°C and Vcc = 3.0 V unless otherwise noted.

Note 2: Icc measurement conditions (NORMAL, SLOW):
All functions are operating; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) Vcc = 3.0 V ± 10%

No.	Parameter	Symbol	Variable		f_{FPH} = 27 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} Period (= x)	t_{FPH}	37.0	31250	37.0		ns
2	A0 to A15 Vaild → ALE Fall	t_{AL}	0.5x – 14		4		ns
3	ALE Fall → A0 to A15 Hold	t_{LA}	0.5x – 16		2		ns
4	ALE High Width	t_{LL}	x – 20		17		ns
5	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 14		4		ns
6	$\overline{RD}$ Rise → ALE Rise	t_{CLR}	0.5x – 10		8		ns
7	$\overline{WR}$ Rise → ALE Rise	t_{CLW}	x – 10		27		ns
8	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 23		14		ns
9	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACH}	1.5x – 26		29		ns
10	$\overline{RD}$ Rise → A0 to A23 Hold	t_{CAR}	0.5x – 13		5		ns
11	$\overline{WR}$ Rise → A0 to A23 Hold	t_{CAW}	x – 13		24		ns
12	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		3.0x – 38		73	ns
13	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		3.5x – 41		88	ns
14	$\overline{RD}$ Fall → D0 to D15 Input	t_{RD}		2.0x – 30		44	ns
15	$\overline{RD}$ Low Width	t_{RR}	2.0x – 15		59		ns
16	$\overline{RD}$ Rise → D0 to A15 Hold	t_{HR}	0		0		ns
17	$\overline{RD}$ Rise → A0 to A15 Output	t_{RAE}	x – 15		22		ns
18	$\overline{WR}$ Low Width	t_{WW}	1.5x – 15		40		ns
19	D0 to D15 Valid → $\overline{WR}$ Rise	t_{DW}	1.5x – 35		20		ns
20	$\overline{WR}$ Rise → D0 to D15 Hold	t_{WD}	x – 25		12		ns
21	A0 to A23 Valid → $\overline{WAIT}$ Input (1+n wait Mode)	t_{AWH}		3.5x – 60		69	ns
22	A0 to A15 Valid → $\overline{WAIT}$ Input (1+n wait Mode)	t_{AWL}		3.0x – 50		61	ns
23	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold (1+n wait Mode)	t_{CW}	2.0x + 0		74		ns
24	A0 to A23 Valid → Port Input	t_{APH}		3.5x – 89		40	ns
25	A0 to A23 Valid → Port Hold	t_{APH2}	3.5x		129		ns
26	A0 to A23 Valid → Port Valid	t_{AP}		3.5x + 80		209	ns

AC Measuring Conditions

- Output Level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input Level: High = 0.9 Vcc, Low = 0.1 Vcc

Note: "x" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>.
The value of "x" changes according to whether a clock gear or a low-speed oscillator is selected.
An example value is calculated for fc, with gear=1/fc (SYSCR1<SYSCK,GEAR2 to 0> = 0000).

(2) Vcc = 2.0 V ± 10%

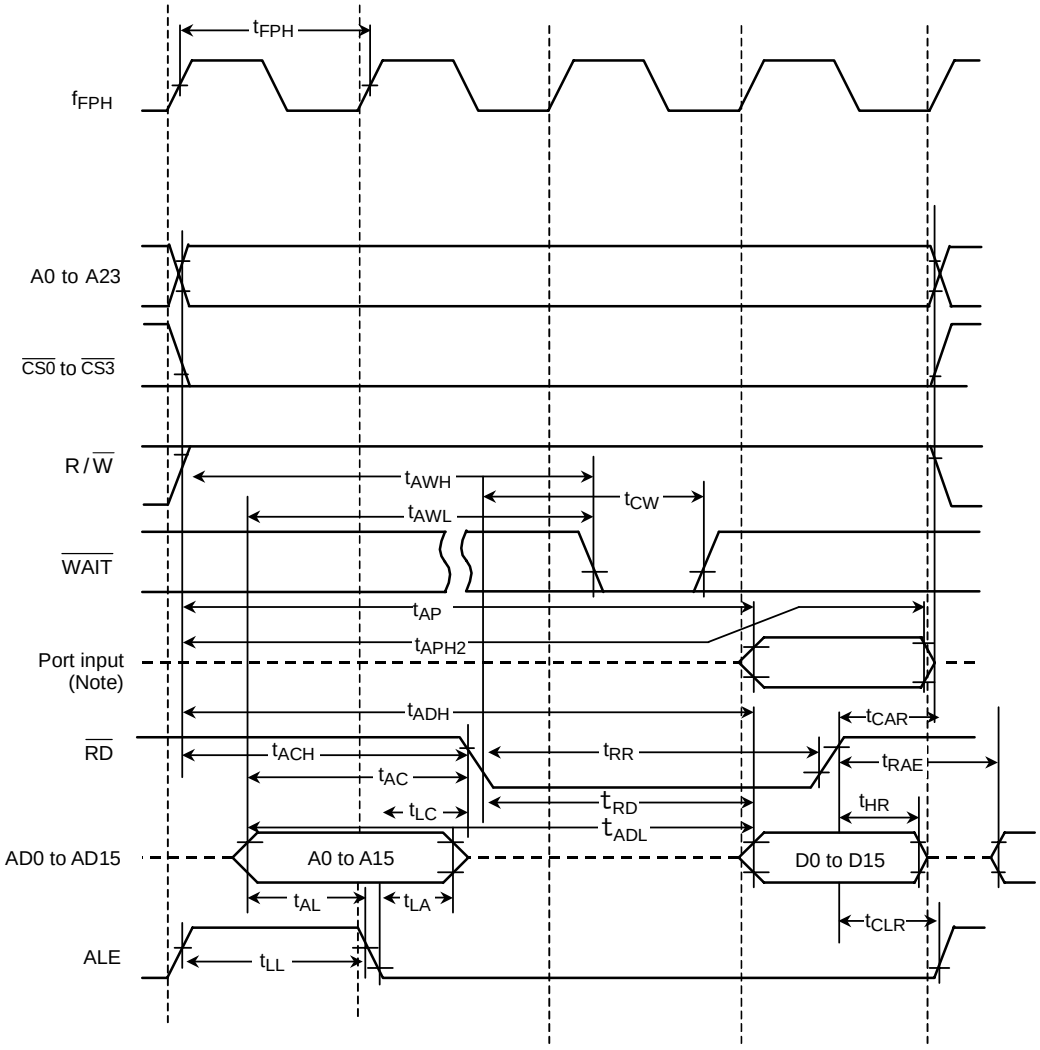
No.	Parameter	Symbol	Variable		f_{FPH} =10M Hz		Unit
			Min	Max	Min	Max	
1	f_{FPH} Period (= x)	t_{FPH}	100	31250	100		ns
2	A0 to A15 → ALE Fall	t_{AL}	0.5 x – 28		22		ns
3	ALE Fall → A0 to A15 Hold	t_{LA}	0.5 x – 35		15		ns
4	ALE High Width	t_{LL}	x – 40		60		ns
5	ALE Fall → $\overline{RD}$ / $\overline{WR}$ Fall	t_{LC}	0.5x – 28		22		ns
6	$\overline{RD}$ Rise → ALE Rise	t_{CLR}	0.5x – 20		30		ns
7	$\overline{WR}$ Rise → ALE Rise	t_{ACW}	x – 20		80		ns
8	A0 to A15 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	t_{ACL}	x – 75		25		ns
9	A0 to A23 Valid → $\overline{RD}$ / $\overline{WR}$ Fall	T_{ACH}	1.5x –70		80		ns
10	$\overline{RD}$ Rise → A0 to A23 Hold	t_{CAR}	0.5x – 30		20		ns
11	$\overline{WR}$ Rise → A0 to A23 Hold	T_{CAW}	x – 30		70		ns
12	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		3.0x – 76		224	ns
13	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		3.5x – 82		268	ns
14	$\overline{RD}$ Fall → D0 to D15 Input	T_{RD}		2.0x – 60		140	ns
15	$\overline{RD}$ Low Width	t_{RR}	2.0x – 30		170		ns
16	$\overline{RD}$ Rise → D0 to D15 Hold	t_{HR}	0		0		ns
17	$\overline{RD}$ Rise → A0 to A15 Output	t_{RAE}	x – 30		70		ns
18	$\overline{WR}$ Low Width	t_{WW}	1.5 x – 30		120		ns
19	D0 to D15 Valid → $\overline{WR}$ Rise	t_{DW}	1.5 x – 70		80		ns
20	$\overline{WR}$ Rise →D0 to D15 Hold	t_{WD}	x – 50		50		ns
21	A0 to A23 Valid → $\overline{WAIT}$ Input $\left[\begin{smallmatrix}1+n\\ \text{wait mode}\end{smallmatrix}\right]$	t_{AWH}		3.5x – 120		230	ns
22	A0 to A15 Valid → $\overline{WAIT}$ Input $\left[\begin{smallmatrix}1+n\\ \text{wait mode}\end{smallmatrix}\right]$	t_{AWL}		3.0x – 100		200	ns
23	$\overline{RD}$ / $\overline{WR}$ Fall → $\overline{WAIT}$ Hold $\left[\begin{smallmatrix}1+n\\ \text{wait mode}\end{smallmatrix}\right]$	t_{CW}	2.0x + 0		200		ns
24	A0 to A23 Valid → Port Input	t_{APH}		3.5x – 170		180	ns
25	A0 to A23 Valid → Port Hold	t_{APH2}	3.5x		350		ns
26	A0 to A23 Valid → Port Valid	t_{AP}		3.5x + 170		520	ns

AC Measuring Conditions

- Output Level: High = 0.7 Vcc, Low = 0.3 Vcc, CL = 50 pF
- Input Level: High = 0.9 Vcc, Low = 0.1 Vcc

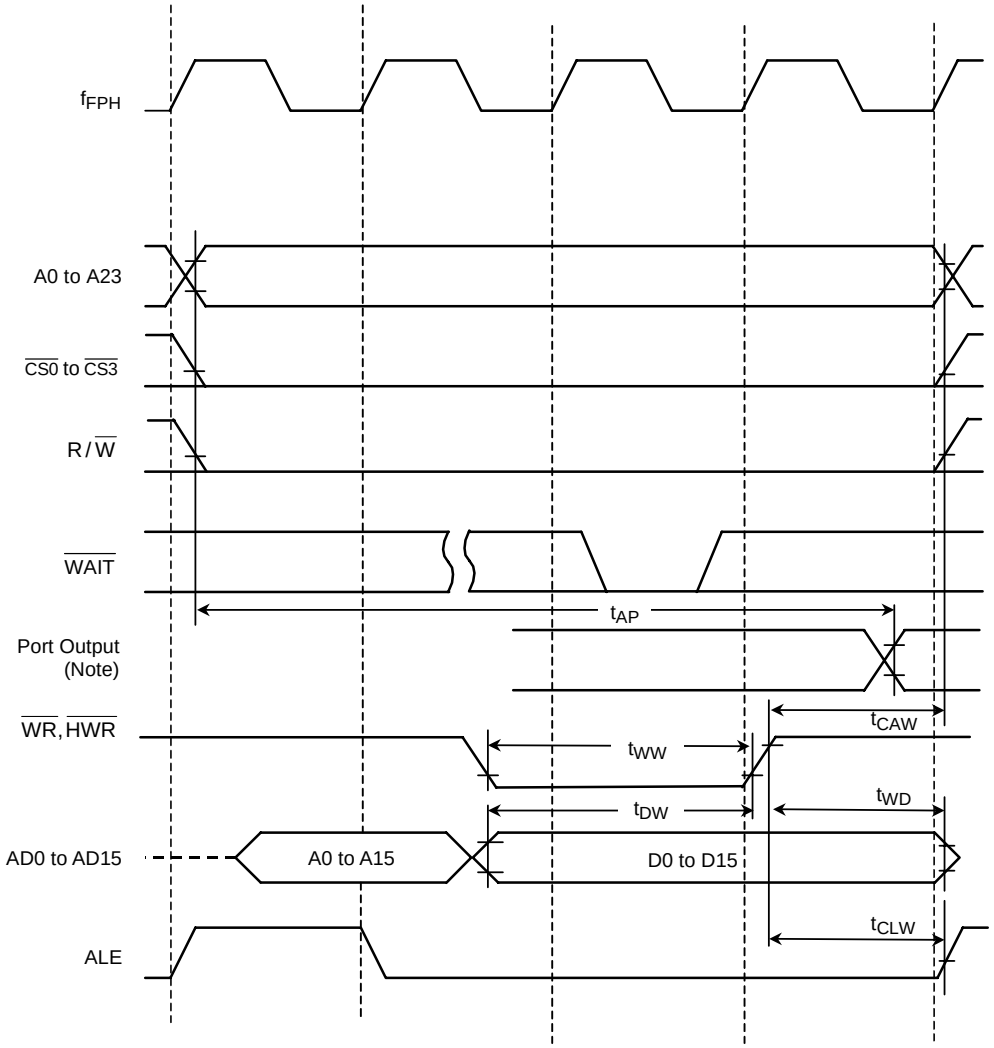
Note: "x" used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>.
The value of "x" changes according to whether a clock gear or a low-speed oscillator is selected.
An example value is calculated for fc, with gear=1/fc (SYSCR1<SYSCK,GEAR2 to 0> = 0000).

(3) Read Cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(4) Write Cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

AVcc = Vcc, AVss = Vss

parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	VREFH	Vcc = 3 V ± 10%	Vcc − 0.2 V	Vcc	Vcc	V
		Vcc = 2 V ± 10%	Vcc	Vcc	Vcc	
Analog Reference Voltage (−)	VREFL	Vcc = 3 V ± 10%	Vss	Vss	Vss + 0.2 V	
		Vcc = 2 V ± 10%	Vss	Vss	Vss	
Analog Input Voltage Range	VAIN		V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage <VREFON> = 1	IREF (VREFL = 0V)	Vcc = 3 V ± 10%		0.94	1.20	mA
		Vcc = 2 V ± 10%		0.65	0.90	
<VREFON> = 0		Vcc = 1.8 V to 3.3 V		0.02	5.0	μA
Error (not including quantizing errors)	−	Vcc = 3 V ± 10%		± 1.0	± 4.0	LSB
		Vcc = 2 V ± 10%		± 1.0	± 4.0	

Note 1: 1 LSB = (VREFH − VREFL)/1024 [V]

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4$ MHz.

Note 3: The value for I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Internal Mode)

(1) SCLK Input Mode

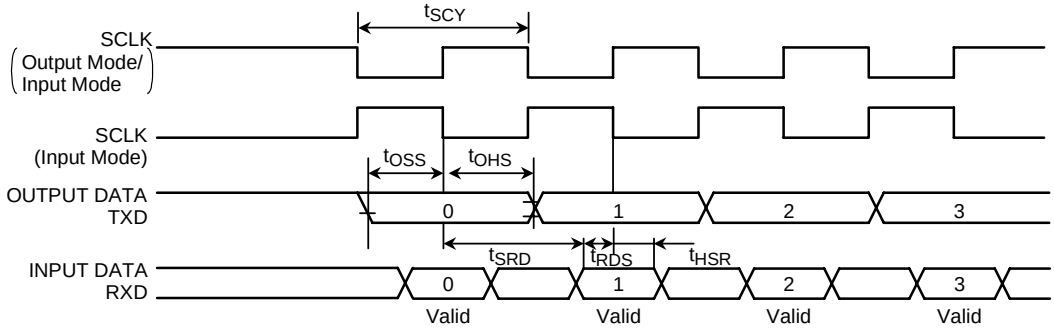
Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period	t_{SCY}	16X		1.6		0.59		μs
Output Data → SCLK Rising /Falling Edge*	t_{OSS}	$t_{SCY}/2 - 4x - 110$ (Vcc=3V±10%)		290		38		ns
		$t_{SCY}/2 - 4x - 180$ (Vcc=2V±10%)		220		—		
SCLK Rising/Falling Edge* → Output Data Hold	t_{OHS}	$t_{SCY}/2 + 2X + 0$		1000		370		ns
SCLK Rising/Falling Edge* → Input Data Hold	t_{HSR}	3x+10		310		121		ns
SCLK Rising/Falling Edge* → Valid Data Input	t_{SRD}		$t_{SCY} - 0$		1600		592	ns
Valid Data Input →SCLK Rising/Falling Edge*	t_{RDS}	0		0		0		ns

*) SCLK Rinsing/Falling Edge: The rising edge is used in SCLK Rising Mode.
The falling edge is used in SCLK Falling Mode.

Note: Value of 27 MHz and 10MHz at t_{SCY} = 16X.

(2) SCLK Output Mode

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period	t_{SCY}	16X	8192X	1.6	819	0.59	303	μs
Output Data → SCLK Rising/Falling Edge*	t_{OSS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising/Falling Edge* → Output Data Hold	t_{OHS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising/Falling Edge* → Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Rising/Falling Edge* → Valid Data Input	t_{SRD}		$t_{SCY} - 1X - 180$		1320		375	ns
Valid Data Input → SCLK Rising/Falling Edge*	t_{RDS}	1X + 180		280		217		ns



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock period	t_{VCK}	8X + 100		900		396		ns
Clock Low level width	t_{VCKL}	4X + 40		440		188		ns
Clock High level width	t_{VCKH}	4X + 40		440		188		ns

4.7 Interrupt and Capture

(1) $\overline{NMI}$, INT0 to INT4 Interrupts

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{NMI}$, INT0 to INT4 Low level width	t_{INTAL}	4X + 40		440		188		ns
$\overline{NMI}$, INT0 to INT4 High level width	t_{INTAH}	4X + 40		440		188		ns

(2) INT5 to INT8 Interrupts, Capture

The INT5 to INT8 input width depends on the system clock and prescaler clock settings.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1:0>	t_{INTBL} (INT5 to INT8 Low level Width)		t_{INTBH} (INT5 to INT8 High Level Width)		Unit
		Variable	f_{FPH} = 10 MHz	Variable	f_{FPH} = 27 MHz	
		Min	Min	Min	Min	
0 (fc)	00 (f_{FPH})	8X + 100	396	8X + 100	396	ns
	10 (fc/16)	128Xc + 0.1	4.8	128Xc + 0.1	4.8	μs
1 (fs)	00 (f_{FPH})	8X + 0.1	244.3	8X + 0.1	244.3	

Note: Xc = Period of Clock fc

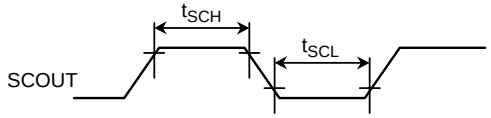
4.8 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		10 MHz		27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Low level width	t_{SCH}	0.5T – 13		37		5		Vcc ≥ 2.7 V	ns
		0.5T – 25		25		–		Vcc < 2.7 V	
High level width	t_{SCL}	0.5T – 13		37		5		Vcc ≥ 2.7 V	ns
		0.5T – 25		25		–		Vcc < 2.7 V	

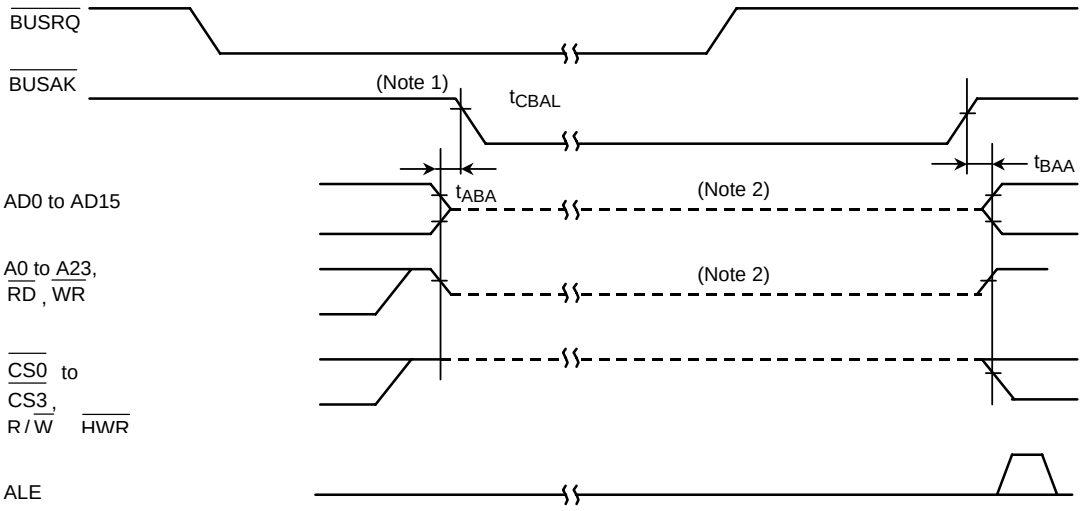
Note: T = Period of SCOUT

Measrement Condition

- Output Level: High 0.7 Vcc/Low 0.3 Vcc, CL = 10pF



4.9 Bus Request/Bus Acknowledge



Paramter	Symbol	Variable		f_{FPH} = 10 MHz		f_{FPH} = 27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Output Buffer Off to $\overline{BUSAK}$ Low	t_{ABA}	0	80	0	80	0	80	Vcc ≥ 2.7 V	ns
		0	300	0	300	0	300	Vcc < 2.7 V	
$\overline{BUSAK}$ High to Output Buffer On	t_{BAA}	0	80	0	80	0	80	Vcc ≥ 2.7 V	ns
		0	300	0	300	0	300	Vcc < 2.7 V	

Note 1: Even if the $\overline{BUSRQ}$ Signal goes Low, the bus will not be released while the $\overline{WAIT}$ signal is Low. The bus will only be released when $\overline{BUSRQ}$ goes Low while $\overline{WAIT}$ is High.

Note 2: This line shows only that the output buffer is in the Off state.
It does not indicate that the signal level is fixed.
Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resister during bus release, careful design is necessary, since fixing of the level is delayed.
The internal programmable pull-up/pull-down resistor is switched between the active and non-active states by the internal signal.

4.10 Recommended Oscillation Circuit

TMP91CY22I has been evaluated by murata manufacturing Co., Ltd. Please refer to murata manufacturing Co., Ltd.

Note: Total loads value of oscillator is sum of external loads (C1 and C2) and floating loads of actual assemble board. There is a possibility of miss-operating. When designing board, it should design minimum length pattern around oscillator. And we recommend that oscillator evaluation try on your actual using board.

(1) Examples of resonator connection

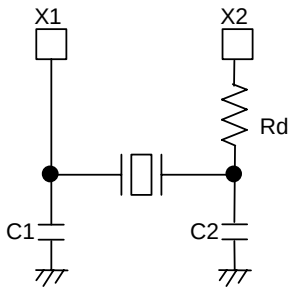


Figure 4.10.1 High-frequency Oscillator Connection

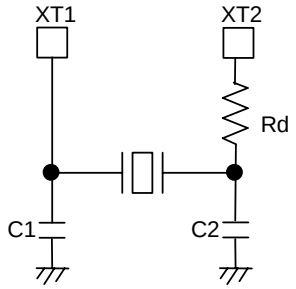


Figure 4.10.2 Low-frequency Oscillator Connection

(2) Recommended ceramic resonators for TMP91CY22I: Murata Manufacturing Co., Ltd.

Ta = –40 to 85°C

MCU	Oscillation Frequency [MHZ]	Item of Oscillator	Parameter of Elements			Running Condition	
			C1 [pF]	C2 [pF]	Rd [Ω]	Voltage of Power [V]	Tc[°C]
TMP91CY22I	2.00	CSTCC2M00G56-R0	(47)	(47)	0	1.8 ~ 2.2	-20 ~ +80
	4.00	CSTCR4M00G55-R0	(39)	(39)		2.7 ~ 3.3	
		CSTLS4M00G56-B0	(47)	(47)			
	6.00	CSTCR6M75G55-R0	(39)	(39)			
		CSTLS6M75G56-B0	(47)	(47)			
	10.00	CSTLS10M0G53-B0	(15)	(15)		1.8 ~ 2.2	

- In CST*** type oscillator, capacitance C1, C2 is built-in.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;

  http://www.murata.co.jp

5. Package Dimensions

P-LQFP100-1414-0.50F

Unit: mm