

# ZXMN3F31DN8

## 30V SO8 dual N-channel enhancement mode MOSFET

### Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.024 @ $V_{GS} = 10V$	7.3
	0.039 @ $V_{GS} = 4.5V$	5.7



### Description

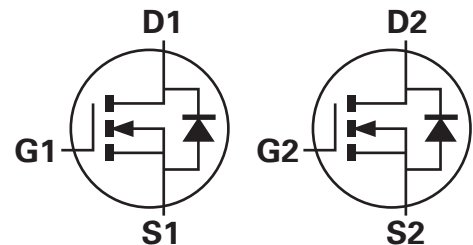
This new generation Trench MOSFET from Zetex features low on-resistance achievable with 4.5V gate drive.

### Features

- Low on-resistance
- 4.5V gate drive capability

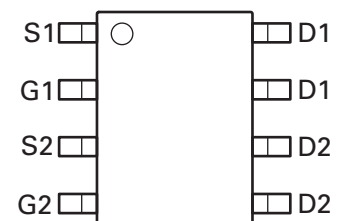
### Applications

- DC-DC Converters
- Power management functions
- Load switching
- Motor control
- Back lighting



### Ordering information

DEVICE	Reel size (inches)	Tape width (mm)	Quantity per reel
ZXMN3F31DN8TA	7	12	500



### Device marking

ZXMN  
3F31D

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## Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain source voltage	$V_{DSS}$	30	V
Gate source voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $V_{GS}=10$ ; $T_A=25^\circ\text{C}^{(b)}$ @ $V_{GS}=10$ ; $T_A=70^\circ\text{C}^{(b)}$ @ $V_{GS}=10$ ; $T_A=25^\circ\text{C}^{(a)}$	$I_D$	7.3 5.9 5.7	A A A
Pulsed drain current <sup>(c)</sup>	$I_{DM}$	33	A
Continuous source current (body diode) <sup>(b)</sup>	$I_S$	3	A
Pulsed source current (body diode) <sup>(c)</sup>	$I_{SM}$	33	A
Power dissipation at $T_A=25^\circ\text{C}^{(a)(d)}$ Linear derating factor	$P_D$	1.25 10	W mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(a)(e)}$ Linear derating factor	$P_D$	1.8 14	W mW/°C
Power dissipation at $T_A=25^\circ\text{C}^{(b)(d)}$ Linear derating factor	$P_D$	2.1 17	W mW/°C
Operating and storage temperature range	$T_j, T_{stg}$	-55 to 150	°C

## Thermal resistance

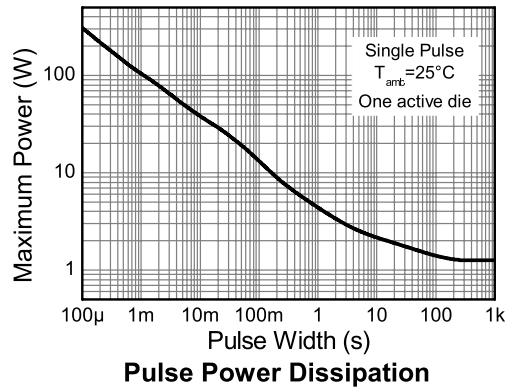
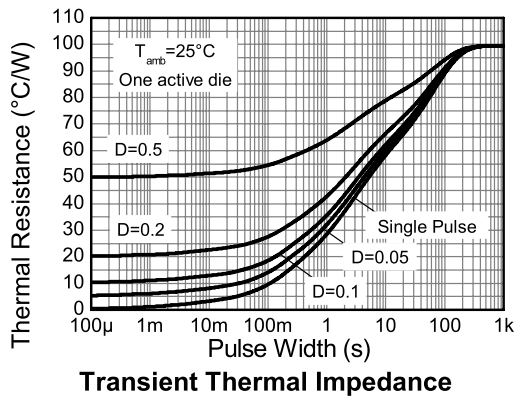
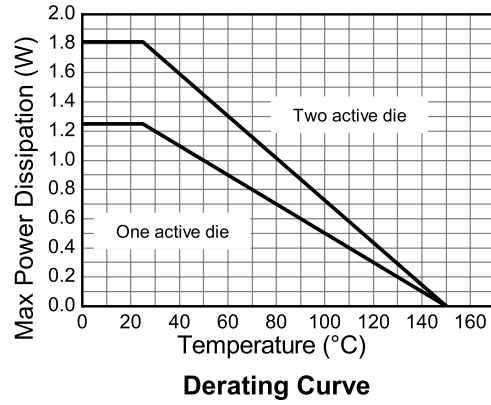
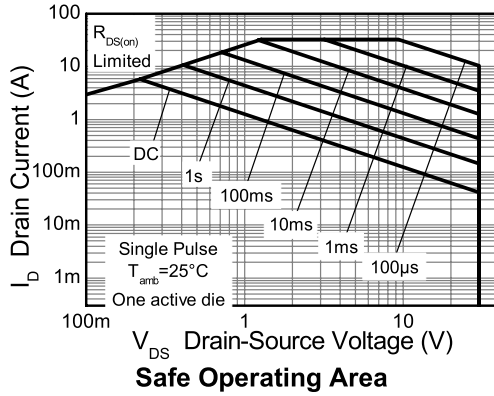
Parameter	Symbol	Limit	Unit
Junction to ambient <sup>(a)(d)</sup>	$R_{\theta JA}$	100	°C/W
Junction to ambient <sup>(a)(e)</sup>	$R_{\theta JA}$	70	°C/W
Junction to ambient <sup>(b)(d)</sup>	$R_{\theta JA}$	60	°C/W
Junction to lead <sup>(f)</sup>	$R_{\theta JL}$	53	°C/W

### NOTES:

- (a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.
- (b) For a device surface mounted on FR4 PCB measured at  $t \leq 10$  sec.
- (c) Repetitive rating - 25mm x 25mm FR4 PCB,  $D=0.02$ , pulse width 300 $\mu\text{s}$  - pulse width limited by maximum junction temperature.
- (d) For a dual device with one active die.
- (e) For a device with two active die running at equal power.
- (f) Thermal resistance from junction to solder-point (at end of drain lead).

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## Thermal characteristics



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## Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	30			V	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$			0.5	$\mu\text{A}$	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Body Leakage	$I_{GSS}$			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0		3.0	V	$I_D = 250\mu\text{A}, V_{DS} = V_{GS}$
Static Drain-Source On-State Resistance (*)	$R_{DS(on)}$			0.024 0.039	$\Omega$ $\Omega$	$V_{GS} = 10\text{V}, I_D = 7.0\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 6.0\text{A}$
Forward Transconductance <sup>(*)(†)</sup>	$g_{fs}$		16.5		S	$V_{DS} = 15\text{V}, I_D = 7\text{A}$
<b>Dynamic</b> (†)						
Input Capacitance	$C_{iss}$		608		pF	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$
Output Capacitance	$C_{oss}$		132		pF	
Reverse Transfer Capacitance	$C_{rss}$		71		pF	
<b>Switching</b> (‡)(†)						
Turn-On-Delay Time	$t_{d(on)}$		2.9		ns	$V_{DD} = 15\text{V}, I_D = 1\text{A}$ $R_G \cong 6.0\Omega, V_{GS} = 10\text{V}$
Rise Time	$t_r$		3.3		ns	
Turn-Off Delay Time	$t_{d(off)}$		16		ns	
Fall Time	$t_f$		8		ns	
Total Gate Charge	$Q_g$		12.9		nC	$V_{DS} = 15\text{V}, V_{GS} = 10\text{V}$ $I_D = 7\text{A}$
Gate-Source Charge	$Q_{gs}$		2.5		nC	
Gate Drain Charge	$Q_{gd}$		2.52		nC	
<b>Source-drain diode</b>						
Diode Forward Voltage <sup>(*)</sup>	$V_{SD}$		0.82	1.2	V	$T_j = 25^{\circ}\text{C}, I_S = 1.7\text{A}, V_{GS} = 0\text{V}$

### NOTES:

(\*) Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

(†) For design aid only, not subject to production testing

(‡) Switching characteristics are independent of operating junction temperature.

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## Typical characteristics

Fig1.  $I_D - V_{DS}$

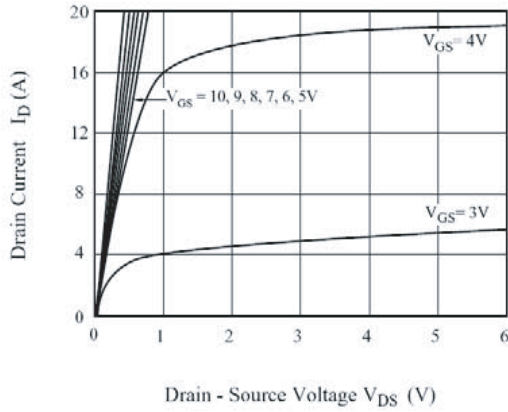


Fig2.  $I_D - V_{GS}$

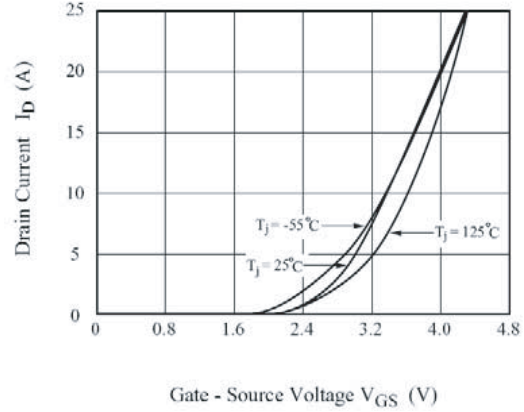


Fig3.  $V_{th} - T_j$

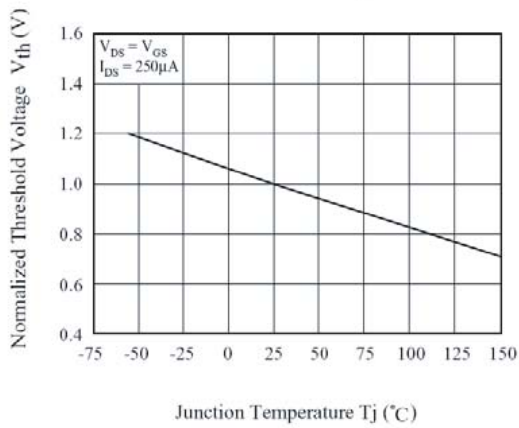


Fig4.  $I_{DR} - V_{SD}$

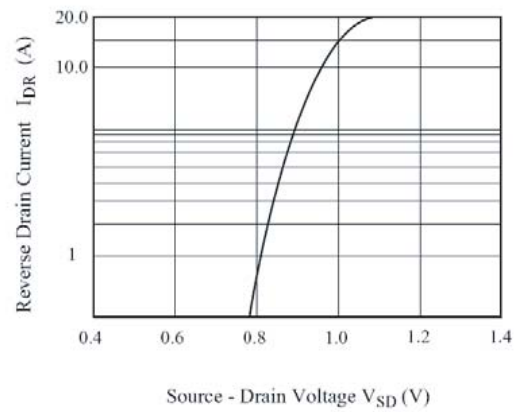
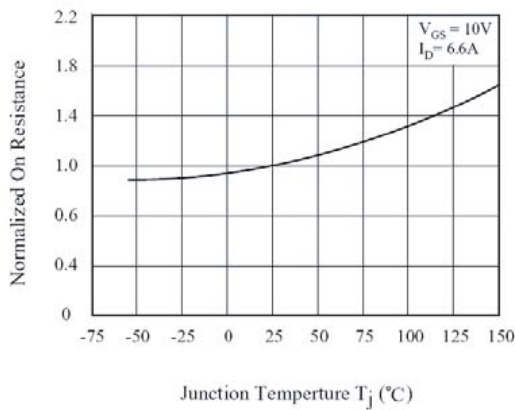
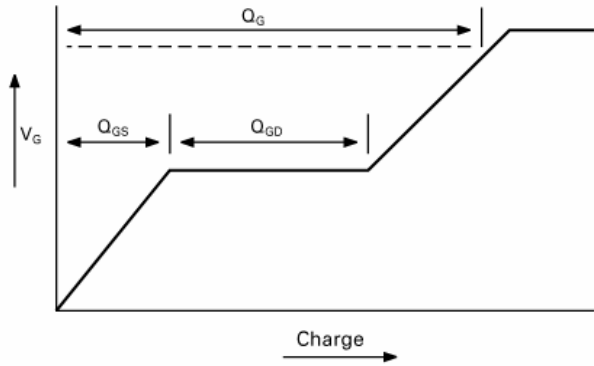


Fig5.  $R_{DS(ON)} - T_j$

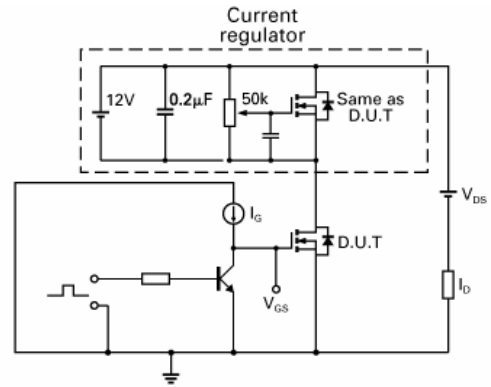


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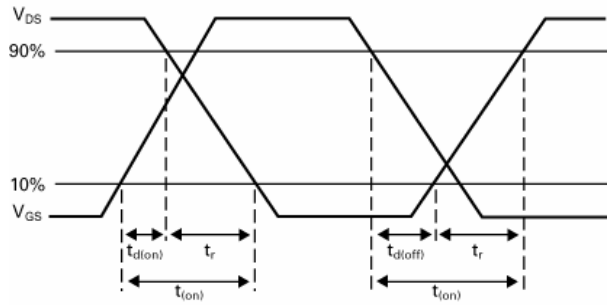
## Test circuits



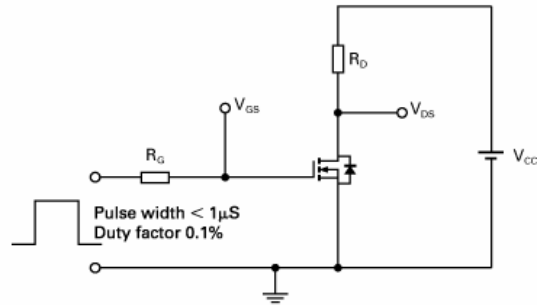
**Basic gate charge waveform**



**Gate charge test circuit**



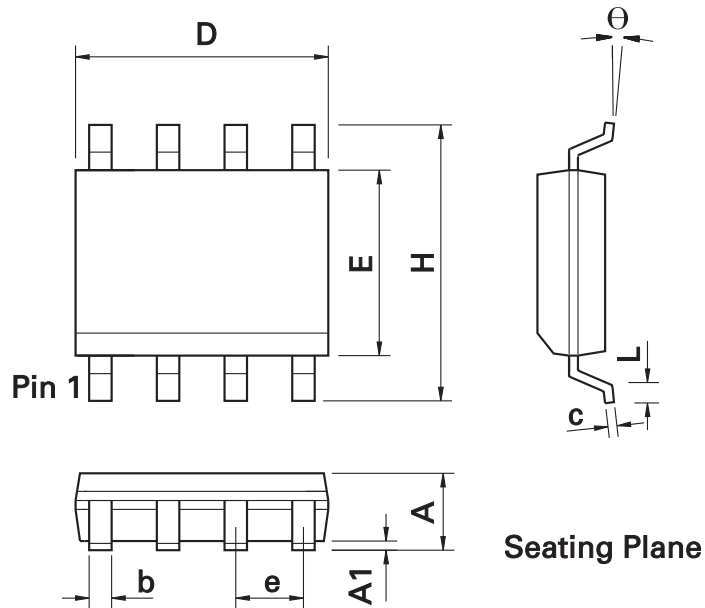
**Switching time waveforms**



**Switching time test circuit**

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## Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	Θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

**Note:** Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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