Data Sheet April 20, 2007 FN6301.1

Dual and Quad Precision Micropower Single Supply Rail-to-Rail Input and Output Precision Op Amps

The ISL28276 and ISL28476 are Dual and Quad channel micropower precision operational amplifier optimized for single supply operation at 5V and can operate down to 2.4V. For equivalent performance in a single channel op-amp reference EL8176.

The ISL28276 and ISL28476 feature an Input Range Enhancement Circuit (IREC) which enables both parts to maintain CMRR performance for input voltages equal to the positive and negative supply rails. The input signal is capable of swinging 0.5V above a 5.0V supply (0.25V for a 2.4V supply) and to within 10mV from ground. The output operation is rail to rail.

The both parts draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications. Offset current, voltage and current noise, slew rate, and gain-bandwidth product are all two to ten times better than other micropower op-amps with equivalent supply current ratings.

The ISL28276 and ISL28476 can be operated from one lithium cell or two Ni-Cd batteries. The input range includes both positive and negative rail.

Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28276IAZ	28276 IAZ	97/Tube	16 Ld QSOP	MDP0040
ISL28276IAZ-T7	28276 IAZ	7” (1k pcs)	16 Ld QSOP	MDP0040
Coming Soon ISL28476FAZ	28476 FAZ	97/Tube	16 Ld QSOP	MDP0040
Coming Soon ISL28476FAZ-T7	28476 FAZ	7” (1k pcs)	16 Ld QSOP	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

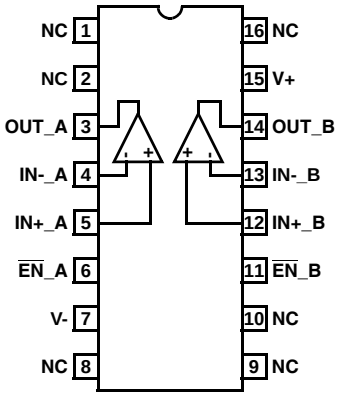
- 60µA supply current per channel
- 100µV max offset voltage
- 500pA input bias current
- 400kHz gain-bandwidth product
- 115dB PSRR and CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above V+ and within 10mV of Ground
- Rail-to-rail output
- Output sources 31mA load current
- Pb-free plus anneal available (RoHS compliant)

Applications

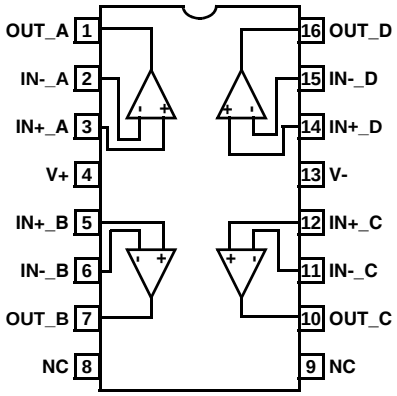
- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

Pinouts

ISL28276
(16 LD QSOP)
TOP VIEW



ISL28476
(16 LD QSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage 5.5V, 1V/µs
Differential Input Current 5mA
Differential Input Voltage 0.5V
Input Voltage . . . . . V_- - 0.5V to V_+ + 0.5V
ESD tolerance, Human Body Model 3kV
ESD tolerance, Machine Model 300V

Thermal Information

Output Short-Circuit Duration . . . . . .Indefinite
Ambient Operating Temperature Range . . . . . .-40°C to +125°C
Storage Temperature Range . . . . . .-65°C to +150°C
Operating Junction Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_+ = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = +25°C unless otherwise specified.
Boldface limits apply over the operating temperature range, -40°C to +125°C

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input Offset Voltage		-100 **-150**	20	100 **150**	µV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability			1.2		µV/Mo
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Drift vs Temperature			0.3		µV/°C
I_{OS}	Input Offset Current			0.25	1.3 **2.0**	nA
I_B	Input Bias Current		-2 **-2.5**	0.5	2 **2.5**	nA
e_N	Input Noise Voltage Peak-to-Peak	f = 0.1Hz to 10Hz		1		μV_{P-P}
	Input Noise Voltage Density	f_O = 1kHz		25		nV/√Hz
i_N	Input Noise Current Density	f_O = 1kHz		0.1		pA/√Hz
CMIR	Input Voltage Range	Guaranteed by CMRR test	**0**		**5**	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	90 **80**	115		dB
PSRR	Power Supply Rejection Ratio	V_+ = 2.4V to 5V	90 **80**	115		dB
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5V to 4.5V, R_L = 100kΩ	350 **350**	550		V/mV
		V_O = 0.5V to 4.5V, R_L = 1kΩ		25		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output low, R_L = 100kΩ		3	6 **30**	mV
		Output low, R_L = 1kΩ		130	175 **225**	mV
		Output high, R_L = 100kΩ	4.990 **4.97**	4.996		V
		Output high, R_L = 1kΩ	4.800 **4.750**	4.880		V
SR+	Positive Slew Rate		0.13 **0.10**	0.17	0.20 **0.25**	V/µs
SR-	Negative Slew Rate		0.10 **0.09**	0.13	0.17 **0.19**	V/µs
GBW	Gain Bandwidth Product			400		kHz

Electrical Specifications V_+ = 5V, 0V, V_{CM} = 0.1V, V_O = 1.4V, T_A = +25°C unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{S,ON}$	Supply Current, Enabled	ISL28276 all channels enabled.		120	156 **175**	µA
$I_{S,OFF}$	Supply Current, Disabled			4	7 **9**	µA
$I_{S,ON}$	Supply Current, Enabled	ISL28476 all channels enabled.		240	312 **350**	µA
$I_{S,OFF}$	Supply Current, Disabled			8	14 **18**	µA
I_{SC}^+	Short Circuit Sourcing Capability	R_L = 10Ω	29 **23**	31		mA
I_{SC}^-	Short Circuit Sinking Capability	R_L = 10Ω	24 **19**	26		mA
V_S	Minimum Supply Voltage		**2.4**			V
V_{INH}	Enable Pin High Level				**2**	V
V_{INL}	Enable Pin Low Level		**0.8**			V
I_{ENH}	Enable Pin Input Current	V_{EN} = 5V		0.7	1.3 **1.5**	µA
I_{ENL}	Enable Pin Input Current	V_{EN} = 0V	**-0.1**	0	**+0.1**	µA

Typical Performance Curves

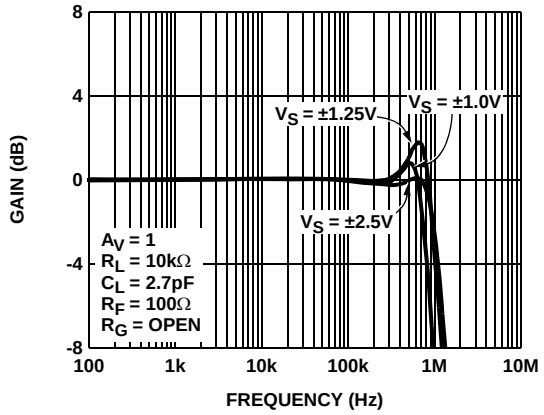


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

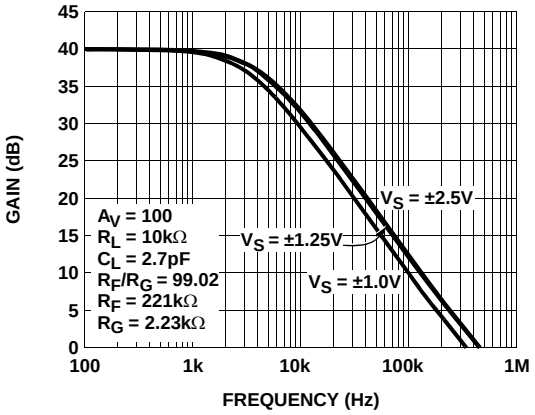


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

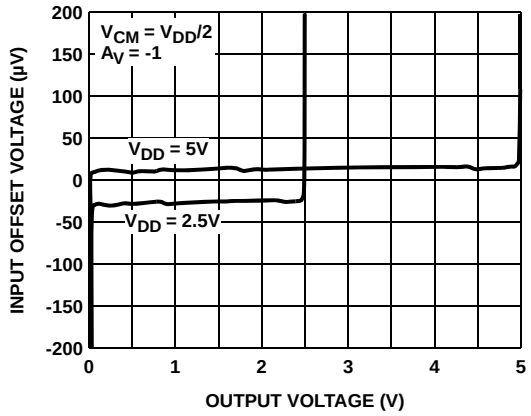


FIGURE 3. INPUT OFFSET VOLTAGE vs OUTPUT VOLTAGE

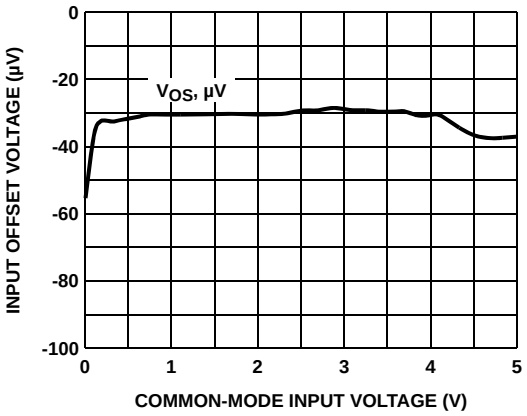


FIGURE 4. INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

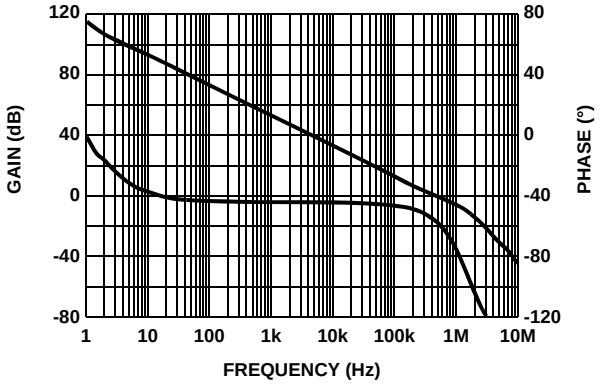


FIGURE 5. A_{VOL} vs FREQUENCY @ 100kΩ LOAD

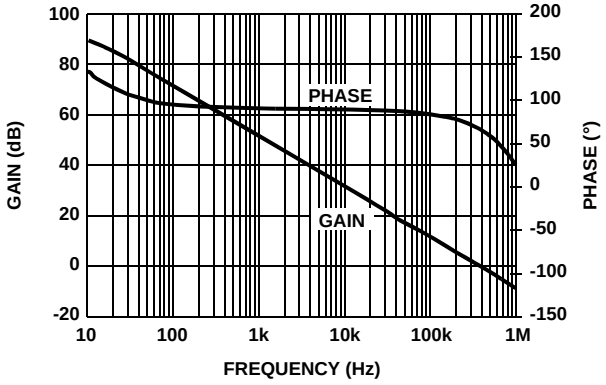


FIGURE 6. A_{VOL} vs FREQUENCY @ 1kΩ LOAD

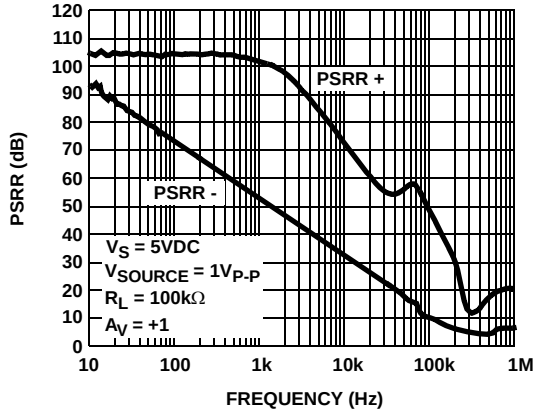


FIGURE 7. PSRR vs FREQUENCY

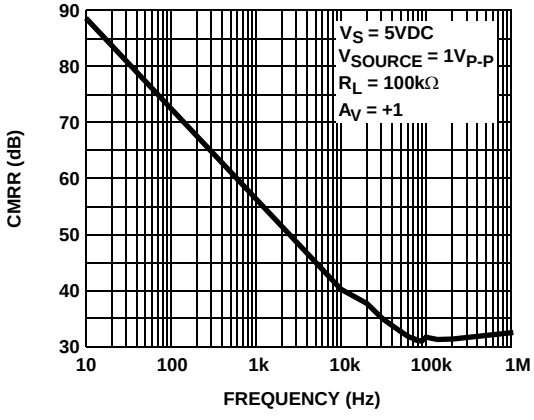


FIGURE 8. CMRR vs FREQUENCY

Typical Performance Curves (Continued)

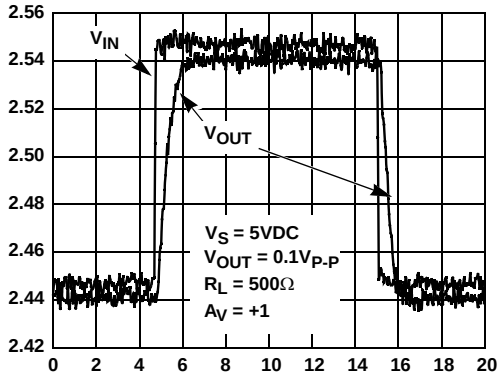


FIGURE 9. SMALL SIGNAL TRANSIENT RESPONSE

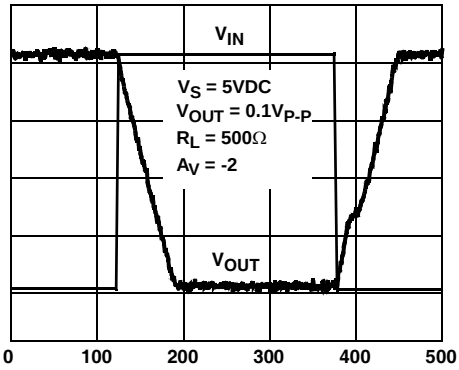


FIGURE 10. LARGE SIGNAL TRANSIENT RESPONSE

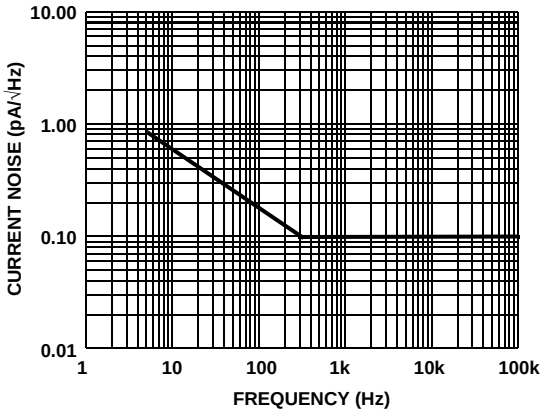


FIGURE 11. CURRENT NOISE vs FREQUENCY

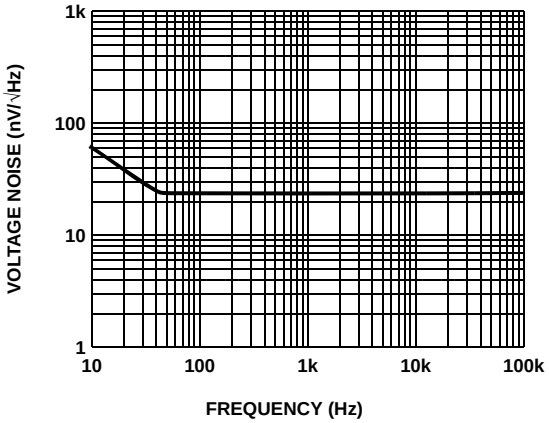


FIGURE 12. VOLTAGE NOISE vs FREQUENCY

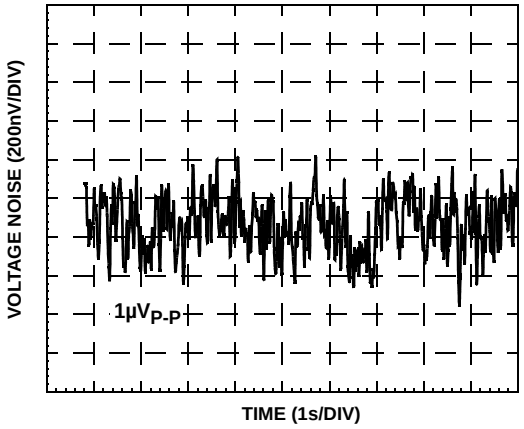


FIGURE 13. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

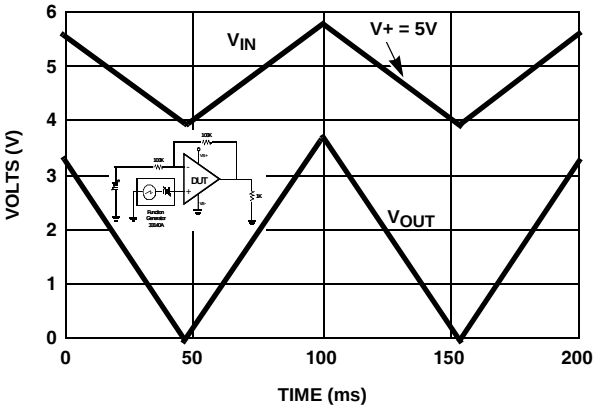


FIGURE 14. INPUT VOLTAGE SWING ABOVE THE V+ SUPPLY

Typical Performance Curves (Continued)

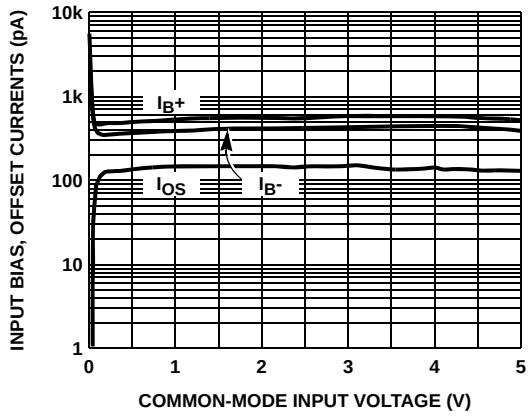


FIGURE 15. INPUT BIAS + OFFSET CURRENTS vs COMMON-MODE INPUT VOLTAGE

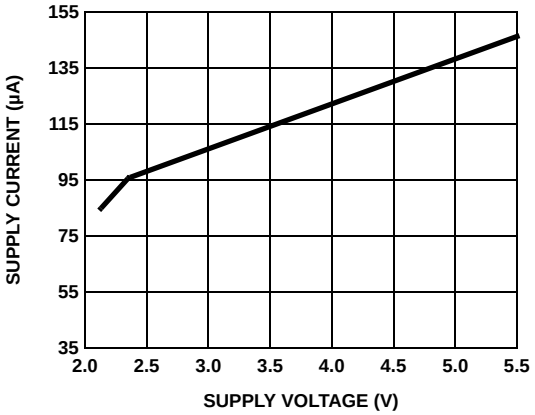


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

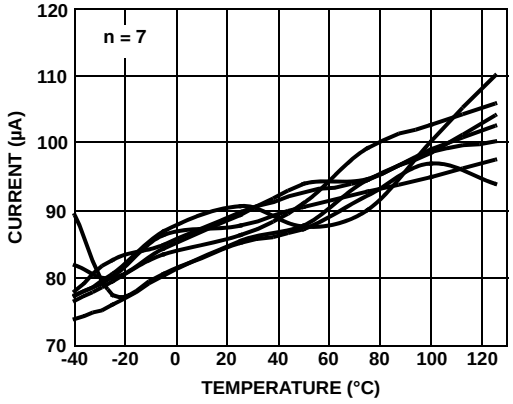


FIGURE 17. SUPPLY CURRENT vs TEMPERATURE V_S = ±1.2V ENABLED. R_L = INF

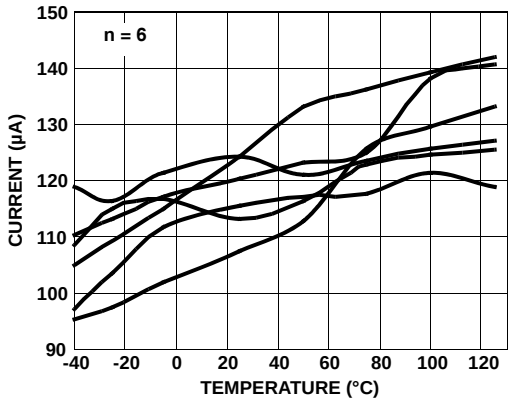


FIGURE 18. SUPPLY CURRENT vs TEMPERATURE V_S = ±2.5V ENABLED. R_L = INF

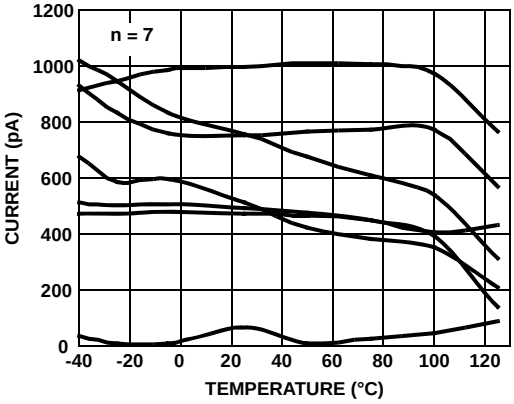


FIGURE 19. I_{BIAS}+ vs TEMPERATURE V_S = ±2.5V

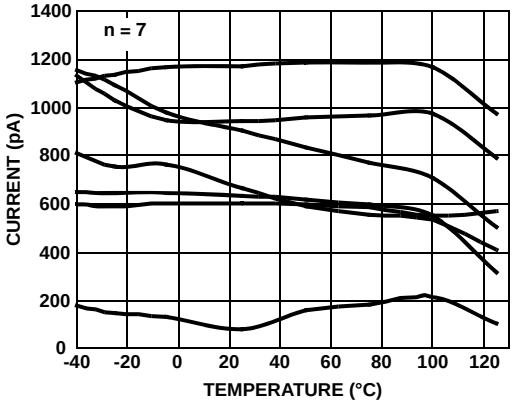


FIGURE 20. I_{BIAS}+ vs TEMPERATURE V_S = ±1.2V

Typical Performance Curves (Continued)

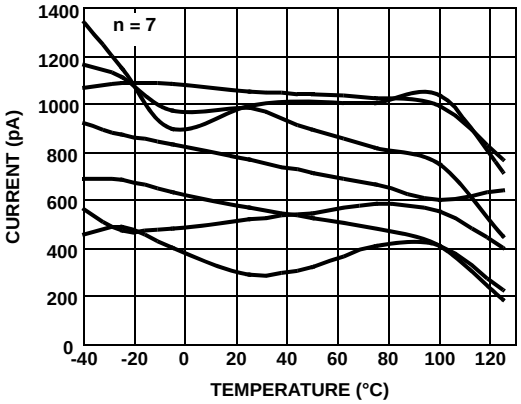


FIGURE 21. I_{BIAS-} vs TEMPERATURE V_S = ±2.5V

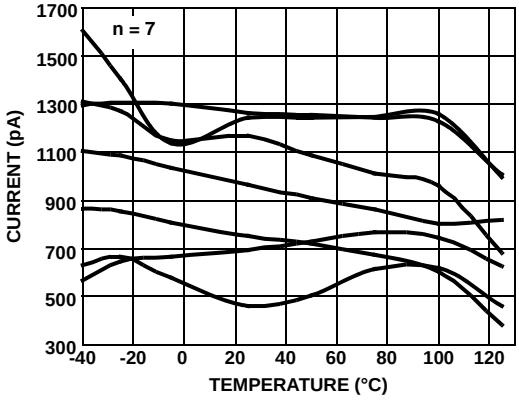


FIGURE 22. I_{BIAS-} vs TEMPERATURE V_S = ±1.2V

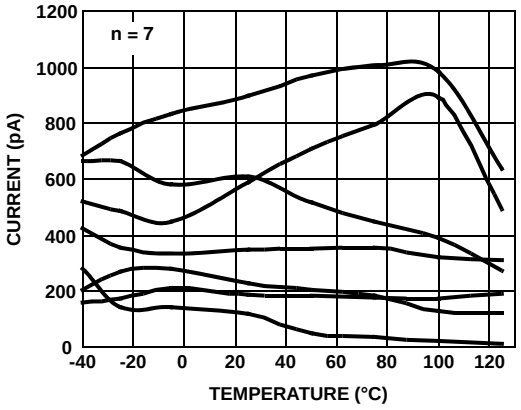


FIGURE 23. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±2.5V

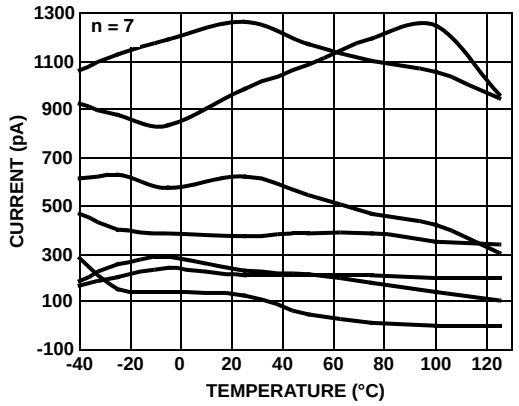


FIGURE 24. INPUT OFFSET CURRENT vs TEMPERATURE V_S = ±1.2V

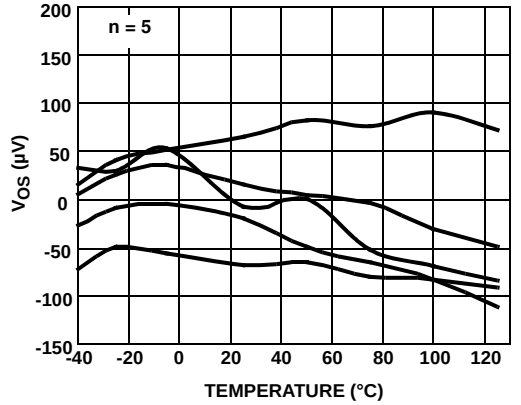


FIGURE 25. INPUT OFFSET VOLTAGE vs TEMPERATURE V_S = ±2.5V

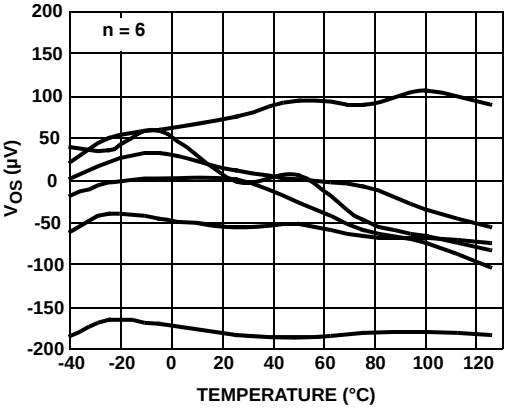


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE V_S = ±1.2V

Typical Performance Curves (Continued)

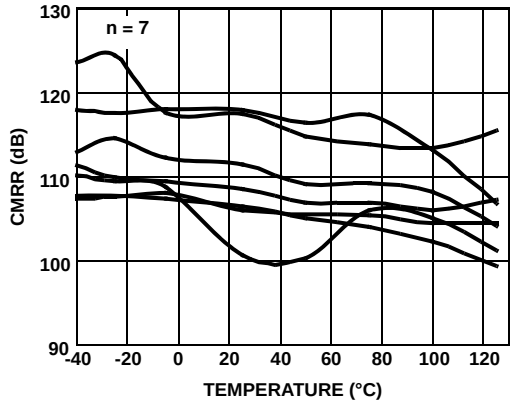


FIGURE 27. CMRR vs TEMPERATURE V_{CM} = +2.5V TO -2.5V

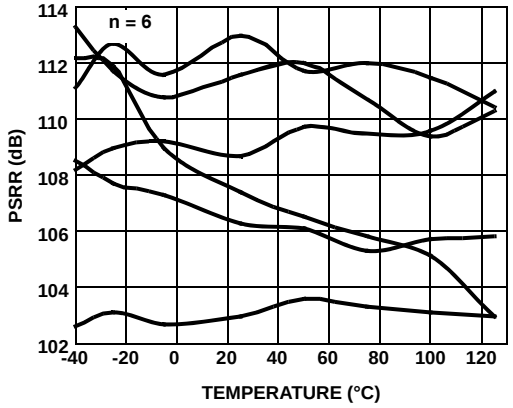


FIGURE 28. PSRR vs TEMPERATURE V_S = ±1.2V TO ±2.5V

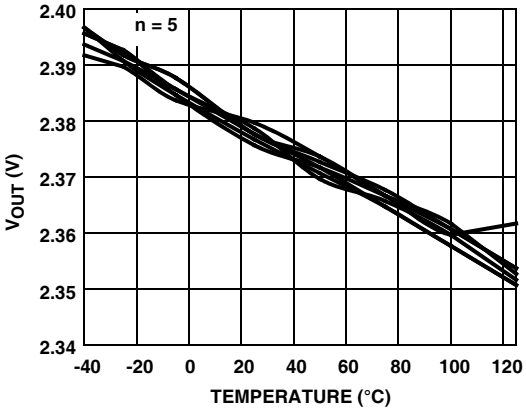


FIGURE 29. POSITIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

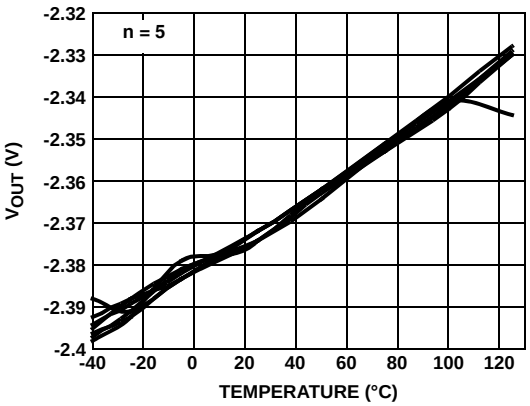


FIGURE 30. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 1k V_S = ±2.5V

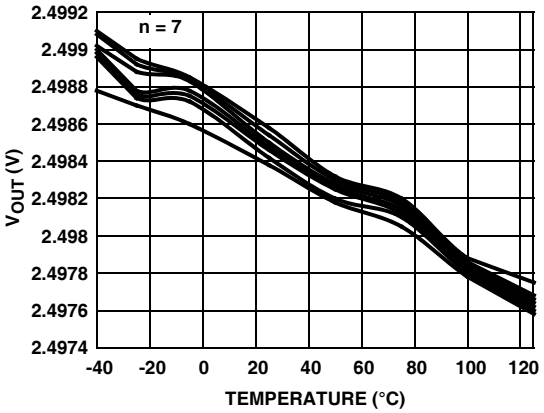


FIGURE 31. POSITIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

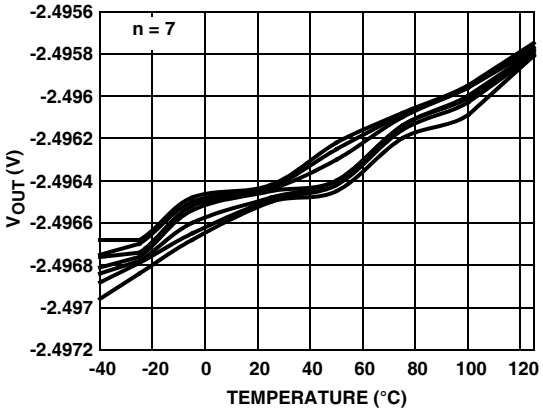


FIGURE 32. NEGATIVE V_{OUT} vs TEMPERATURE R_L = 100k V_S = ±2.5V

Typical Performance Curves (Continued)

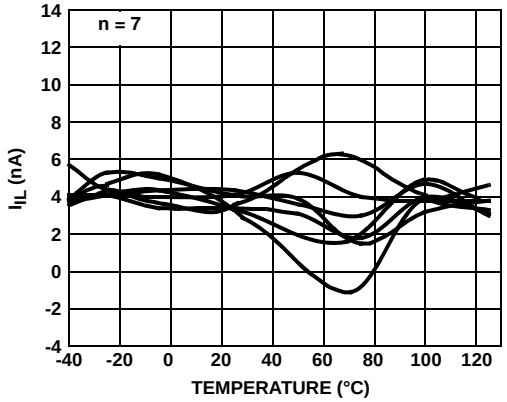


FIGURE 33. I_{IL} (EN) vs TEMPERATURE V_S = ±2.5V

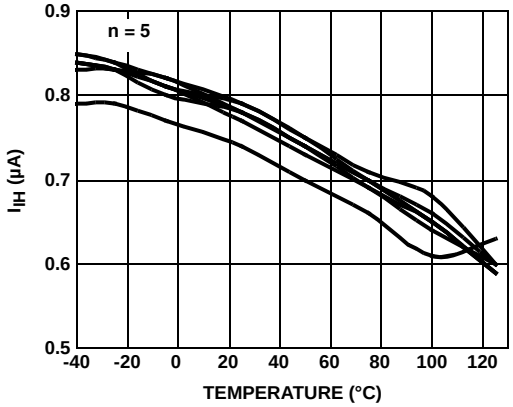


FIGURE 34. I_{IH} (EN) vs TEMPERATURE V_S = ±2.5V

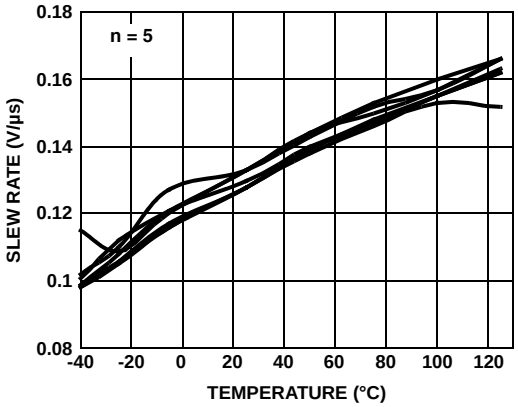


FIGURE 35. + SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V A_V = 2

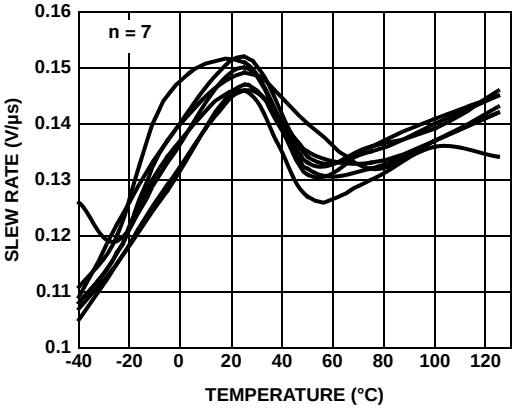


FIGURE 36. - SLEW RATE vs TEMPERATURE V_S = ±2.5V INPUT = ±0.75V A_V = 2

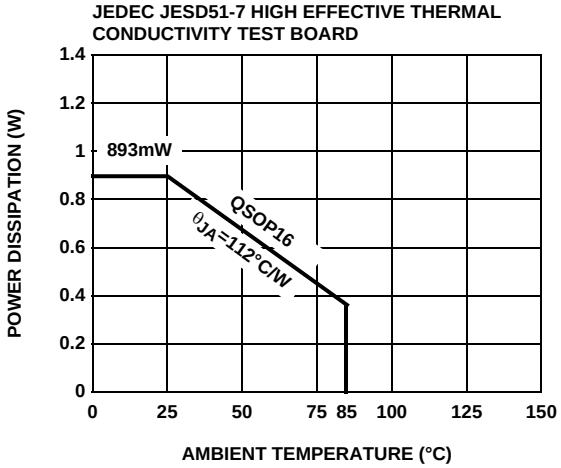


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

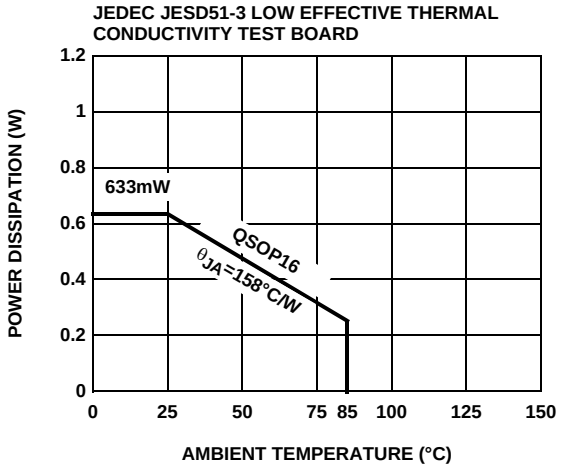
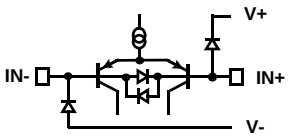


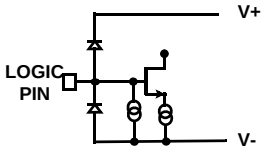
FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

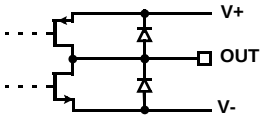
ISL28276 (16 LD QSOP)	ISL28476 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	1	OUT_A	Circuit 3	Amplifier A output
4	2	IN-_A	Circuit 1	Amplifier A inverting input
5	3	IN+_A	Circuit 1	Amplifier A non-inverting input
15	4	V+	Circuit 4	Positive power supply
12	5	IN+_B	Circuit 1	Amplifier B non-inverting input
13	6	IN-_B	Circuit 1	Amplifier B inverting input
14	7	OUT_B	Circuit 3	Amplifier B output
1, 2, 8, 9, 10, 16	8, 9	NC		No internal connection
	10	OUT_C	Circuit 3	Amplifier C output
	11	IN-_C	Circuit 1	Amplifier C inverting input
	12	IN+_C	Circuit 1	Amplifier B non-inverting input
7	13	V-	Circuit 4	Negative power supply
	14	IN+_D	Circuit 1	Amplifier D non-inverting input
	15	IN-_D	Circuit 1	Amplifier D inverting input
	16	OUT_D	Circuit 3	Amplifier D output
6		$\overline{EN}$_A	Circuit 2	Amplifier A enable pin internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.
11		$\overline{EN}$_B	Circuit 2	Amplifier B enable pin with internal pull-down; Logic “1” selects the disabled state; Logic “0” selects the enabled state.



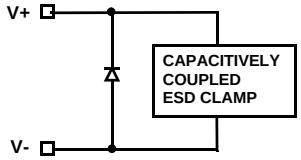
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

Applications Information

Introduction

The ISL28276 and ISL28476 are Dual and Quad channel CMOS rail-to-rail input, output (RRIO) micropower precision operational amplifier with an enable feature. The parts are designed to operate from single supply (2.4V to 5.0V) or dual supply (±1.2V to ±2.5V) while drawing only 120μA of supply current. The device has an input common mode range that extends 10% above the positive rail and up to 100mV below the negative supply rail. The output operation can swing within about 4mV of the supply rails with a 100kΩ load (reference Figures 29 through 32). This combination of low power and precision performance makes them suitable for solar and battery power applications.

Rail-to-Rail Input

The input common-mode voltage range of the ISL28276 and ISL28476 is from the negative supply to 10% greater than the positive supply without introducing additional offset errors or degrading performance associated with a conventional rail-to-rail input operational amplifier. Many rail-to-rail input stages use two differential input pairs, a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an undesired change in magnitude and polarity of input offset current.

The ISL28276 and ISL28476 achieve input rail-to-rail operation without sacrificing important precision specifications and degrading distortion performance. The devices’ input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives us an undistorted behavior from typically 100mV below the

negative rail and 10% higher than the V+ rail (0.5V higher than V+ when V+ equals 5V).

Input Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. They have additional back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA.

Input Bias Current Compensation

The input bias currents are decimated down to a typical of 500pA while maintaining an excellent bandwidth for a micro-power operational amplifier. Inside the ISL28276 and ISL28476 is an input bias canceling circuit. The input stage transistors are still biased with an adequate current for speed but the canceling circuit sinks most of the base current, leaving a small fraction as input bias current.

Rail-to-Rail Output

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. The output with a 100kΩ load will swing to within 3mV of the supply rails.

Enable/Disable Feature

The ISL28276 offers an $\overline{EN}$ pin that disables the device when pulled up to at least 2.2V. In the disabled state (output in a high impedance state), the part consumes typically 4µA. By disabling the part, multiple ISL28276 parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the $\overline{EN}$ pin. The $\overline{EN}$ pin also has an internal pull down. If left open, the $\overline{EN}$ pin will pull to the negative rail and the device will be enabled by default.

Proper Layout Maximizes Performance

To achieve the maximum performance of the high input impedance and low offset voltage, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 39 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

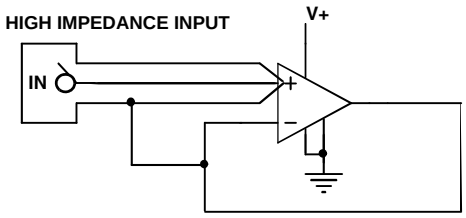


FIGURE 39. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

Example Application

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28276 (Figure 40) is used to convert the differential thermocouple voltage into single-ended signal with 10X gain. The ISL28276's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the converter to run from a single 5V supply.

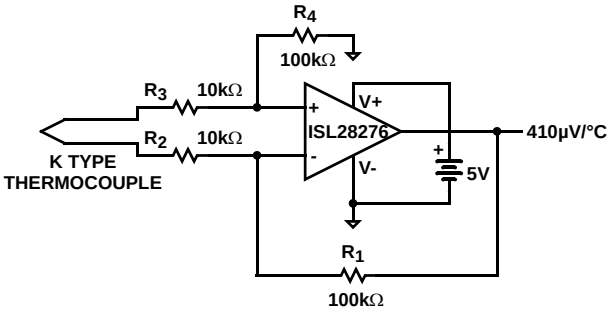
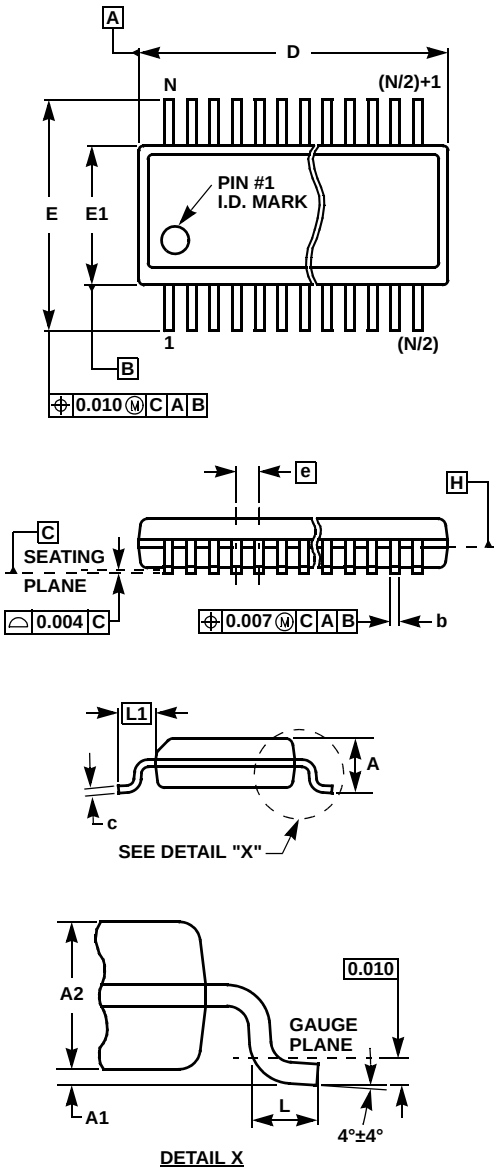


FIGURE 40. THERMOCOUPLE AMPLIFIER

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.