TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC7MBL6353SFT, TC7MBL6353SFK, TC7MBL6353SFTG

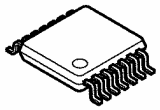
## Low Voltage/Low Capacitance Dual 1-of-2 Multiplexer/Demultiplexer

The TC7MBL6353S is a Low Voltage/Low Capacitance CMOS Dual 1-of-2 Multiplexer/Demultiplexer. The low on-resistance of the switch allows connections to be made with minimal propagation delay time.

This device consists of two individual two-inputs multiplexer/ demultiplexer with common select input (S) and output enable ($\overline{OE}$). The A input is connected to the B1 or B2 outputs as determined by the combination of both the select input (S) and output enable ($\overline{OE}$). When the output enable ($\overline{OE}$) input is held at "H" level, the switches are open regardless of the state of the select inputs, and a high-impedance state exists between the switches.

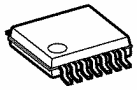
All inputs are equipped with protection circuits against static discharge.

TC7MBL6353SFT



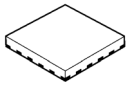
TSSOP14-P-0044-0.65A

TC7MBL6353SFK



VSSOP14-P-0030-0.50

TC7MBL6353SFTG



VQON16-P-0303-0.50

Weight

| | |
|---|---|
| TSSOP14-P-0044-0.65A | : 0.06 g (typ.) |
| VSSOP14-P-0030-0.50 | : 0.02 g (typ.) |
| VQON16-P-0303-0.50 | : 0.013 g(typ.) |

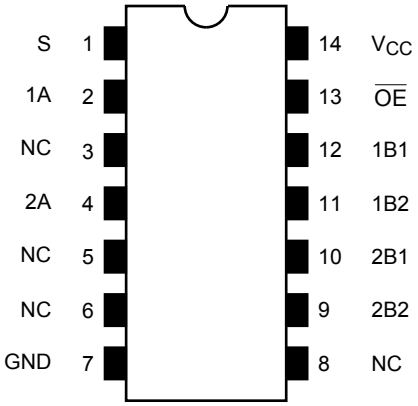
### Features

- Operating voltage: $V_{CC}$ = 1.65~3.6 V
- Low capacitance: $C_{I/O}$ = 15 pF Switch On (typ.) @3 V
- Low on-resistance: $R_{ON}$ = 9 Ω (typ.) @3 V
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- Power-down protection for inputs ($\overline{OE}$ input only)
- Package: TSSOP14,VSSOP (US14), VQON16

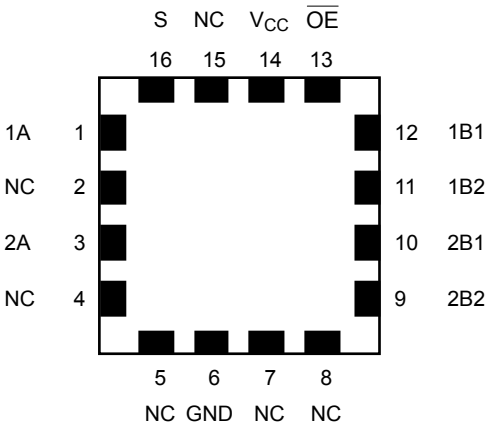
Note: When mounting VQON package, the type of recommended flux is RA or RMA.

## Pin Assignment (top view)

FT (TSSOP14-P-0044-0.65A)
FK (VSSOP14-P-0030-0.50)



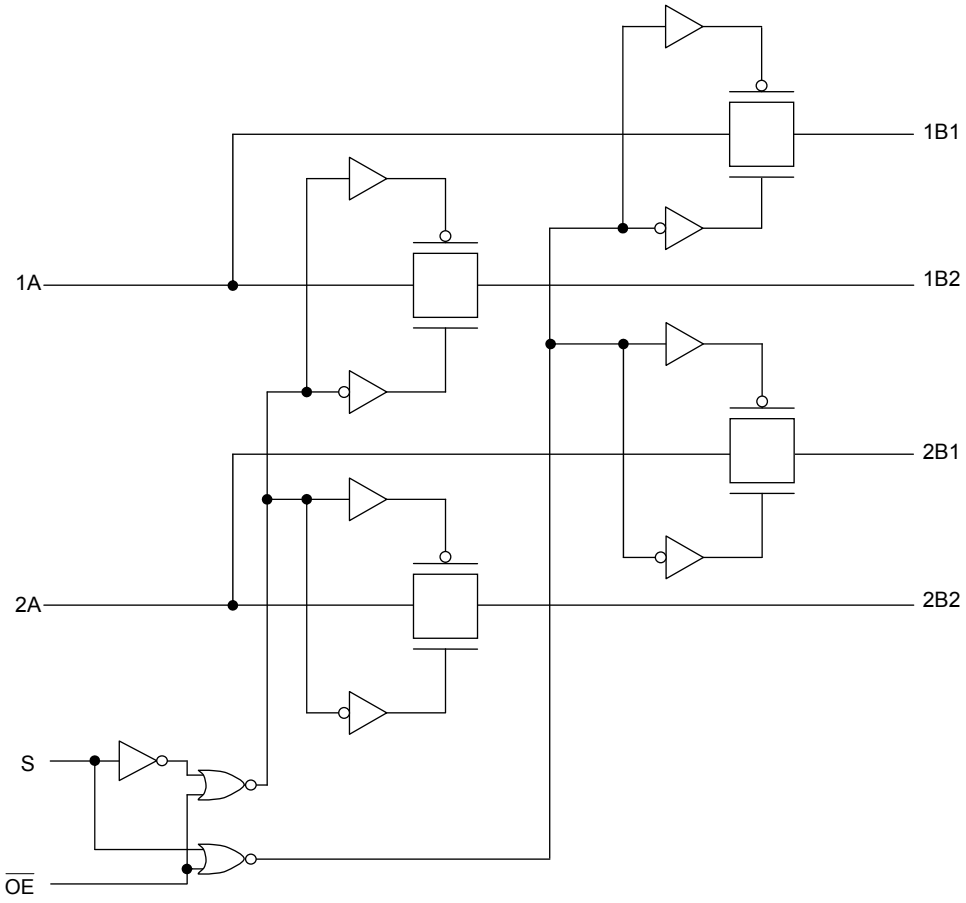

FTG (VQON16-P-0303-0.50)




## Truth Table

| Inputs | | Function |
|---|---|---|
| S | $\overline{OE}$ | |
| X | H | Disconnect |
| L | L | nA port = nB1 port |
| H | L | nA port = nB2 port |

## System Diagram



## Absolute Maximum Ratings (Note)

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Power supply range | | $V_{CC}$ | −0.5~4.6 | V |
| Control pin input voltage | | $V_{IN}$ | −0.5~4.6 | V |
| Switch terminal I/O voltage | | $V_S$ | −0.5~$V_{CC}$ + 0.5 | V |
| Clump diode current | Control input pin | $I_{IK}$ | −50 | mA |
| | Switch terminal | | ±50 | mA |
| Switch I/O current | | $I_S$ | 50 | mA |
| Power dissipation | | $P_D$ | 180 | mW |
| DC $V_{CC}$/GND current | | $I_{CC}/I_{GND}$ | ±100 | mA |
| Storage temperature | | $T_{stg}$ | −65~150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristic | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 1.65~3.6 | V |
| Control pin input voltage | $V_{IN}$ | 0~3.6 | V |
| Switch I/O voltage | $V_S$ | 0~$V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | −40~85 | °C |
| Input rise and fall time | dt/dv | 0~10 | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

## Electrical Characteristics

### DC Characteristics (Ta = −40~85°C)

| Parameter | | Symbol | Test Condition | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Input voltage | "H" level | $V_{IH}$ | — | 1.65~3.6 | 0.7 × $V_{CC}$ | — | — | V |
| | "L" level | $V_{IL}$ | — | 1.65~3.6 | — | — | 0.3 × $V_{CC}$ | |
| Input leakage current ( $\overline{OE}$ , S) | | $I_{IN}$ | $V_{IN}$ = 0~3.6V | 1.65~3.6 | — | — | ±1.0 | μA |
| Power-off leakage current | | $I_{OFF}$ | $\overline{OE}$ = 0~3.6 V | 0 | — | — | 1.0 | μA |
| Off-state leakage current (switch off) | | $I_{SZ}$ | A, B = 0~$V_{CC}$ , $\overline{OE}$ = $V_{CC}$ | 1.65~3.6 | — | — | ±1.0 | μA |
| On resistance (Note2) | | $R_{ON}$ | $V_{IS}$ = 0 V, $I_{IS}$ = 30 mA (Note1) | 3.0 | — | 9 | 13 | Ω |
| | | | $V_{IS}$ = 3.0 V, $I_{IS}$ = 30 mA (Note1) | 3.0 | — | 15 | 20 | |
| | | | $V_{IS}$ = 2.4 V, $I_{IS}$ = 15 mA (Note1) | 3.0 | — | 19 | 27 | |
| | | | $V_{IS}$ = 0 V, $I_{IS}$ = 24 mA (Note1) | 2.3 | — | 10 | 16 | |
| | | | $V_{IS}$ = 2.3 V, $I_{IS}$ = 24 mA (Note1) | 2.3 | — | 17 | 24 | |
| | | | $V_{IS}$ = 2.0 V, $I_{IS}$ = 15 mA (Note1) | 2.3 | — | 21 | 30 | |
| Increase in $I_{CC}$ per input | | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND, $I_{OUT}$ = 0 | 3.6 | — | — | 10 | μA |

Note1: All typical values are at Ta=25°C.

Note2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

### AC Characteristics (Ta = −40~85°C)

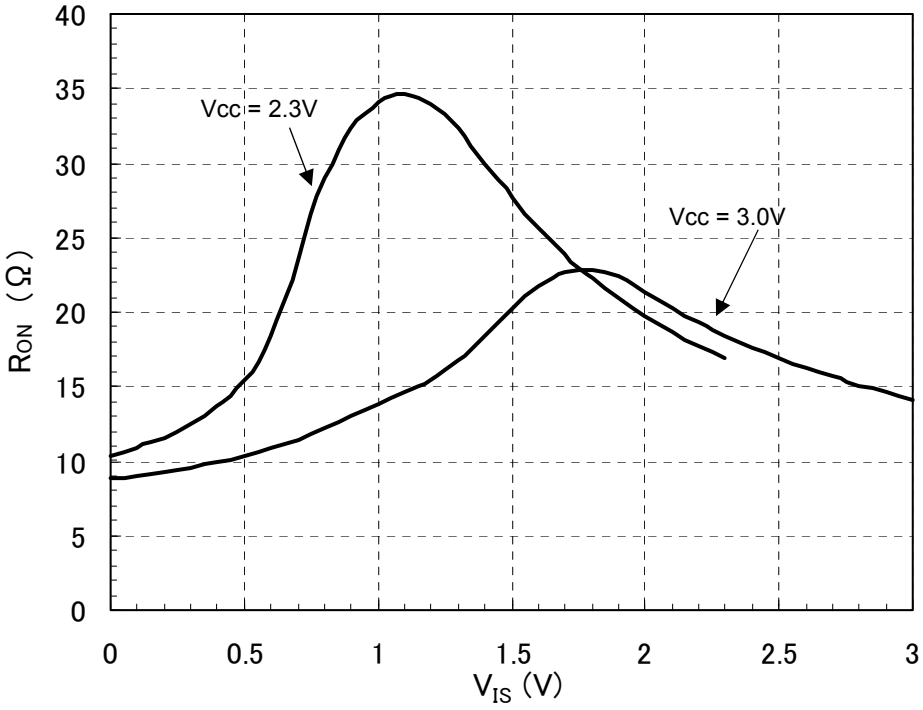
| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Propagation delay time (S to bus) | $t_{pLH}$ $t_{pHL}$ | Figure 1, Figure 2 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 11 | |
| Output enable time ( $\overline{OE}$ to bus) | $t_{pZL}$ $t_{pZH}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 11 | |
| Output enable time (S to bus) | $t_{pZL}$ $t_{pZH}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 11 | |
| Output disable time ( $\overline{OE}$ to bus) | $t_{pLZ}$ $t_{pHZ}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 11 | |
| Output disable time (S to bus) | $t_{pLZ}$ $t_{pHZ}$ | Figure 1, Figure 3 | 3.3 ± 0.3 | — | 6 | ns |
| | | | 2.5 ± 0.2 | — | 7 | |
| | | | 1.8 ± 0.15 | — | 11 | |

## Capacitive Characteristics (Ta = 25°C)

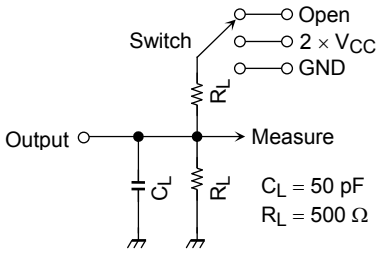
| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Unit |
|---|---|---|---|---|---|
| Control pin input capacitance ( $\overline{OE}$ , S) | $C_{IN}$ | | 3.0 | 3 | pF |
| Switch terminal capacitance (B1~2) | $C_{I/O}$ | $\overline{OE}$ = $V_{CC}$ (switch off) | 3.0 | 6 | pF |
| Switch terminal capacitance (A) | $C_{I/O}$ | $\overline{OE}$ = $V_{CC}$ (switch off) | 3.0 | 9 | pF |
| Switch terminal capacitance | $C_{I/O}$ | $\overline{OE}$ = GND (switch on) | 3.0 | 15 | pF |

Note: This parameter is guaranteed by design

## ・$R_{ON}$ Characteristic (typ.) Ta=25℃



## AC Test Circuit




| Parameter | Switch |
|---|---|
| $t_{pLH}$, $t_{pHL}$ | Open |
| $t_{pLZ}$, $t_{pZL}$ | 2 × $V_{CC}$ |
| $t_{pHZ}$, $t_{pZH}$ | GND |

**Figure 1**

## AC Waveform

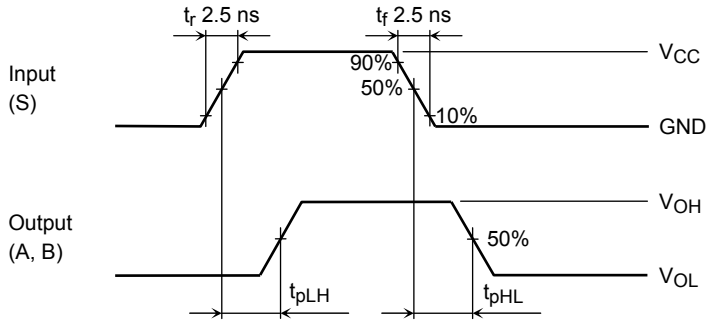



**Figure 2 $t_{pLH}$, $t_{pHL}$**

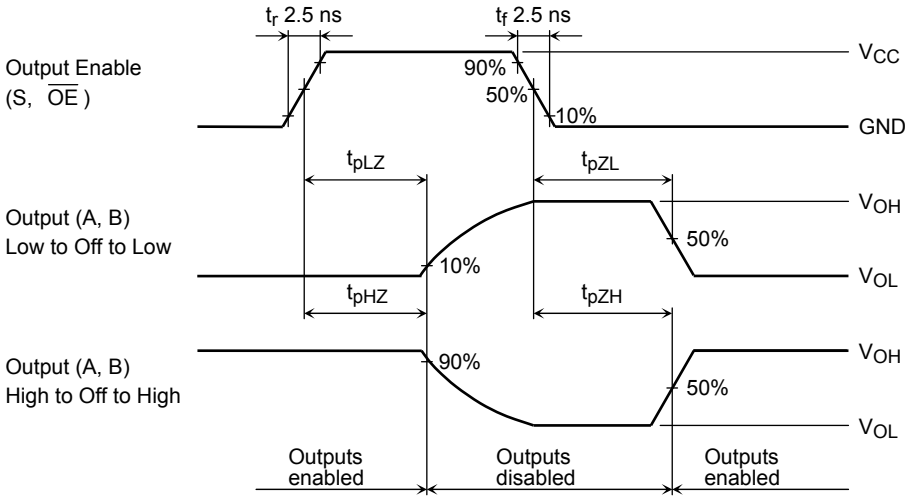



**Figure 3 $t_{pLZ}$, $t_{pHZ}$, $t_{pZL}$, $t_{pZH}$**

## Rise and Fall Times (tr / tf) of the TC7MBL6353S I/O Signals

The tr(out) and tf(out) values of the output signals are affected by the CR time constant of the input, which consists of the switch terminal capacitance ($C_{I/O}$) and the on-resistance ($R_{ON}$) of the input.

In practice, the tr(out) and tf(out) values are also affected by the circuit's capacitance and resistance components other than those of the TC7MBL6353S.

The tr / tf (out) values can be approximated as follows. (Figure 4 shows the test circuit.)

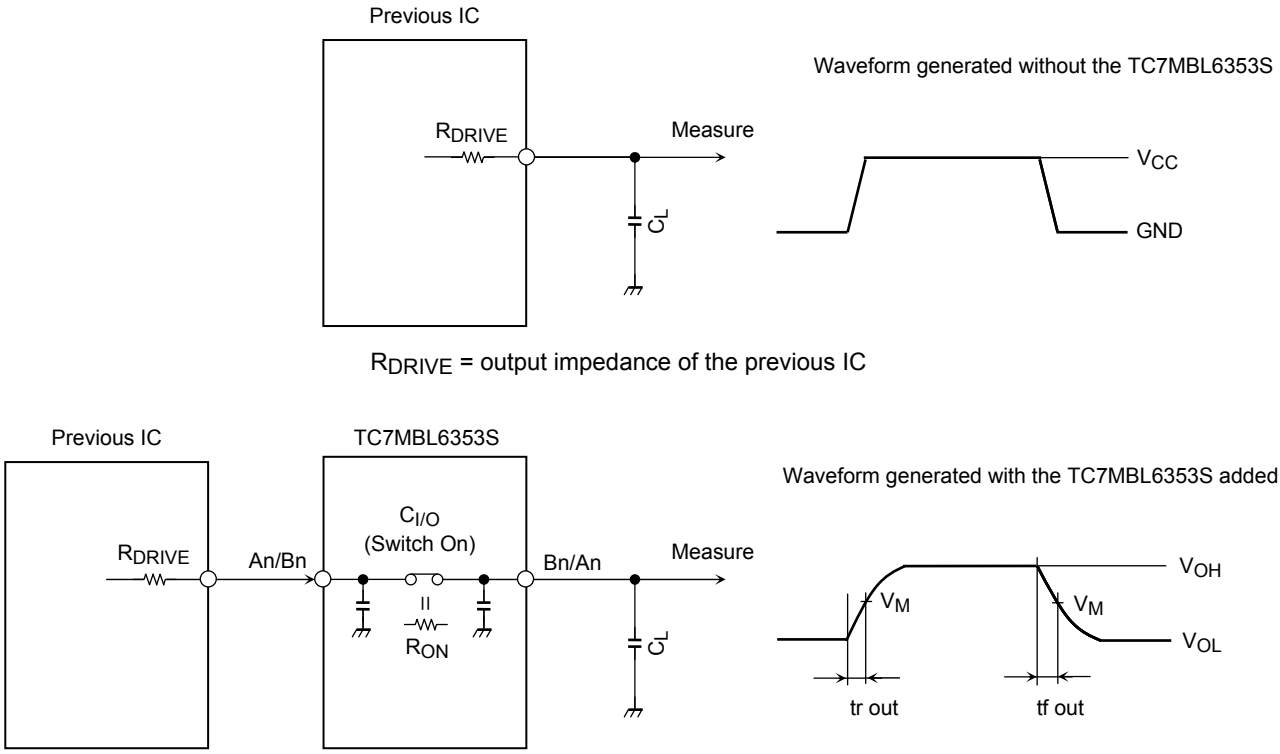
$$tr / tf\ out\ (approx) = -( C_{I/O} + C_L ) \cdot (R_{DRIVE} + R_{ON}) \cdot \ln( ( ( V_{OH} - V_{OL} ) - V_M ) / ( V_{OH} - V_{OL} ) )$$

where, $R_{DRIVE}$ is the output impedance of the previous-stage circuit.

Calculation example:

$$tr\ out\ (approx) = -( 15 + 15 )E\text{-}12 \cdot ( 120 + 9) \cdot \ln( ( ( 3.0 - 0 ) - 1.5 ) / ( 3.0 - 0 ) )$$
$$\approx 2.7\ ns$$

Calculation conditions:
$V_{CC}$ = 3.0V , $C_L$ = 15pF , $R_{DRIVE}$ = 120Ω(output impedance of the previous IC), $V_M$ = 1.5V ($V_{CC}$ / 2)
Output of the previous IC = digital (i.e., high-level voltage = $V_{CC}$; low-level voltage = GND)

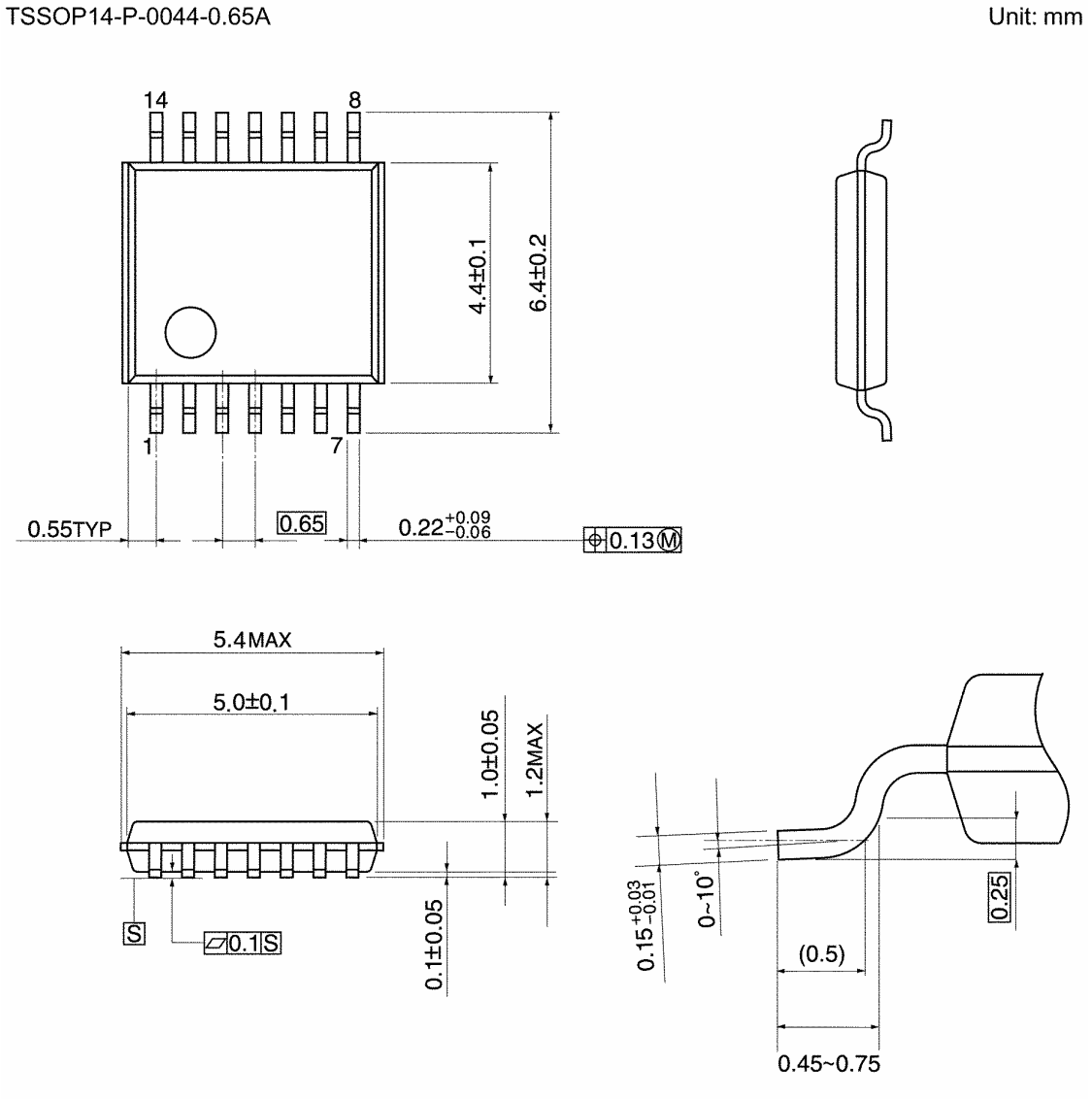



| Parameter | $V_{CC}$ | | |
|---|---|---|---|
| | 3.3 ± 0.3 V | 2.5 ± 0.2 V | 1.8 ± 0.15 V |
| $V_M$ | $V_{CC}$ / 2 | $V_{CC}$ / 2 | $V_{CC}$ / 2 |

**Figure 4 Test Circuit**

## Package Dimensions

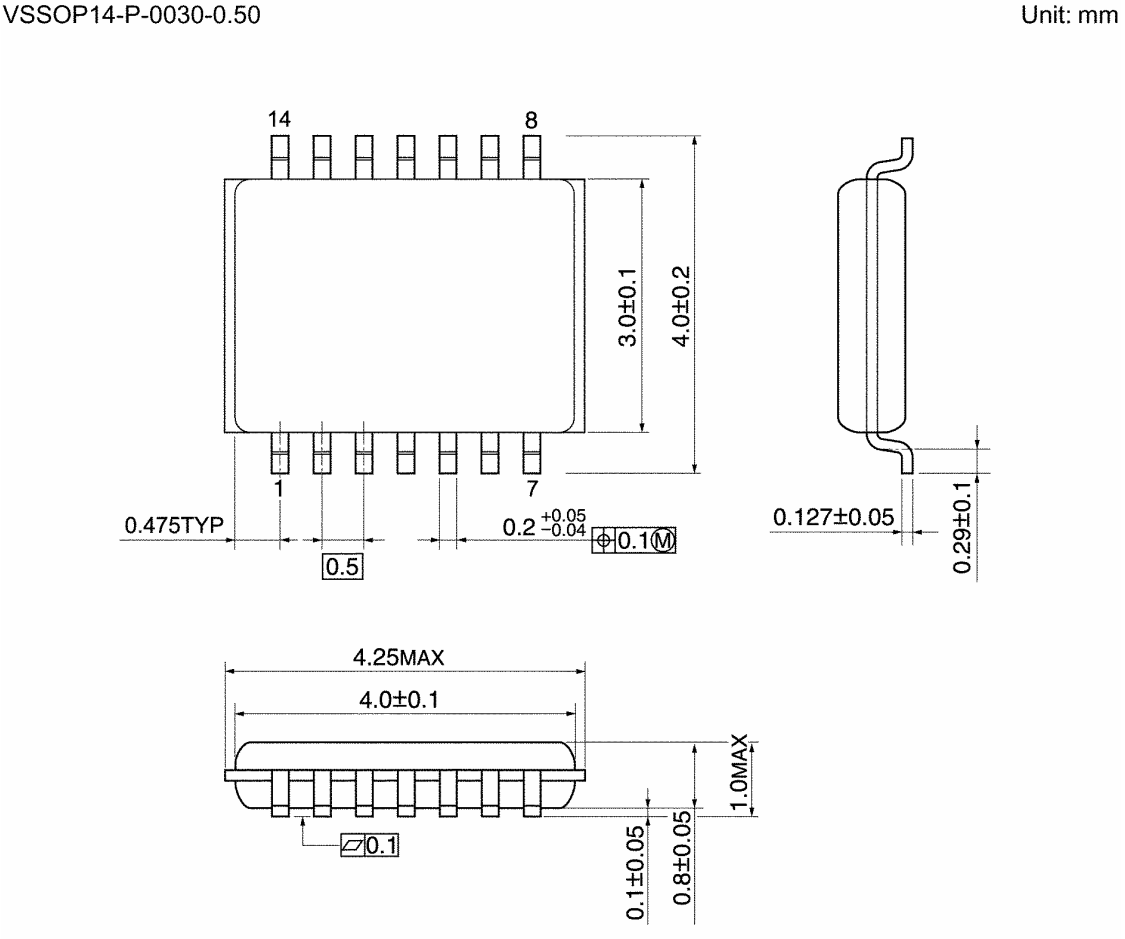
TSSOP14-P-0044-0.65A Unit: mm




Weight: 0.06 g (typ.)

## Package Dimensions

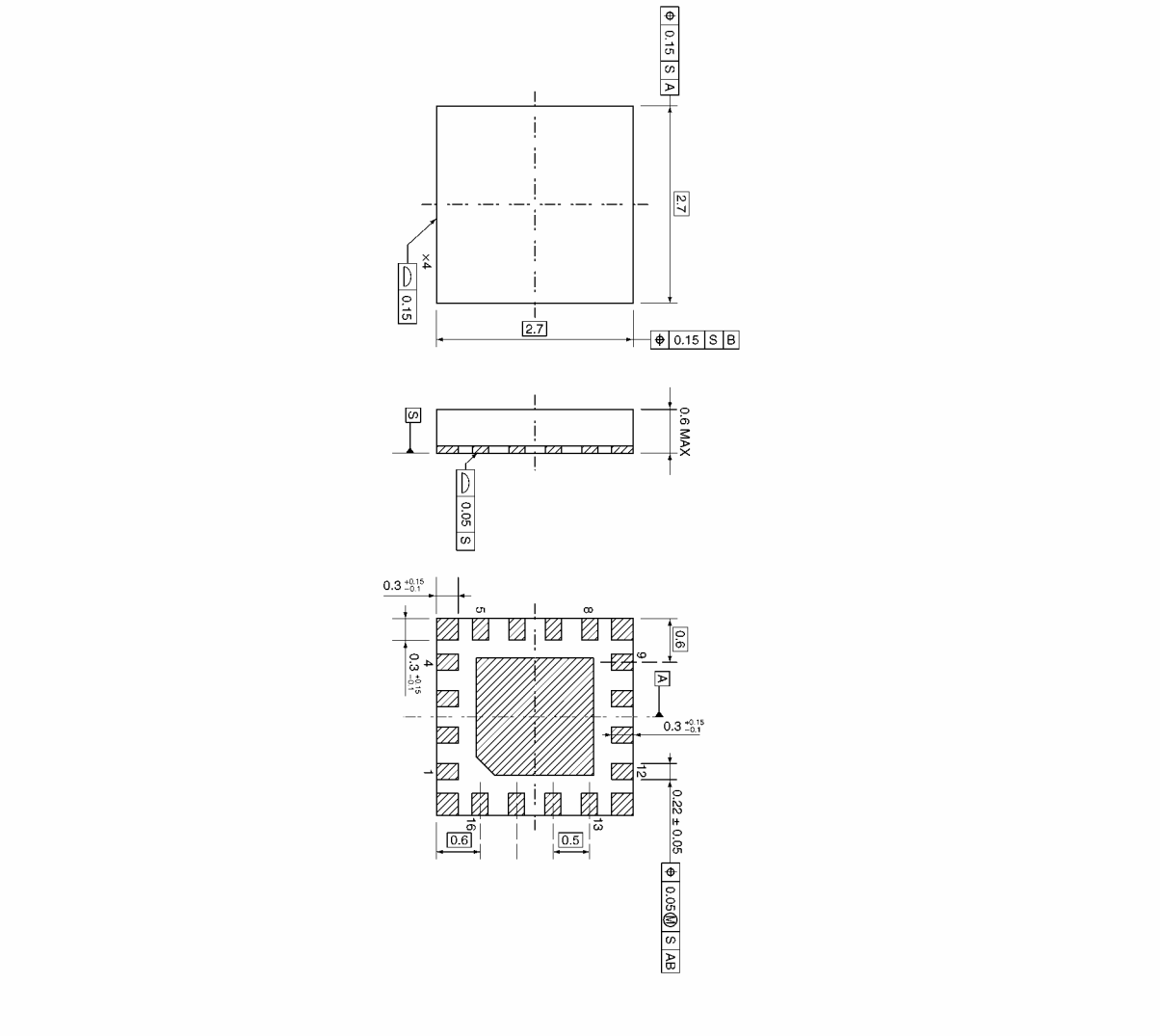
VSSOP14-P-0030-0.50 Unit: mm




Weight: 0.02 g (typ.)

## Package Dimensions

VQON16-P-0303-0.50 Unit: mm




Weight: 0.013 g (typ.)

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