## TC7MZ4051FK,TC7MZ4052FK,TC7MZ4053FK

## TC7MZ4051FK 8-Channel Analog Multiplexer/Demultiplexer <br> TC7MZ4052FK Dual 4-Channel Analog Multiplexer/Demultiplexer

TC7MZ4053FK Triple 2-Channel Analog Multiplexer/Demultiplexer

The TC7MZ4051/4052/4053FK are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The TC7MZ4051/4052/4053FK offer analog/digital signal selection as well as mixed signals. The 4051 has an 8 -channel configuration, the 4052 has an 4 -channel $\times 2$ configuration, and


VSSOP $16-P-0030-0.50$

Weight: 0.02 g (typ.) the 4053 has a 2 -channel $\times 3$ configuration.

The switches for each channel are turned ON by the control pin digital signals.

Although the control signal logical amplitude ( $\mathrm{V}_{\mathrm{CC}}-\mathrm{GND}$ ) is small, the device can perform large-amplitude ( $\mathrm{VCC}_{\mathrm{C}}-\mathrm{VEE}$ ) signal switching.

For example, if $\mathrm{V}_{\mathrm{CC}}=3 \mathrm{~V}, \mathrm{GND}=0 \mathrm{~V}$, and VEE $=-3 \mathrm{~V}$, signals between -3 V and +3 V can be switched from the logical circuit using a single 3 V power supply.

All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the VCC). As a result, for example, 5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the TC7MZ4051/4052/4053FK can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

## Features

- Low ON resistance: $\mathrm{R}_{\mathrm{on}}=22 \Omega$ (typ.) ( $\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{EE}}=3 \mathrm{~V}$ )

$$
\mathrm{R}_{\mathrm{on}}=15 \Omega \text { (typ.) }(\mathrm{VCC}-\mathrm{VEE}=6 \mathrm{~V})
$$

- High speed: $\mathrm{t}_{\mathrm{pd}}=3 \mathrm{~ns}$ (typ.) $\left(\mathrm{V}_{\mathrm{CC}}=3.0 \mathrm{~V}\right)$
- Low power dissipation: $\mathrm{ICC}_{C}=4 \mu \mathrm{~A}(\max )\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right)$
- Input level: VIL $=0.8 \mathrm{~V}(\max )\left(\mathrm{VCC}_{\mathrm{C}}=3 \mathrm{~V}\right)$

$$
\mathrm{V}_{\mathrm{IH}}=2.0 \mathrm{~V}(\mathrm{~min})\left(\mathrm{V}_{\mathrm{CC}}=3 \mathrm{~V}\right)
$$

- Power down protection is provided on all control inputs
- Pin and function compatible with $74 \mathrm{HC} 4051 / 4052 / 4053$


## Pin Assignment (top view)



Truth Table

| Control Inputs |  |  |  | "ON" Channel |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Inhibit | C* | B | A | MZ4051FK | MZ4052FK | MZ4053FK |
| L | L | L | L | 0 | OX, OY | 0X, OY, OZ |
| L | L | L | H | 1 | 1X, 1Y | 1X, OY, OZ |
| L | L | H | L | 2 | 2X, 2Y | 0X, 1Y, 0Z |
| L | L | H | H | 3 | $3 X, 3 Y$ | 1X, 1Y, 0Z |
| L | H | L | L | 4 | - | 0X, 0Y, 1Z |
| L | H | L | H | 5 | - | 1X, 0Y, 1Z |
| L | H | H | L | 6 | - | 0X, 1Y, 1Z |
| L | H | H | H | 7 | - | 1X, 1Y, 1Z |
| H | X | X | X | None | None | None |

X: Don't care, *: Except MZ4052FK

## System Diagram

## TC7MZ4051FK



## TC7MZ4052FK



## TC7MZ4053FK



Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Power supply voltage | $\mathrm{V}_{\mathrm{CC}}$ | $-0.5 \sim 7.0$ | V |
|  | $\mathrm{~V}_{\mathrm{CC}} \sim \mathrm{V}_{\mathrm{EE}}$ | $-0.5 \sim 7.0$ |  |
| Control input voltage | $\mathrm{V}_{\mathrm{IN}}$ | $-0.5 \sim 7.0$ | V |
| Switch I/O voltage | $\mathrm{V}_{\mathrm{I} / \mathrm{O}}$ | $\mathrm{V}_{\mathrm{EE}}-0.5 \sim \mathrm{~V}_{\mathrm{CC}}+0.5$ | V |
| Input diode current | $\mathrm{I}_{\mathrm{IK}}$ | -20 | mA |
| I/O diode current | $\mathrm{I}_{\mathrm{IOK}}$ | $\pm 20$ | mA |
| Switch through current | $\mathrm{I}_{\mathrm{T}}$ | $\pm 25$ | mA |
| DC $\mathrm{V}_{\mathrm{CC}}$ or ground current | $\mathrm{I}_{\mathrm{CC}}$ | $\pm 50$ | mW |
| Power dissipation | $\mathrm{P}_{\mathrm{D}}$ | 180 | ${ }^{\circ} \mathrm{C}$ |
| Storage temperature | $\mathrm{T}_{\mathrm{stg}}$ | $-65 \sim 150$ |  |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
| :---: | :---: | :---: | :---: |
| Power supply voltage | $V_{C C}$ | 2~6 | V |
|  | $V_{\text {EE }}$ | -4~0 |  |
|  | $\mathrm{V}_{\mathrm{CC}} \sim \mathrm{V}_{\mathrm{EE}}$ | 2~6 |  |
| Input voltage | $\mathrm{V}_{\text {IN }}$ | 0~6.0 | V |
| Switch I/O voltage | $\mathrm{V}_{1 / \mathrm{O}}$ | $\mathrm{V}_{\mathrm{EE}} \sim \mathrm{V}_{\mathrm{CC}}$ | V |
| Operating temperature | Topr | -40~85 | ${ }^{\circ} \mathrm{C}$ |
| Input rise and fall time | dt/dv | 0~100 ( $\left.\mathrm{V}_{\mathrm{CC}}=3.3 \pm 0.3 \mathrm{~V}\right)$ | $\mathrm{ns} / \mathrm{V}$ |
|  |  | $0 \sim 20\left(\mathrm{~V}_{\mathrm{CC}}=5 \pm 0.5 \mathrm{~V}\right)$ |  |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either $\mathrm{V}_{\mathrm{cc}}$ or GND.

## Electrical Characteristics

DC Electrical Characteristics

| Characteristics |  | Symbol | Test Condition |  |  | $\mathrm{Ta}=25^{\circ} \mathrm{C}$ |  |  | $\mathrm{Ta}=-40 \sim 85^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{\mathrm{EE}}(\mathrm{V})$ |  | $V_{C C}(\mathrm{~V})$ | Min | Typ. | Max | Min | Max |  |
| Input voltage | High-level |  | $\mathrm{V}_{\mathrm{IH}}$ | - |  | 2.0 | 1.5 | - | - | 1.5 | - | V |
|  |  | 3.0 |  |  |  | 2.0 | - | - | 2.0 | - |  |  |
|  |  | 4.5 |  |  |  | 3.15 | - | - | 3.15 | - |  |  |
|  |  | 6.0 |  |  |  | 4.2 | - | - | 4.2 | - |  |  |
|  | Low-level | VIL | - |  | 2.0 | - | - | 0.5 | - | 0.5 |  |  |
|  |  |  |  |  | 3.0 | - | - | 0.8 | - | 0.8 |  |  |
|  |  |  |  |  | 4.5 | - | - | 1.35 | - | 1.35 |  |  |
|  |  |  |  |  | 6.0 | - | - | 1.8 | - | 1.8 |  |  |
| ON resistance |  | RON | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{I} / \mathrm{O}}=\mathrm{V}_{\mathrm{CC}} \text { to } \mathrm{V}_{\mathrm{EE}} \\ & \mathrm{I}_{\mathrm{I} / \mathrm{O}}=2 \mathrm{~mA} \end{aligned}$ | GND | 2.0 | - | 200 | - | - | - | $\Omega$ |  |
|  |  | GND |  | 3.0 | - | 45 | 86 | - | 108 |  |  |
|  |  | GND |  | 4.5 | - | 24 | 37 | - | 46 |  |  |
|  |  | -3.0 |  | 3.0 | - | 17 | 26 | - | 33 |  |  |
|  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{I} / \mathrm{O}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{V}_{\mathrm{EE}} \\ & \mathrm{I}_{\mathrm{I} / \mathrm{O}}=2 \mathrm{~mA} \end{aligned}$ | GND | 2.0 | - | 28 | 73 | - | 84 |  |  |
|  |  | GND | 3.0 | - | 22 | 38 | - | 44 |  |  |
|  |  | GND | 4.5 | - | 17 | 27 | - | 31 |  |  |
|  |  | -3.0 | 3.0 | - | 15 | 24 | - | 28 |  |  |
| Difference of ON resistance between switches |  |  | $\Delta \mathrm{R}_{\text {ON }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \\ & \mathrm{~V}_{\mathrm{I} / \mathrm{O}}=\mathrm{V}_{\mathrm{CC}} \text { to } \mathrm{V}_{\mathrm{EE}} \\ & \mathrm{I}_{\mathrm{I} / \mathrm{O}}=2 \mathrm{~mA} \end{aligned}$ | GND | 2.0 | - | 10 | 25 | - | 35 | $\Omega$ |
|  |  | GND |  |  | 3.0 | - | 5 | 15 | - | 20 |  |  |
|  |  | GND |  |  | 4.5 | - | 5 | 13 | - | 18 |  |  |
|  |  | -3.0 |  |  | 3.0 | - | 5 | 10 | - | 15 |  |  |
| Input/Output leakage current (switch OFF) |  |  | IOFF | $\begin{aligned} & V_{\mathrm{OS}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{GND} \\ & \mathrm{~V}_{\text {IS }}=\mathrm{GND} \text { to } \mathrm{V}_{\mathrm{CC}} \\ & \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {IL }} \text { or } \mathrm{V}_{\text {IH }} \end{aligned}$ | GND | 3.0 | - | - | $\pm 0.25$ | - | $\pm 2.5$ | $\mu \mathrm{A}$ |
|  |  | -3.0 |  |  | 3.0 | - | - | $\pm 0.5$ | - | $\pm 5.0$ |  |  |
| Input/Output leakage current (switch ON, output open) |  |  | IIN | $\begin{aligned} & V_{\mathrm{OS}}=\mathrm{V}_{\mathrm{CC}} \text { or } \mathrm{GND} \\ & \mathrm{~V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IL}} \text { or } \mathrm{V}_{\mathrm{IH}} \end{aligned}$ | GND | 3.0 | - | - | $\pm 0.25$ | - | $\pm 2.5$ | $\mu \mathrm{A}$ |
|  |  | -3.0 |  |  | 3.0 | - | - | $\pm 0.5$ | - | $\pm 5.0$ |  |  |
| Control input c | rrent | IIN | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}$ or GND | GND | 6.0 | - | - | $\pm 0.1$ | - | $\pm 0.1$ | $\mu \mathrm{A}$ |  |
| Quiescent supply current |  | ICC | $\mathrm{V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{CC}}$ or GND | GND | 3.0 | - | - | 4.0 | - | 40.0 | $\mu \mathrm{A}$ |  |
|  |  | -3.0 |  | 3.0 | - | - | 8.0 | - | 80.0 |  |  |

AC Electrical Characteristics ( $\mathrm{C}_{\mathrm{L}}=\mathbf{5 0} \mathbf{~ p F}$, Input: $\mathrm{t}_{\mathbf{r}}=\mathrm{t}_{\mathbf{f}}=\mathbf{3} \mathbf{n s}, \mathrm{GND}=\mathbf{0} \mathbf{V}$ )

| Characteristics | Symbol | Test Condition |  |  |  | $\mathrm{Ta}=25^{\circ} \mathrm{C}$ |  |  | $\mathrm{Ta}=-40 \sim 85^{\circ} \mathrm{C}$ |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | $\mathrm{V}_{\mathrm{EE}}(\mathrm{V})$ | $\mathrm{V}_{\mathrm{Cc}}(\mathrm{V})$ | Min | Typ. | Max | Min | Max |  |
| Phase difference between input and output | ¢I/O | All types |  | GND | 2.0 | - | 3.2 | 6.0 | - | 6.9 | ns |
|  |  |  |  | GND | 3.0 | - | 1.8 | 3.0 | - | 3.5 |  |
|  |  |  |  | GND | 4.5 | - | 1.3 | 1.8 | - | 2.1 |  |
|  |  |  |  | -3.0 | 3.0 | - | 1.1 | 1.3 | - | 1.5 |  |
| Output enable time | $\begin{aligned} & \mathrm{t}_{\mathrm{pzLL}} \\ & \mathrm{t}_{\mathrm{pzH}} \end{aligned}$ | Figure 1 ( Note 1) |  | GND | 2.0 | - | 9.0 | 17 | - | 20 | ns |
|  |  |  |  | GND | 3.0 | - | 5.7 | 9.0 | - | 11 |  |
|  |  |  |  | GND | 4.5 | - | 4.5 | 6.0 | - | 7.0 |  |
|  |  |  |  | -3.0 | 3.0 | - | 5.8 | 8.0 | - | 10 |  |
| Output disable time | $\begin{gathered} \mathrm{tplZ}^{\mathrm{t}_{\mathrm{pHZ}}} \end{gathered}$ | Figure | 1 (Note 1) | GND | 2.0 | - | 13.5 | 21 | - | 25 | ns |
|  |  |  |  | GND | 3.0 | - | 11.3 | 15 | - | 18 |  |
|  |  |  |  | GND | 4.5 | - | 10.3 | 12 | - | 14 |  |
|  |  |  |  | -3.0 | 3.0 | - | 10.9 | 13 | - | 15 |  |
| Control input capacitance | $\mathrm{C}_{\text {in }}$ | All type | s (Note 2) | - | - | - | 5 | 10 | - | 10 | pF |
| COMMON terminal capacitance | $\mathrm{ClS}_{\text {I }}$ | 4051 | Figure 2 (Note 2) | -3.0 | 3.0 | - | 11 | 25 | - | 25 | pF |
|  |  | 4052 |  |  |  |  | 9 | 20 |  | 20 |  |
|  |  | 4053 |  |  |  |  | 7 | 15 |  | 15 |  |
| SWITCH terminal capacitance | Cos | 4051 | Figure 2 <br> (Note 2) | -3.0 | 3.0 | - | 6 | 13 | - | 13 | pF |
|  |  | 4052 |  |  |  |  | 6 | 13 |  | 13 |  |
|  |  | 4053 |  |  |  |  | 6 | 13 |  | 13 |  |
| Feedthrough capacitance | ClOS | 4051 | Figure 2 (Note 2) | -3.0 | 3.0 | - | 3 | 6 | - | 6 | pF |
|  |  | 4052 |  |  |  |  | 3 | 6 |  | 6 |  |
|  |  | 4053 |  |  |  |  | 3 | 6 |  | 6 |  |
| Power dissipation capacitance | CPD | 4051 | Figure 2 (Note 3) | GND | 6.0 | - | 14 | - | - | - | pF |
|  |  | 4052 |  |  |  |  | 24 |  |  |  |  |
|  |  | 4053 |  |  |  |  | 18 |  |  |  |  |

Note 1: $\mathrm{R}_{\mathrm{L}}=1 \mathrm{k} \Omega$
Note 2: $\mathrm{C}_{\mathrm{in}}, \mathrm{C}_{\mathrm{IS}}, \mathrm{C}_{\mathrm{OS}}$ and $\mathrm{C}_{\mathrm{IOS}}$ are guaranteed by the design.
Note 3: $C_{P D}$ is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$\operatorname{ICC}(\mathrm{opr})=\mathrm{C}_{\text {PD }} \cdot \mathrm{V}_{\mathrm{CC}} \cdot \mathrm{f}_{\mathrm{IN}}+\mathrm{I}_{\mathrm{CC}}$
*Analog Switch Characteristics (GND = $0 \mathrm{~V}, \mathrm{Ta}=25^{\circ} \mathrm{C}$ )

*: These characteristics are determined by design of devices.



Figure 1 tpLZ, $t_{p H z}, t_{p Z L}, t_{p z H}$


Figure $2 \quad \mathrm{C}_{\text {Ios }}, \mathrm{C}_{\text {IS }}, \mathrm{C}_{\text {os }}$


Figure 3 Frequency Response (switch on)


Figure 4 Feedthrough


Figure 5 Cross Talk (control input to output signal)


Figure 6 Cross Talk (between any two switches)

## Package Dimensions

VSSOP16-P-0030-0.50


Weight: 0.02 g (typ.)

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