



TSM12N02

N-Channel Enhancement Mode MOSFET

TO-252



Pin assignment:

- 1. Gate
- 2. Drain
- 3. Source

$V_{DS} = 20V$

$I_D = 12A$

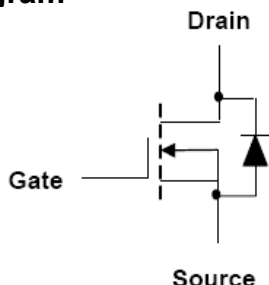
$R_{DS(on)}, V_{GS} @ 10V, I_{DS}@8A = 30m\Omega$

$R_{DS(on)}, V_{GS} @ 4.5V, I_{DS}@6A = 40m\Omega$

Features

- ◇ Advanced trench process technology
- ◇ Low gate charge
- ◇ High Density Cell Design for Ultra Low On-Resistance
- ◇ Fully Characterized Avalanche Voltage and Current
- ◇ High performance technology for low $R_{DS(ON)}$
- ◇ Fast switching speed

Block Diagram



Ordering Information

Part No.	Packing	Package
TSM12N02CP	Tape & Reel	TO-252

Absolute Maximum Rating ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	20	V	
Gate-Source Voltage	V_{GS}	± 12	V	
Continuous Drain Current	I_D	12	A	
Pulsed Drain Current	I_{DM}	30		
Maximum Power Dissipation	P_D	$T_A = 25^\circ C$	1.3	W
		$T_A = 100^\circ C$	2	W/ $^\circ C$
Operating Junction Temperature	T_J	+150	$^\circ C$	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ C$	

Thermal Performance

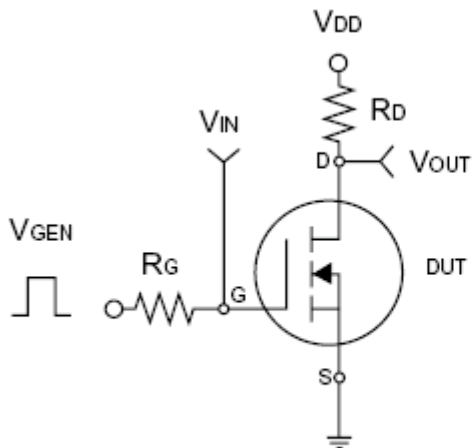
Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction-to-case Thermal Resistance	$R_{\theta jc}$	2.2	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	50	

Note: 1. Maximum DC current limited by the package
 2. 1-in² 2oz Cu PCB board

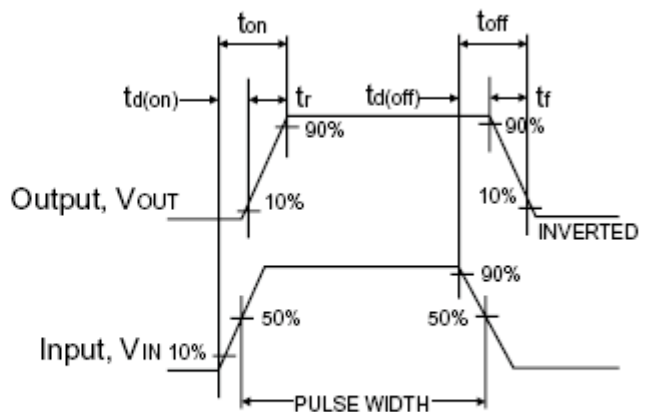


Electrical Characteristics						
$T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	BV_{DSS}	20	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 8\text{A}$	$R_{DS(ON)}$	--	21	30	m Ω
Drain-Source On-State Resistance	$V_{GS} = 4.5\text{V}, I_D = 6\text{A}$	$R_{DS(ON)}$	--	30	40	m Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	0.6	--	--	V
Zero Gate Voltage Drain Current	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	1.0	μA
Gate Body Leakage	$V_{GS} = \pm 12\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Forward Transconductance	$V_{DS} = 10\text{V}, I_D = 6\text{A}$	g_{fs}	7	13	--	S
Dynamic						
Total Gate Charge	$V_{DS} = 10\text{V}, I_D = 6\text{A}, V_{GS} = 4.5\text{V}$	Q_g	--	7.1	--	nC
Gate-Source Charge		Q_{gs}	--	1.96	--	
Gate-Drain Charge		Q_{gd}	--	2.94	--	
Turn-On Delay Time	$V_{DD} = 10\text{V}, R_L = 10\Omega, I_D = 1\text{A}, V_{GEN} = 4.5\text{V}, R_G = 6\Omega$	$t_{d(on)}$	--	4.9	--	nS
Turn-On Rise Time		t_r	--	2.6	--	
Turn-Off Delay Time		$t_{d(off)}$	--	15.7	--	
Turn-Off Fall Time		t_f	--	14	--	
Input Capacitance	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}, f = 1.0\text{MHz}$	C_{iss}	--	620	--	pF
Output Capacitance		C_{oss}	--	124	--	
Reverse Transfer Capacitance		C_{rss}	--	95	--	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	1.7	A
Diode Forward Voltage	$I_S = 1.7\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.2	V

Note: 1. pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
 2. Negligible, Dominated by circuit inductance.

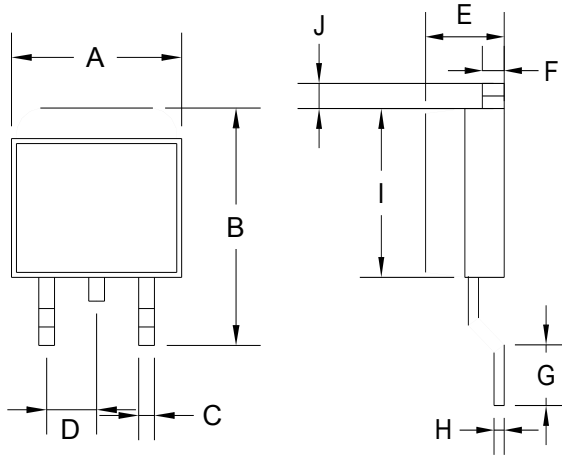


Switching Test Circuit



Switchin Waveforms

TO-252 Mechanical Drawing



DIM	TO-252 DIMENSION			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.570	6.840	0.259	0.269
B	9.250	10.400	0.364	0.409
C	0.550	0.700	0.022	0.028
D	2.560	2.670	0.101	0.105
E	2.300	2.390	0.090	0.094
F	0.490	0.570	0.019	0.022
G	1.460	1.580	0.057	0.062
H	0.520	0.570	0.020	0.022
I	5.340	5.550	0.210	0.219
J	1.460	1.640	0.057	0.065