

**SOP-8**

**Pin Definition:**

1. Source
2. Source
3. Source
4. Gate
- 5, 6, 7, 8. Drain

**PRODUCT SUMMARY**

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
25	15 @ $V_{GS} = 10V$	10
	21 @ $V_{GS} = 4.5V$	8

**Features**

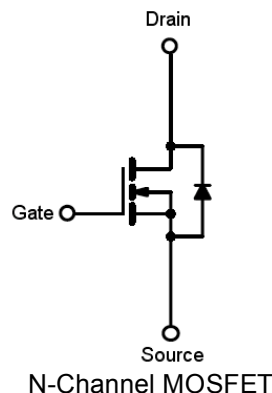
- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

**Application**

- Load Switch
- Dc-DC Converters and Motors Drivers

**Ordering Information**

Part No.	Package	Packing
TSM4410CS RL	SOP-8	2.5Kpcs / 13" Reel

**Block Diagram**

**Absolute Maximum Rating** ( $T_a = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	25	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	25	A
Pulsed Drain Current	$I_{DM}$	50	A
Continuous Source Current (Diode Conduction) <sup>a,b</sup>	$I_S$	2.3	A
Maximum Power Dissipation	$P_D$	$T_a = 25^\circ C$	2
		$T_a = 70^\circ C$	1.3
Operating Junction Temperature	$T_J$	+150	$^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta JC}$	30	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	50	$^\circ C/W$

**Notes:**

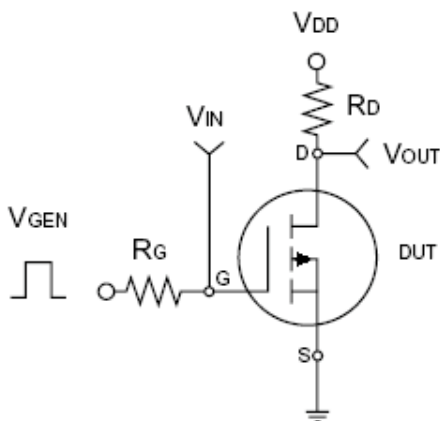
- a. Maximum DC current limited by the package
- b. Surface Mounted on 1" x 1" FR4 Board,  $t \leq 10$  sec.

### Electrical Specifications (Ta = 25°C unless otherwise noted)

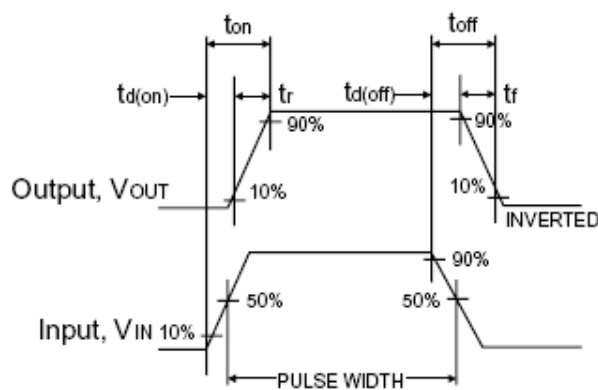
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	25	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.0	1.9	3.0	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = 25V, V_{GS} = 0V$	$I_{DSS}$	--	--	1.0	$\mu A$
On-State Drain Current	$V_{DS} \geq 5V, V_{GS} = 10V$	$I_{D(ON)}$	25	--	--	A
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 10A$	$R_{DS(ON)}$	--	13	15	m $\Omega$
	$V_{GS} = 4.5V, I_D = 8A$		--	18	21	
Forward Transconductance	$V_{DS} = 15V, I_D = 15A$	$g_{fs}$	--	25	--	S
Diode Forward Voltage	$I_S = 2.3A, V_{GS} = 0V$	$V_{SD}$	--	0.85	1.3	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$V_{DS} = 15V, I_D = 10A,$ $V_{GS} = 10V$	$Q_g$	--	14.7	26	nC
Gate-Source Charge		$Q_{gs}$	--	2.5	--	
Gate-Drain Charge		$Q_{gd}$	--	3	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	921	--	pF
Output Capacitance		$C_{oss}$	--	208.7	--	
Reverse Transfer Capacitance		$C_{rss}$	--	108.2	--	
<b>Switching<sup>c</sup></b>						
Turn-On Delay Time	$V_{DD} = 15V, R_L = 15\Omega,$ $I_D = 1A, V_{GEN} = 10V,$ $R_G = 16\Omega$	$t_{d(on)}$	--	20.2	--	ns
Turn-On Rise Time		$t_r$	--	5.9	--	
Turn-Off Delay Time		$t_{d(off)}$	--	49.5	--	
Turn-Off Fall Time		$t_f$	--	16.7	--	

Notes:

- a. pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

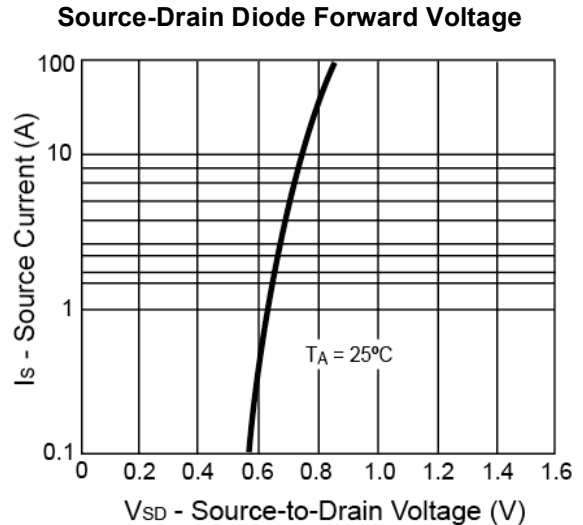
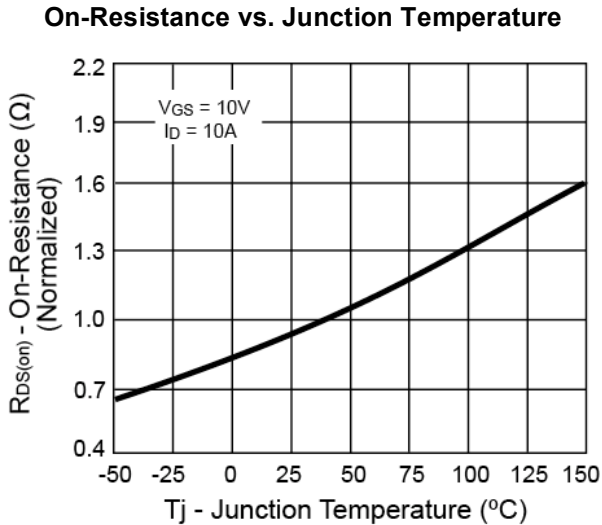
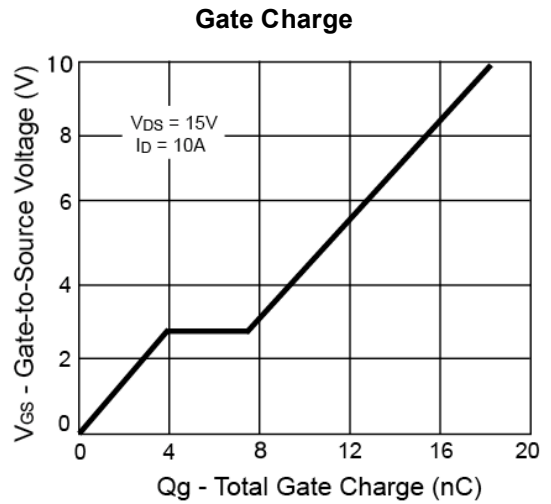
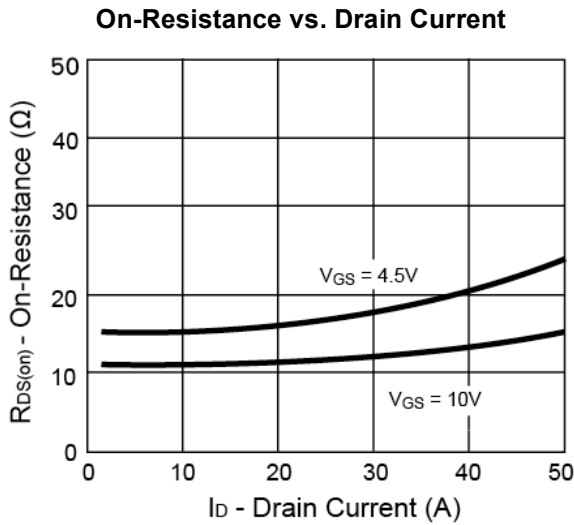
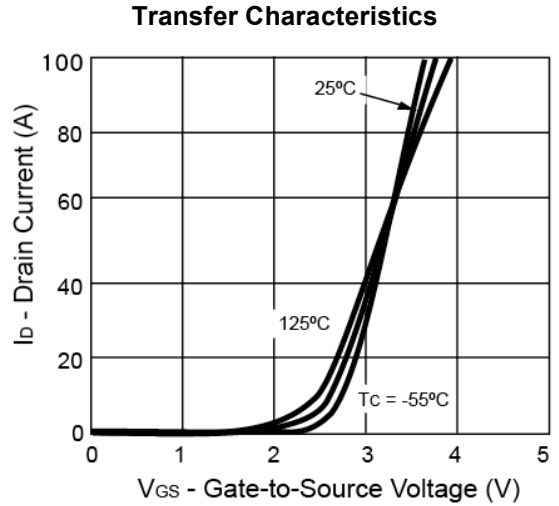
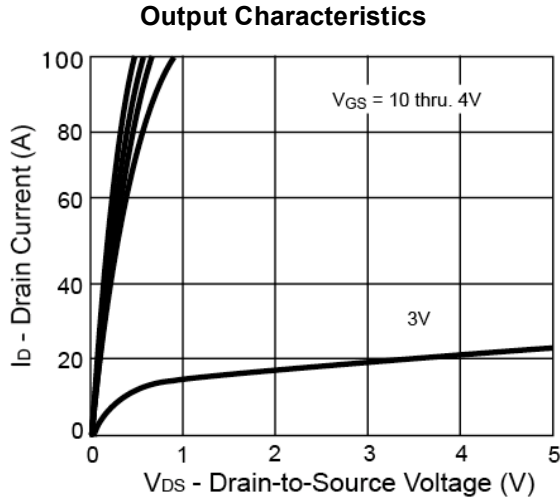


Switching Test Circuit



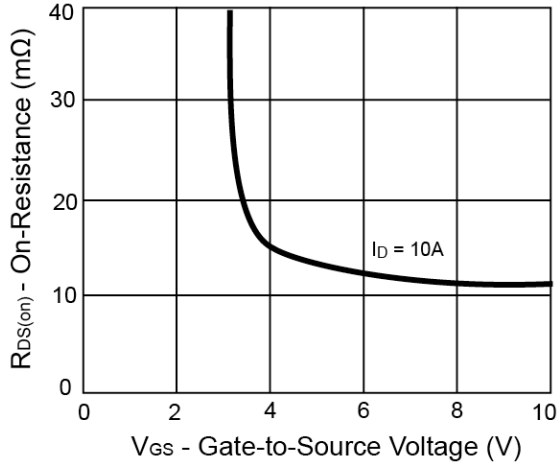
Switchin Waveforms

**Electrical Characteristics Curve** (Ta = 25°C, unless otherwise noted)

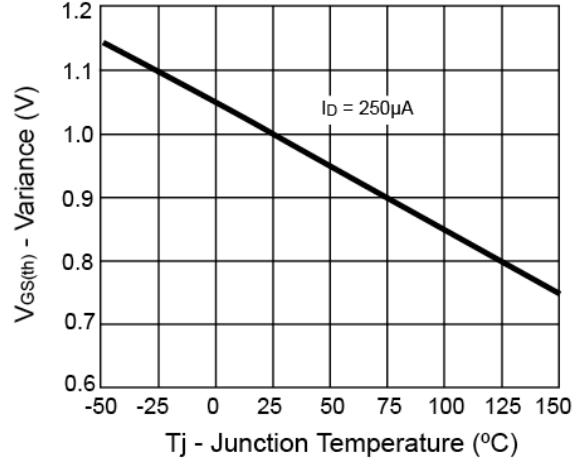


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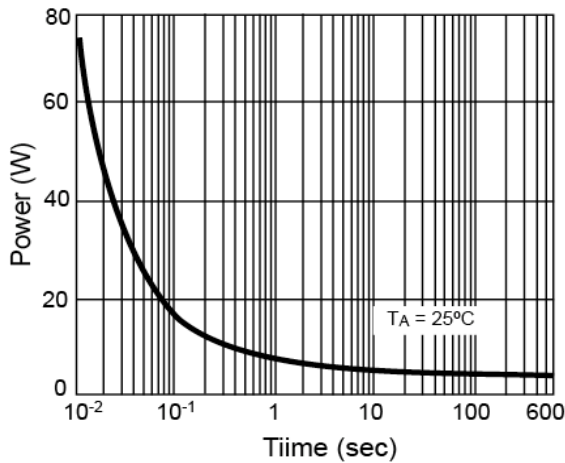
**On-Resistance vs. Gate-Source Voltage**



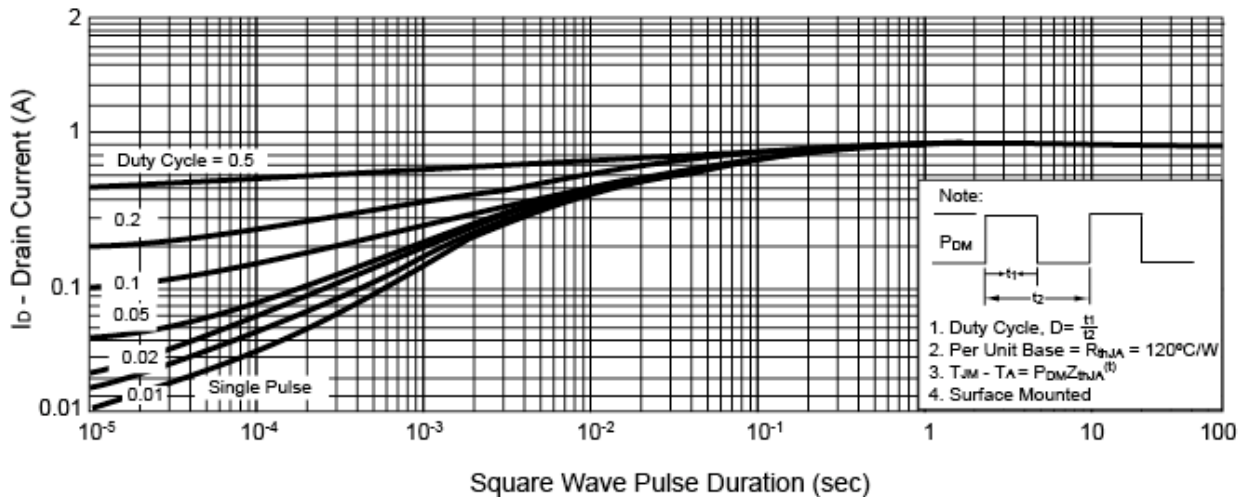
**Threshold Voltage**



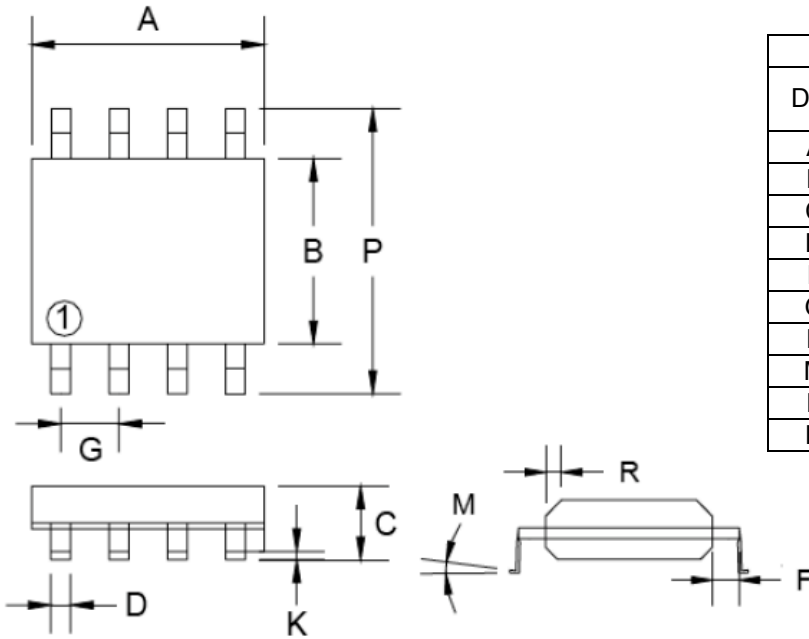
**Single Pulse Power**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

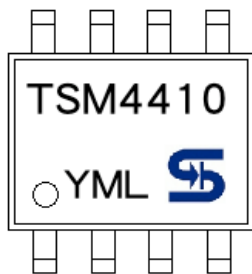


**SOP-8 Mechanical Drawing**



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**Marking Diagram**



- Y** = Year Code
- M** = Month Code  
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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