Rev 0; 1/08

Low-Cost CCFL Controller

General Description

The DS3991 is a controller for cold-cathode fluorescent lamps (CCFLs) that are used to backlight liquid-crystal displays (LCDs). The DS3991 is available for both push-pull and half-bridge drive topologies.

The DS3991 converts a DC voltage (5V to 24V) to the high-voltage ($300V_{RMS}$ to $1400V_{RMS}$) AC waveform that is required to power the CCFLs. The push-pull and half-bridge drive schemes use a minimal number of external components, which reduces component and assembly cost and makes the printed circuit board (PCB) design easy to implement. Both drive schemes provide an efficient DC to AC conversion and produce near-sinusoidal waveforms.

Applications

LCD PC Monitors

LCD TVs

Features

- **CCFL Controller for Backlighting LCD Panels**
- **Minimal External Components Required**
- **Lamp Fault Monitoring for Lamp-Open, Lamp-Overcurrent, Failure-to-Strike, and Overvoltage Conditions**
- **Accurate (±5%) On-Board Oscillator for Lamp Frequency (40kHz to 80kHz)**
- **Accurate (±5%) On-Board Oscillator for DPWM Burst-Dimming Frequency (80Hz to 300Hz)**
- **Device Supply Undervoltage Lockout**
- **Inverter Supply Undervoltage and Overvoltage Lockouts**
- **Soft-Start on Burst-Dimming Minimizes Audible Transformer Noise**
- **Strike Frequency Boost**
- **100% to < 10% Dimming Range**
- **Low Cost**
- **Single-Supply Operation Range: 4.5V to 5.5V**
- **Temperature Range: -40°C to +85°C**
- **16-Pin SO Package (150 mils)**

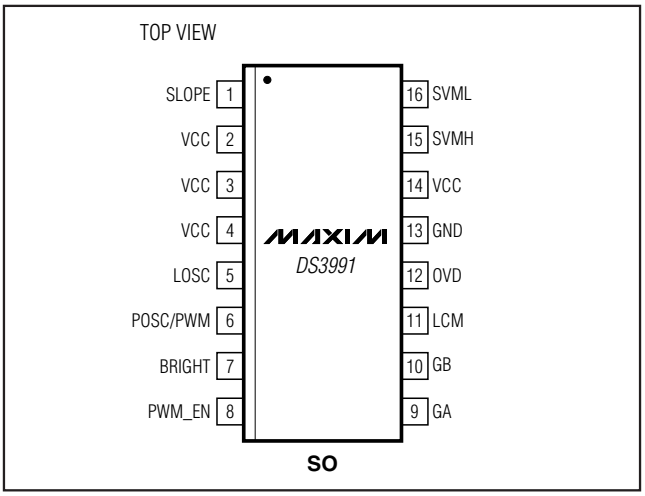
Ordering Information

PART	CONFIGURATION	TEMP RANGE	DIMMING FREQUENCY RANGE (Hz)	PIN-PACKAGE
DS3991V+C	Push-Pull	-40°C to +85°C	80 to 300	16 SO (150 mils)
DS3991V+T&R/C	Push-Pull	-40°C to +85°C	80 to 300	16 SO (150 mils)
DS3991V+	Half-Bridge	-40°C to +85°C	80 to 300	16 SO (150 mils)
DS3991V+T&R	Half-Bridge	-40°C to +85°C	80 to 300	16 SO (150 mils)

+Denotes a lead-free package.
T&R = Tape and reel.

Typical Operating Circuits appear at end of data sheet.

Pin Configuration



Low-Cost CCFL Controller

ABSOLUTE MAXIMUM RATINGS

Voltage Range on VCC Relative to Ground .....-0.5V to +6.0V
Voltage Range on Any Lead
Other than VCC.....-0.5V to (V_{CC} + 0.5V), not to exceed +6.0V

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....See J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Note 1)	4.5		5.5	V
Input Logic 1	V_{IH}		2.2		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		+0.8	V
BRIGHT, SVML, SVMH Voltage Range	V_{RA}		-0.3		V_{CC}+ 0.3	V
LCM and OVD Voltage Range	V_{RC}	(Note 2)	-0.3		V_{CC} + 0.3	V
Gate-Driver Output Charge Loading	Q_G				20	nC
LOSC and POSC Loading	C_{OSC}				20	pF

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	GA, GB loaded with 300pF		5	10	mA
Low-Level Output Voltage (GA, GB)	V_{OL}	I_{OL} = 4mA			0.4	V
High-Level Output Voltage (GA, GB)	V_{OH}	I_{OH} = -1mA	2.4			V
UVLO Threshold: V_{CC} Rising	V_{UVLOR}				4.3	V
UVLO Threshold: V_{CC} Falling	V_{UVLOF}		3.7			V
UVLO Hysteresis	V_{UVLOH}			100		mV
SVML Falling Threshold	V_{SVMLT}		1.94	2.00	2.06	V
SVMH Rising Threshold	V_{SVMHT}		1.94	2.00	2.06	V
SVML and SVMH Hysteresis	V_{SVMH}			150		mV
LCM and OVD DC Bias Voltage	V_{DCB}			1.35		V
LCM and OVD Input Resistance	R_{DCB}			50		kΩ
Lamp-Off Threshold	V_{LOT}	(Note 3)	1.65	1.75	1.85	V
Lamp Overcurrent Threshold	V_{LOCT}	(Note 3)	3.25	3.35	3.45	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Lamp Regulation Threshold	V_{LRT}	(Note 3)	2.29	2.35	2.41	V
OVD Threshold	V_{OVDT}	(Note 3)	2.25	2.35	2.45	V
Lamp Frequency	LF_{OSCI}		40		80	kHz
Lamp Frequency Tolerance	LF_{TOL}	LOSC resistor ±0.1% over temperature; measured from 0°C to +85°C	-5		+5	%
Burst-Dimming PWM Frequency	PF_{OSCI}		80		300	Hz
Burst-Dimming PWM Frequency Tolerance	PF_{TOL}	POSC resistor ±0.1% over temperature	-5		+5	%
BRIGHT Voltage: Minimum Brightness	V_{BMIN}	SLOPE = 0			0	V
		SLOPE = 1	3.3			V
BRIGHT Voltage: Maximum Brightness	V_{BMAX}	SLOPE = 0	3.3			V
		SLOPE = 1			0	V
Gate-Driver Output Rise/Fall	t_R/t_F	C_L = 600pF			100	ns

Note 1: All voltages are referenced to ground unless otherwise noted. Currents into the IC are positive; currents out of the IC are negative.

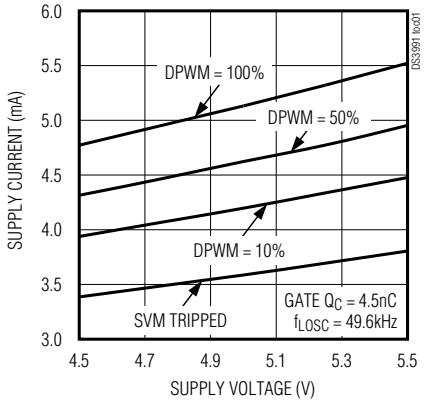
Note 2: During fault conditions, if AC-coupled, LCM and OVD can go below ground by up to 1V for up to 1s.

Note 3: Threshold voltage includes the DC bias-voltage offset.

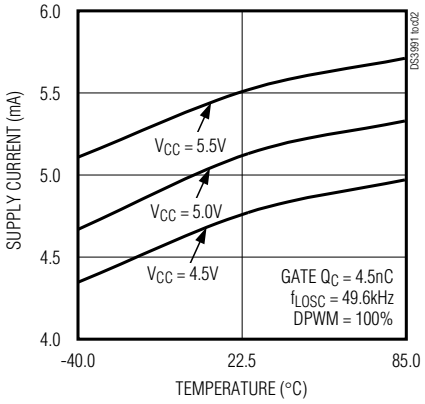
Typical Operating Characteristics

(V_{CC} = 5.0V, T_A = +25°C, unless otherwise noted.)

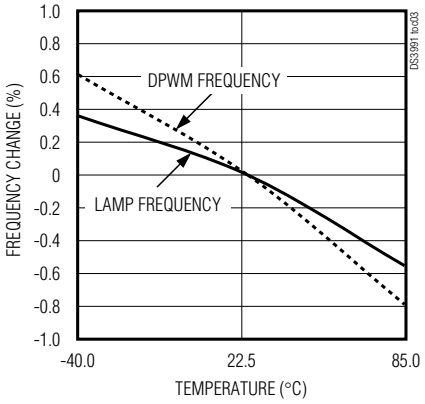
ACTIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



ACTIVE SUPPLY CURRENT vs. TEMPERATURE



INTERNAL FREQUENCY CHANGE vs. TEMPERATURE

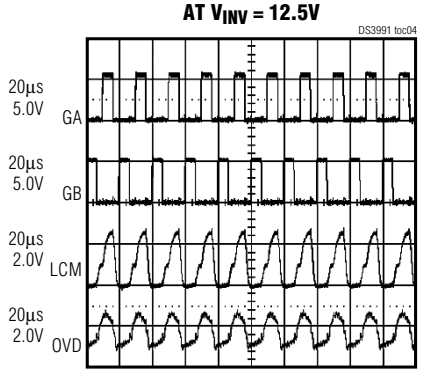


Low-Cost CCFL Controller

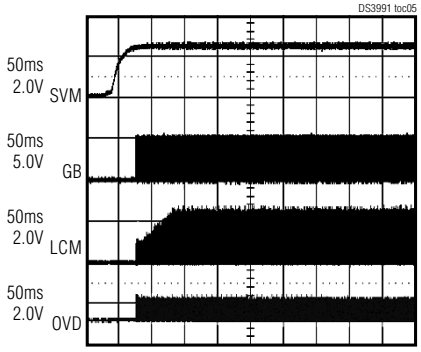
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, multilamp configuration, unless otherwise noted.)

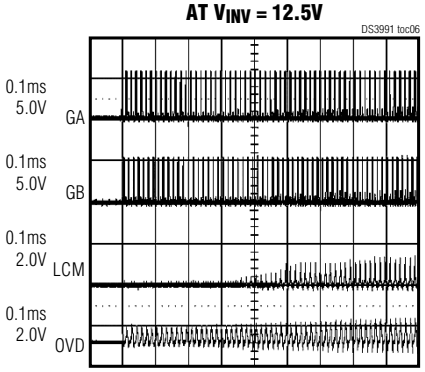
PUSH-PULL TYPICAL OPERATION AT V_{INV} = 12.5V



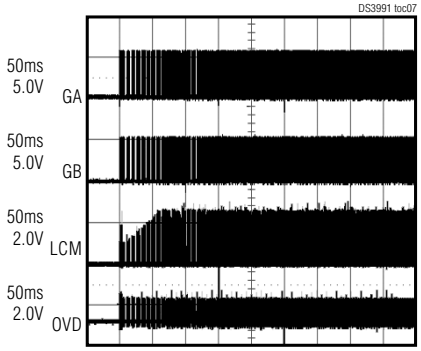
PUSH-PULL TYPICAL STARTUP WITH SVM



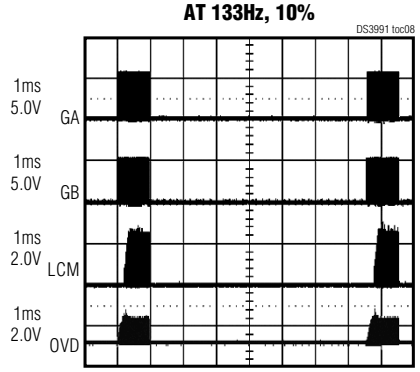
PUSH-PULL SOFT-START AT V_{INV} = 12.5V



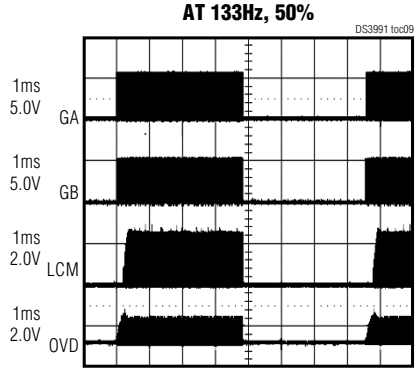
PUSH-PULL LAMP STRIKE, EXPANDED VIEW



PUSH-PULL BURST DIMMING AT 133Hz, 10%



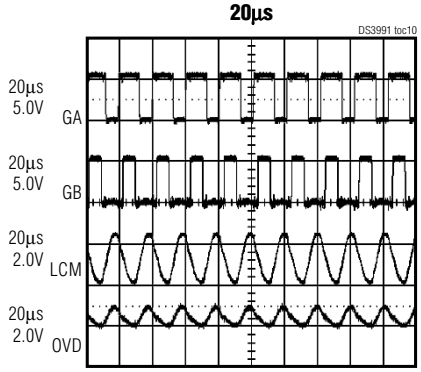
PUSH-PULL BURST DIMMING AT 133Hz, 50%



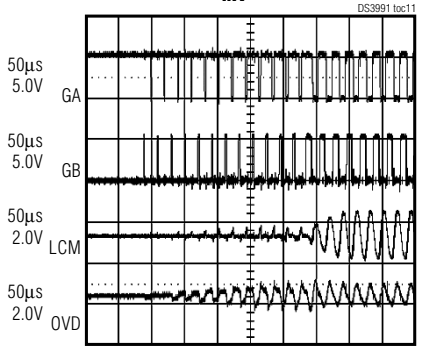
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, T_A = +25°C, single-lamp configuration, unless otherwise noted.)

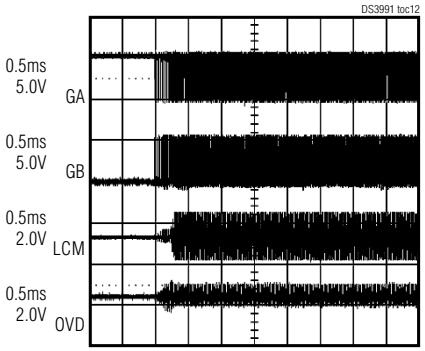
HALF-BRIDGE NORMAL OPERATION, 20µs



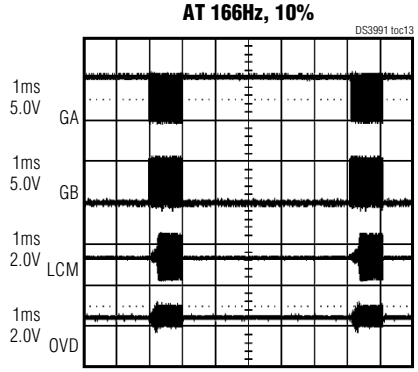
HALF-BRIDGE SOFT-START AT V_{INV} = 12.5V



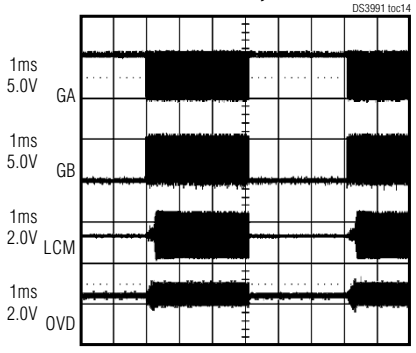
HALF-BRIDGE LAMP STRIKE, EXPANDED VIEW



HALF-BRIDGE BURST DIMMING AT 166Hz, 10%



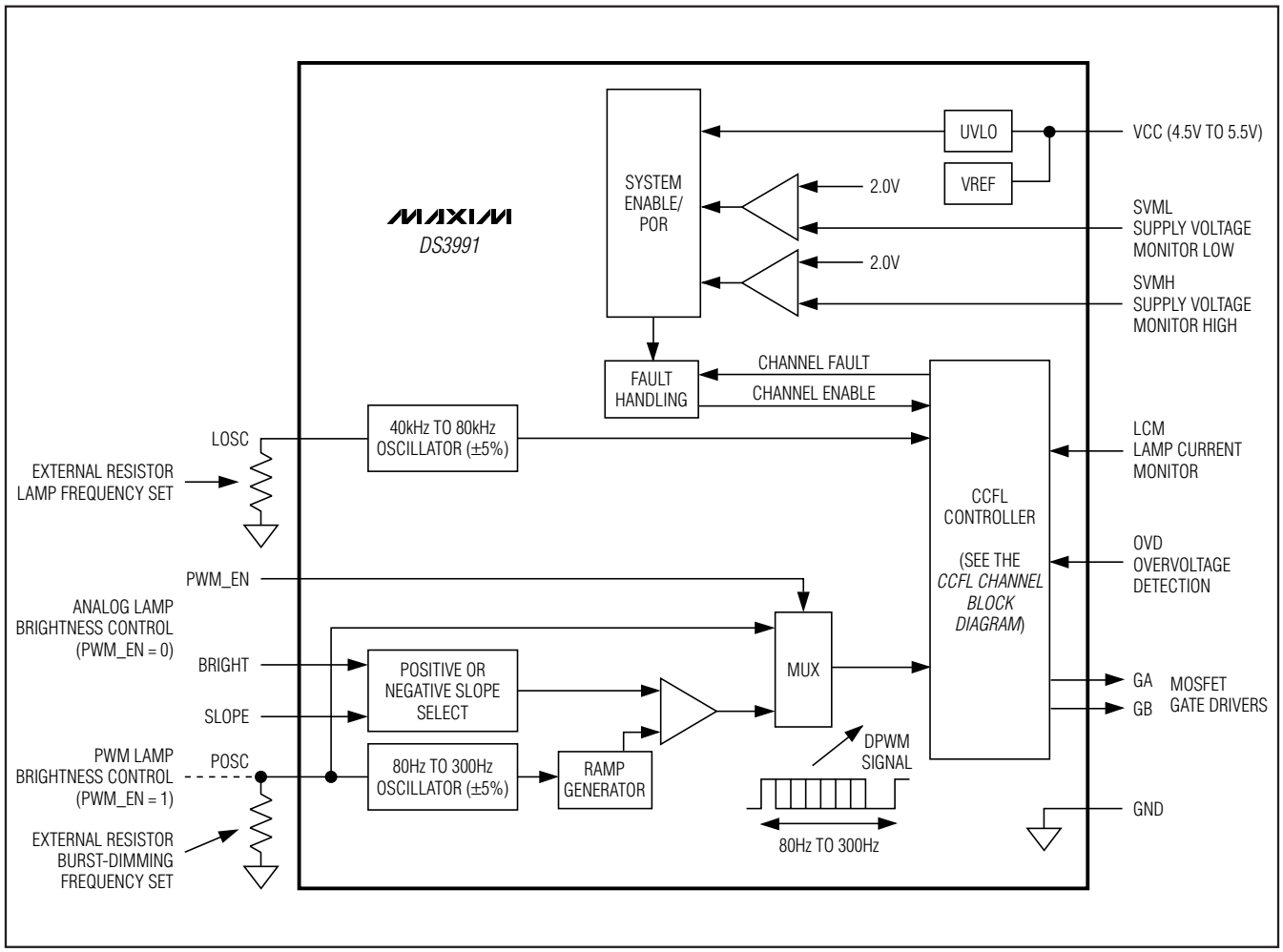
HALF-BRIDGE BURST DIMMING AT 166Hz, 50%



Pin Description

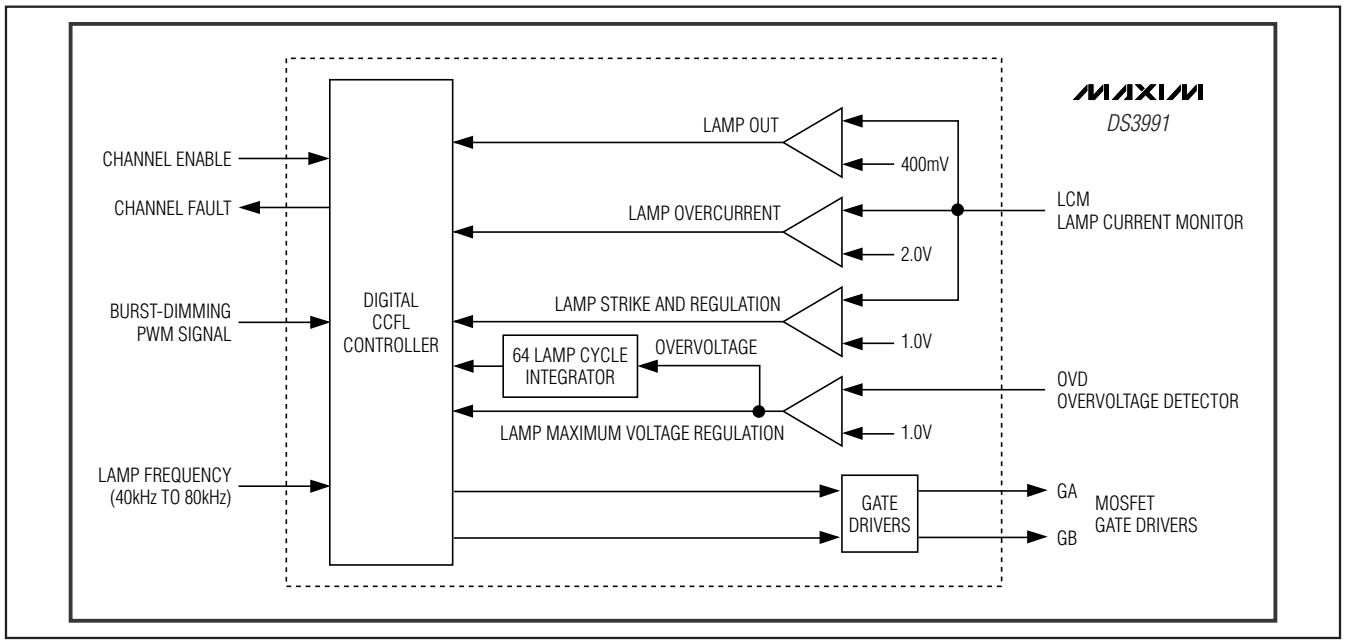
PIN	NAME	I/O	FUNCTION
1	SLOPE	I	BRIGHT Slope Select. This digital input determines the slope of the BRIGHT input when an analog DC voltage is used to control lamp brightness (PWM_EN = 0). SLOPE = 0: positive slope (0V = minimum brightness, 3.3V = 100% brightness) SLOPE = 1: negative slope (0V = 100% brightness, 3.3V = minimum brightness)
2, 3, 4	VCC	—	Connect to Voltage Supply. These pins should be connected to the voltage supply pin, VCC.
5	LOSC	O	Lamp Oscillator Resistor Adjust. A resistor (R_{LOSC}) to ground on this pin sets the frequency of the lamp oscillator (F_{LOSC}). (R_{LOSC} x F_{LOSC} = 4.0E9).
6	POSC/ PWM	O/I	Burst-Dimming PWM Oscillator Resistor Adjust/PWM Digital Input. If PWM_EN = 0, a resistor (R_{POSC}) to ground on this pin sets the frequency (F_{POSC}) of the burst-dimming PWM oscillator (R_{POSC} x F_{POSC} = 4.0E6). If PWM_EN =1, a digital 80Hz to 300Hz PWM signal at this input controls the lamp brightness.
7	BRIGHT	I	Lamp-Brightness Control. If PWM_EN = 0, a 0V to 3.3V analog DC voltage at this input controls the brightness of the lamp.
8	PWM_EN	I	PWM Lamp-Brightness Control Enable. This digital input determines whether the BRIGHT or POSC/PWM input is used to control lamp brightness. PWM_EN = 0 = PWM disabled (analog DC voltage applied at the BRIGHT input) PWM_EN = 1 = PWM enabled (digital PWM signal applied at the POSC/PWM input)
9	GA	O	MOSFET Gate Drive A. Drives a logic-level power MOSFET.
10	GB	O	MOSFET Gate Drive B. Drives a logic-level power MOSFET.
11	LCM	I	Lamp Current Monitor Input. Lamp current is monitored by a resistor placed in series with the low-voltage side of the lamp.
12	OVD	I	Overvoltage Detection Input. Lamp voltage is monitored by a capacitor divider placed on the high-voltage side of the lamp.
13	GND	—	Signal Ground
14	VCC	—	Voltage Supply, 4.5V to 5.5V
15	SVMH	I	Supply Voltage Monitor High. The DC inverter-supply voltage is monitored by an external resistor divider. The resistor-divider should be set such that it provides 2V at this pin for the maximum allowable range of the DC inverter supply. Pulling this input above 2V turns the lamps off and resets the controller. Connect to GND if not used.
16	SVML	I	Supply Voltage Monitor Low. The DC inverter-supply voltage is monitored by an external resistor divider. The resistor-divider should be set such that it provides 2V at this pin for the minimum allowable range of the DC inverter supply. Pulling this input below 2V turns the lamps off and resets the controller. Connect to VCC if not used.

Main System Block Diagram



Low-Cost CCFL Controller

CCFL Channel Block Diagram



Detailed Description

The DS3991 is available for both push-pull and half-bridge drive topologies. In both drive topologies, the DS3991 drives two logic-level MOSFETs. The DS3991 alternately turns on the two MOSFETs to create the high-voltage AC waveform on the secondary. By varying the duration of the MOSFET turn-on times, the controller is able to accurately control the amount of current flowing through the CCFL lamp. See the *Typical Push-Pull Application* and *Typical Half-Bridge Application* figures.

The DS3991 can also drive more than one CCFL lamp per channel. The *Typical Push-Pull Application, Multiple Lamp Per Channel* and *Typical Half-Bridge Application, Multiple Lamp Per Channel* figures show an application driving three lamps.

A series resistor on the low-voltage side of the CCFL lamp enables current monitoring. The voltage developed across this resistor is fed to the lamp current monitor (LCM) input on the DS3991. The DS3991 compares the resistor voltage against an internal reference voltage to determine the duty cycle for the MOSFET gates. See the *Main System Block Diagram* and the *CCFL Channel Block Diagram* for more information.

Dimming Control

The DS3991 uses burst dimming to control the lamp brightness. During the high period of the DPWM cycle, the lamp is driven at the selected lamp frequency (40kHz to 80kHz) as shown in Figure 1. This part of the cycle is also called the burst period because of the lamp-frequency burst that occurs during this time. During the low period of the DPWM cycle, the controller disables the MOSFET gate drivers so the lamp is not driven. This causes the current to stop flowing in the lamp, but the time is short enough to keep the lamp from de-ionizing. Dimming is increased/decreased by adjusting (i.e., modulating) the burst-period duty cycle. At the beginning of each burst-dimming cycle, soft-start slowly ramps the lamp current to reduce the potential to create audible transformer noise.

There are two methods to control the duty cycle and frequency of the burst-dimming DPWM. If the PWM_EN pin is tied low, then the analog-control method is enabled; a 0V to 3.3V analog voltage at the BRIGHT input pin determines the duty cycle of a digital pulse-width modulated (DPWM) signal. The frequency of the DPWM signal is determined by the value of the resistor tied from the POSC pin to ground. The slope of the BRIGHT dimming input is either positive or negative based on whether the SLOPE pin is tied low or high, respectively.

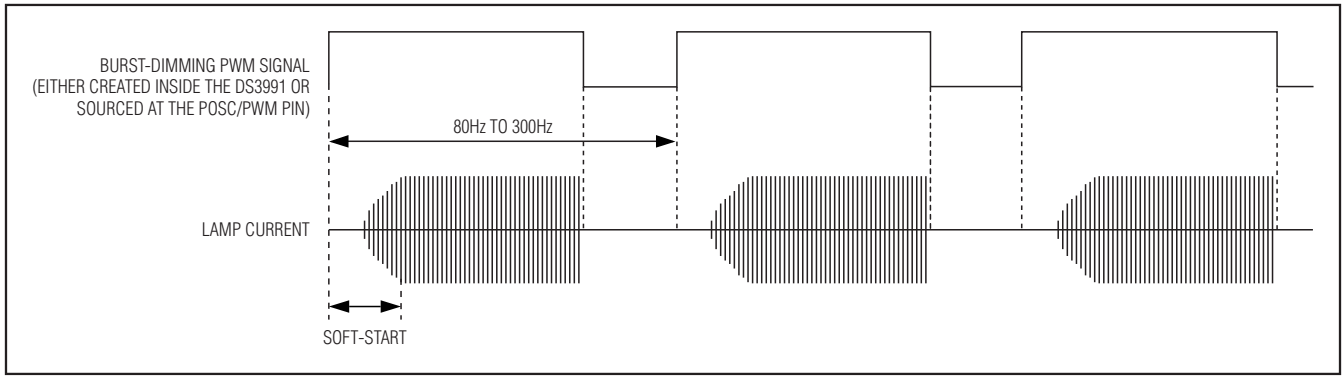


Figure 1. Digital PWM Dimming and Soft-Start

If the PWM_EN pin is tied high, the digital control method is enabled and an external PWM signal between 80Hz and 300Hz is applied at the POSC/PWM pin to set the brightness of the lamp. In the digital control method, the SLOPE and BRIGHT pins are not used.

Lamp Strike

On lamp strike, the DS3991 boosts the normal operating lamp frequency by 33%. This is done to increase the voltage created and help ensure that the lamp strikes. Once the controller detects that the lamp has struck, the frequency is returned to the normal lamp frequency.

Setting the Lamp and DPWM Frequencies Using External Resistors

Both the lamp and DPWM frequencies are set using external resistors. The resistance required for either frequency can be determined using the following formula:

$$R_{OSC} = \frac{K}{f_{OSC}}$$

where K = 4000kΩ x kHz for lamp frequency calculations, K = 4kΩ x kHz for DPWM frequency calculations.

Example: Select the resistor values to configure the DS3991 to have a 50kHz lamp frequency and a 160Hz DPWM frequency. For the DPWM resistor calculation, K = 4 kΩ x kHz. For the lamp frequency resistor (R_{LOSC}) calculation, K = 4000 kΩ x kHz. The formula above can now be used to calculate the resistor values for R_{LOSC} and R_{POSC} as follows:

$$R_{LOSC} = \frac{4000k\Omega \times kHz}{50kHz} = 80k\Omega$$

$$R_{POSC} = \frac{4k\Omega \times kHz}{0.160kHz} = 25k\Omega$$

Supply Monitoring

The DS3991 has supply-voltage monitors (SVML and SVMH) for the inverter's DC supply (V_{INV}) and an undervoltage lockout for the V_{CC} supply to ensure that voltage levels are adequate for proper operation. The inverter supply is monitored for overvoltage conditions at the SVMH pin and undervoltage conditions at the SVML pin. External resistor-dividers at each SVM input feed into two comparators, both having 2V thresholds (see Figure 2). Using the equation below to determine the resistor values, the SVMH and SVML trip points (V_{TRIP}) can be customized to shut off the inverter when the inverter supply voltage rises above or drops below specified values.

Operating with the inverter supply at too low of a level can prevent the transformer from reaching the strike voltage and could potentially cause numerous other problems. Operating with the inverter voltage at too high of a level can be damaging to the inverter components. Proper use of the SVMs can prevent these problems. If desired, the high and/or low SVMs can be disabled by connecting the SVMH pin to GND and the SVML pin to VCC.

$$V_{TRIP} = 2.0 \times \left(\frac{R_1 + R_2}{R_1} \right)$$

The SVMH and SVML are high-impedance inputs and noise on the inverter supply can cause the monitors to inadvertently trigger even though the inputs contain hysteresis. The user may wish to add a lowpass filter to reduce the noise present at the SVMH and SVML inputs.

The V_{CC} monitor is a 5V supply undervoltage lockout (UVLO) that prevents operation when the DS3991 does not have adequate voltage for its analog circuitry to operate or to drive the external MOSFETs. The V_{CC} monitor features hysteresis to prevent V_{CC} noise from

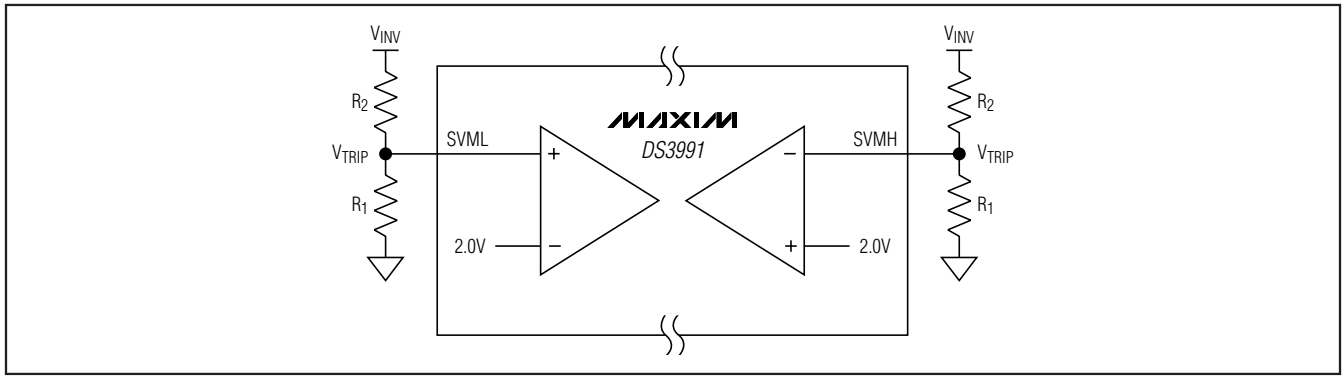


Figure 2. Setting the SVML and SVMH Threshold Voltages

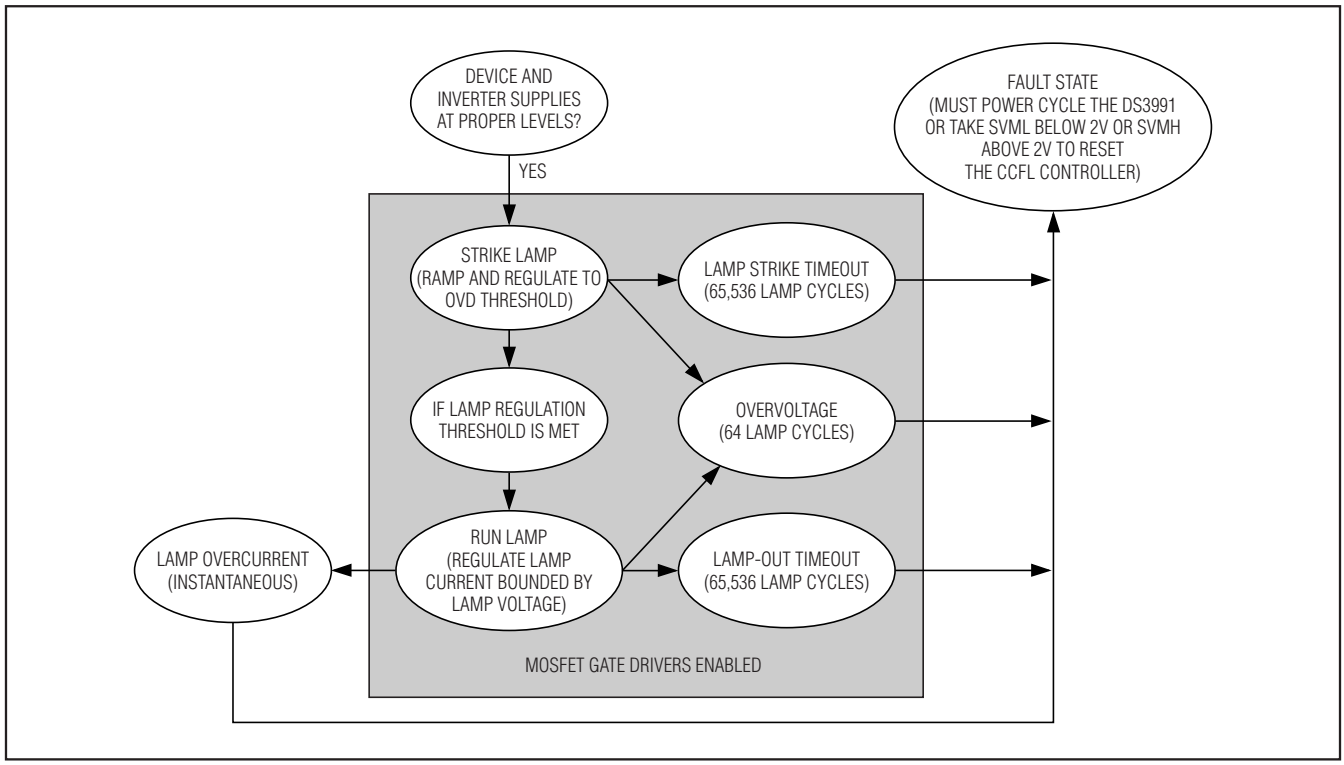


Figure 3. Fault-Handling Flowchart

causing spurious operation when V_{CC} is near the trip point. This monitor cannot be disabled by any means.

Fault Monitoring

The DS3991 provides extensive fault monitoring. It can detect open-lamp, lamp overcurrent, failure to strike, and overvoltage conditions. Figure 3 shows a flowchart of how the DS3991 controls and monitors each lamp. The steps are as follows:

The lamps do not turn on unless the DS3991 supply voltage is >4.5V and the voltage at the supply-voltage monitor low (SVML) input is > 2V and the supply-voltage monitor high (SVMH) input is < 2V.

When both the DS3991 and the DC inverter supplies are at acceptable levels, the DS3991 attempts to strike the lamps. The DS3991 slowly ramps up the MOSFET gate duty cycle until the lamp strikes. The controller detects

that the lamp has struck by detecting current flow in the lamp. If during the strike ramp, the maximum allowable voltage is reached, the controller stops increasing the MOSFET gate duty cycle to keep from overstressing the system. The DS3991 goes into a fault-handling state if the lamp has not struck after 65,536 lamp cycles. If an overvoltage event is detected during the strike attempt, the DS3991 disables the MOSFET gate drivers and goes into the fault handling state.

Once the lamp is struck, the DS3991 moves to the run-lamp stage. In the run-lamp stage, the DS3991 adjusts the MOSFET gate duty cycle to optimize the lamp current. The gate duty cycle is always constrained to keep the system from exceeding the maximum allowable lamp voltage. If lamp current ever drops below the lamp-out reference point for 65,536 lamp cycles, the lamp is considered extinguished. In this case the MOSFET gate drivers are disabled and the device moves to the fault-handling stage.

In the case of a lamp overcurrent, the DS3991 instantaneously declares the controller to be in a fault state. If the DS3991 goes into the fault state, the DS3991 shuts down. Once a fault state is entered, the controller remains in that state until one of the following occurs:

- V_{CC} drops below the UVLO threshold
- SVML input drops below 2.0V
- SVMH input goes above 2.0V

Applications Information

Component Selection

External component selection has a large impact on the overall system performance and cost. The two most important external components are the transformers and MOSFETs.

The transformer should be able to operate in the 40kHz to 80kHz frequency range of the DS3991, and the turns ratio should be selected so the MOSFET drivers run at 28% to 35% duty cycle during steady-state operation. The transformer must be able to withstand the high open-circuit voltage that is used to strike the lamp. Additionally, its primary/secondary resistance and inductance characteristics must be considered because they contribute significantly to determining the efficiency and transient response of the system. Table 1 shows a transformer specification that has been utilized for a 12V inverter supply, 438mm x 2.2mm lamp design.

The MOSFETs must have a threshold voltage that is low enough to work with logic-level signals, a low on-resistance to maximize efficiency and limit the MOSFET's power dissipation, and a breakdown voltage high enough to handle the transient. For push-pull topologies, the breakdown voltage of the MOSFETs should be a minimum of 3x the inverter voltage supply. Additionally, the total gate charge must be less than Q_G, which is specified in the *Recommended Operating Conditions* table.

Table 1. Transformer Specifications (as used in the Typical Operating Circuits)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turns Ratio (Secondary/Primary) Push-Pull Type	(Notes 1, 2, 3)		40		
Turns Ratio (Secondary/Primary) Half-Bridge Type	(Note 3)		80		
Frequency		40		80	kHz
Output Power				6	W
Output Current			5	8	mA
Primary DCR	Center tap to one end		200		mΩ
Secondary DCR			500		Ω
Primary Leakage			12		µH
Secondary Leakage			185		mH
Primary Inductance			70		µH
Secondary Inductance			500		mH
Secondary Output Voltage	1000ms (min)	2000			V_{RMS}
	Continuous	1000			

Note 1: Primary should be bifilar wound with center-tap connection.

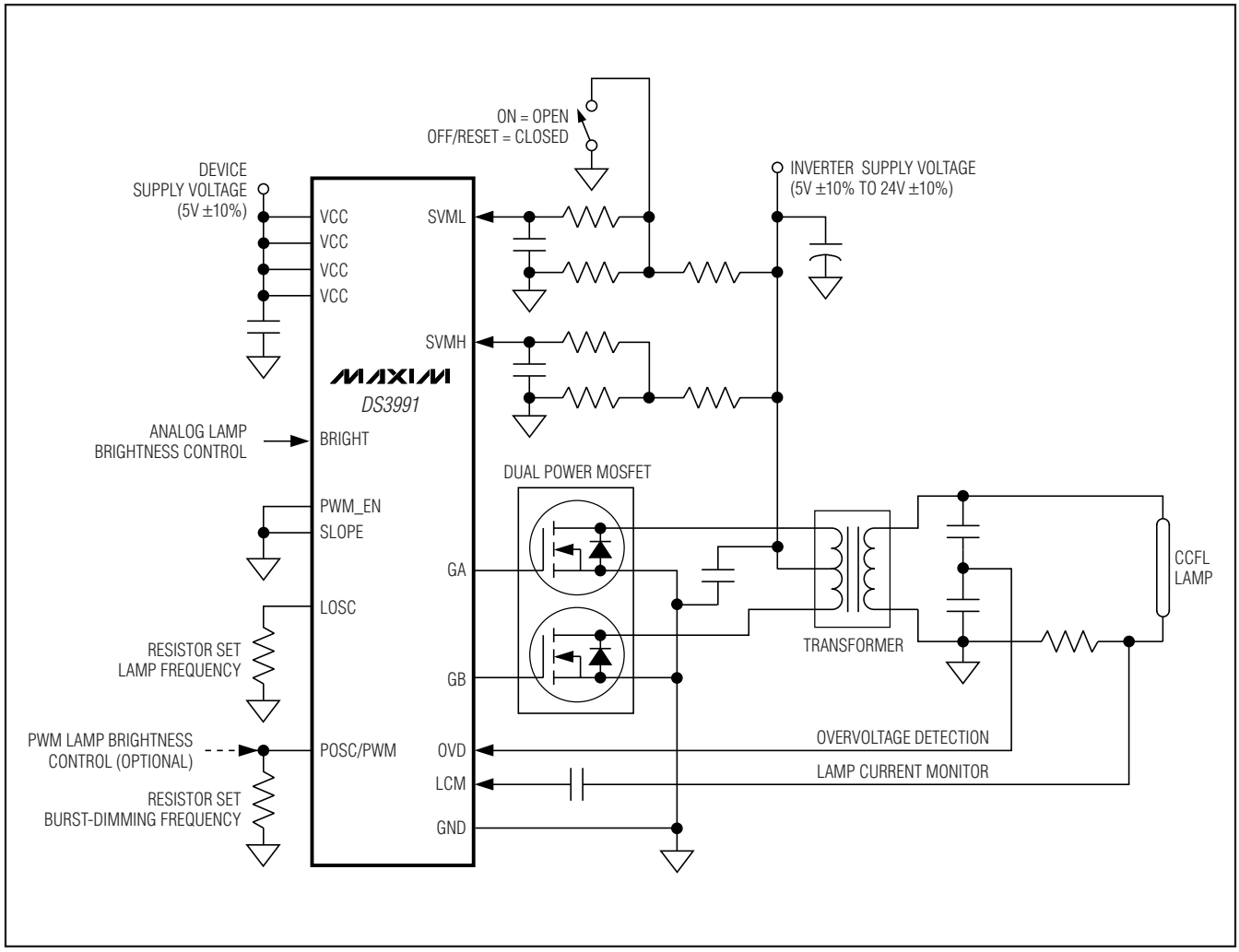
Note 2: Turns ratio is defined as secondary winding divided by the sum of both primary windings.

Note 3: This is the nominal turns ratio for driving a 438mm x 2.2mm lamp with a 12V supply. Refer to Application Note 3375 for more information on push-pull type applications.

Low-Cost CCFL Controller

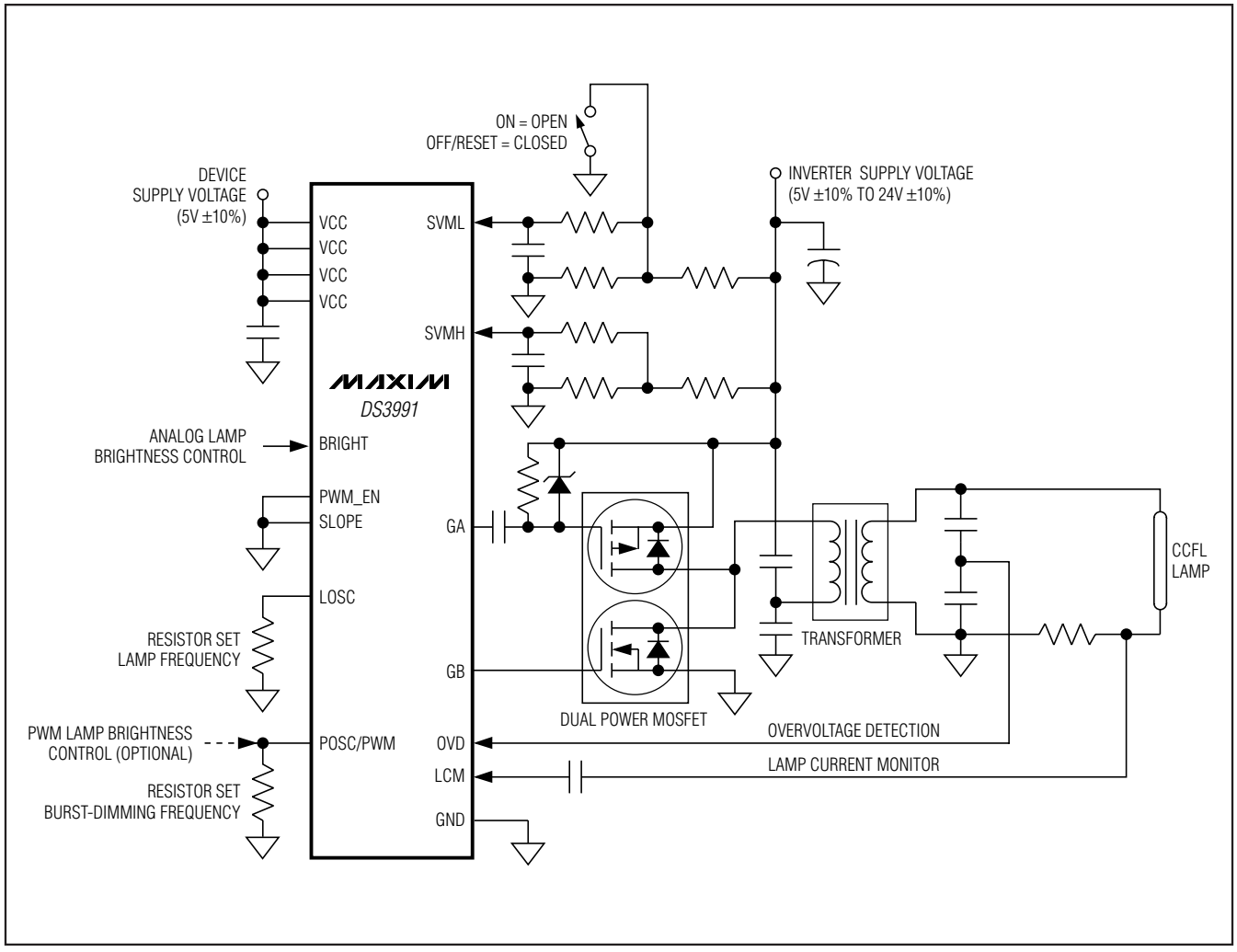
Typical Operating Circuits

Typical Push-Pull Application



Typical Operating Circuits (continued)

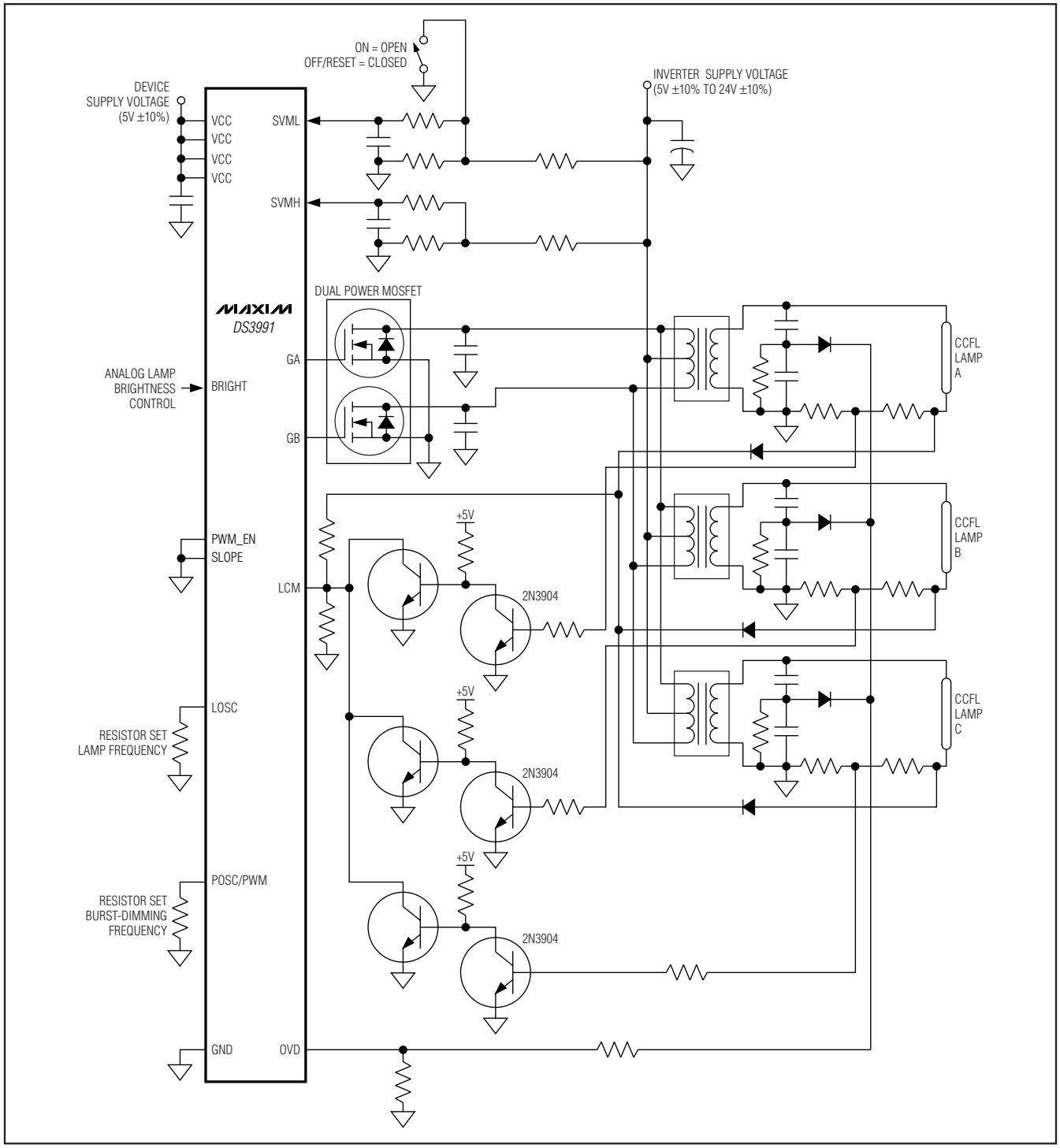
Typical Half-Bridge Application



Low-Cost CCFL Controller

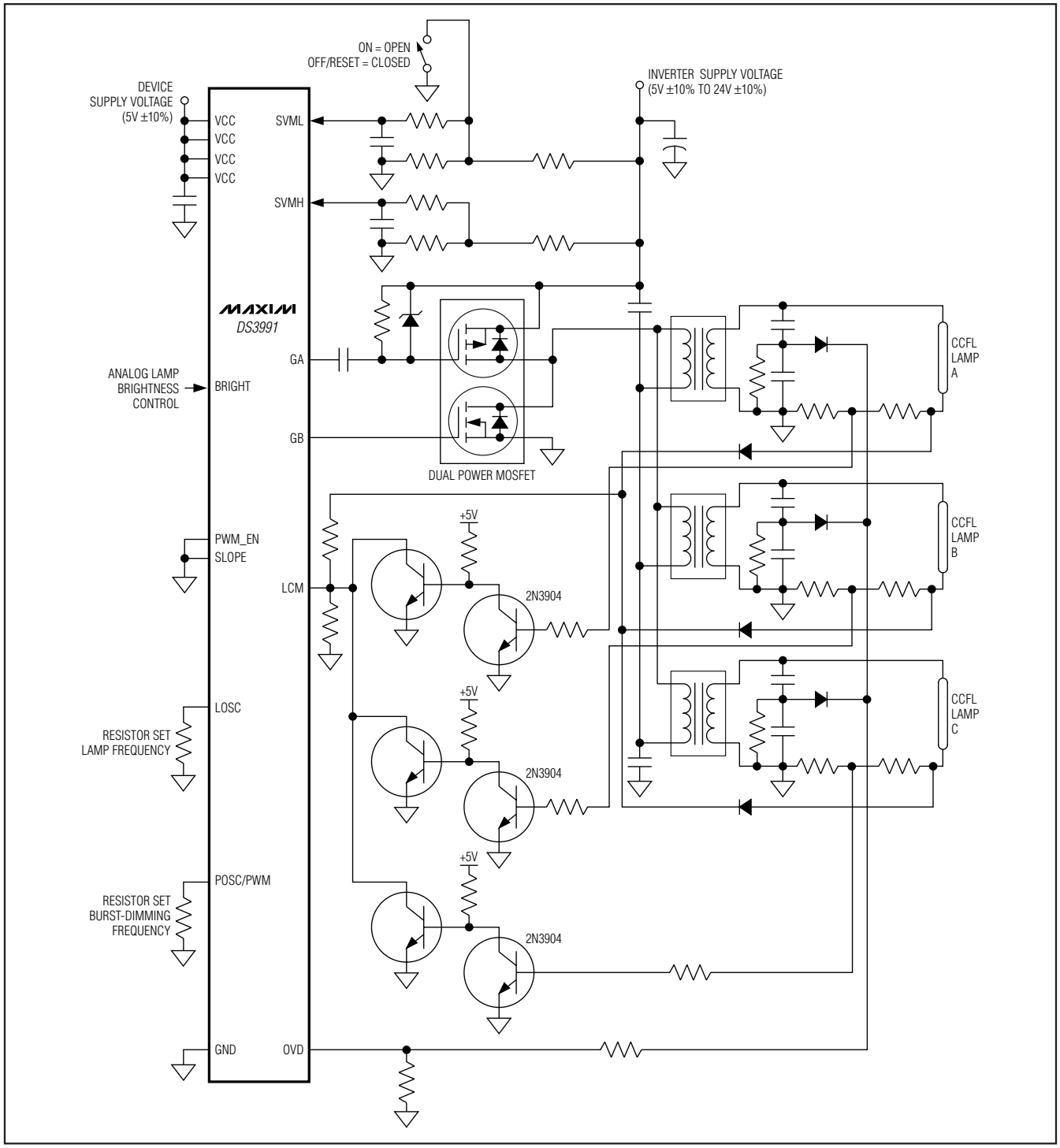
Typical Operating Circuits (continued)

Typical Push-Pull Application, Multiple Lamps Per Channel



Typical Operating Circuits (continued)

Typical Half-Bridge Application, Multiple Lamps Per Channel



Low-Cost CCFL Controller

Power-Supply Decoupling

To achieve best results, it is highly recommended that a decoupling capacitor be used on pin 14, the IC power-supply pin. Typical values of decoupling capacitors are 0.01µF or 0.1µF. Use a high-quality, ceramic, surface-mount capacitor, and mount it as close as possible to the VCC and GND pins of the IC to minimize lead inductance. Pins 2, 3, and 4 require connection to supply voltage (VCC) but do not require any additional decoupling.

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.

PACKAGE TYPE	DOCUMENT NO.
16 SO (150 mils)	**56-G2008-001**