

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N7002FU

High Speed Switching Applications

Analog Switch Applications

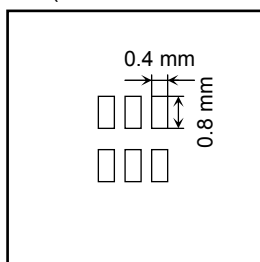
- Small package
- Low ON resistance : $R_{on} = 3.3 \Omega$ (max) (@ $V_{GS} = 4.5 V$)
 : $R_{on} = 3.2 \Omega$ (max) (@ $V_{GS} = 5 V$)
 : $R_{on} = 3.0 \Omega$ (max) (@ $V_{GS} = 10 V$)

Absolute Maximum Ratings ($T_a = 25^\circ C$) (Q1, Q2 Common)

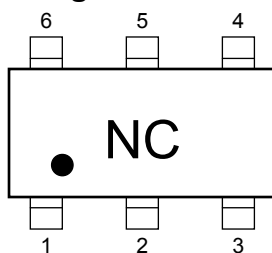
Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	60	V
Gate-Source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	200	mA
	Pulse	I_{DP}	800	
Drain power dissipation ($T_a = 25^\circ C$)		P_D (Note 1)	300	mW
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature range		T_{stg}	-55~150	$^\circ C$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

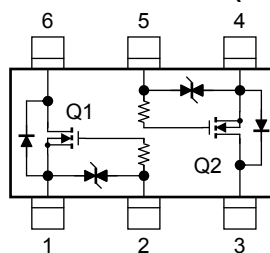
Note 1: Total rating, mounted on FR4 board
 (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.32mm² \times 6)



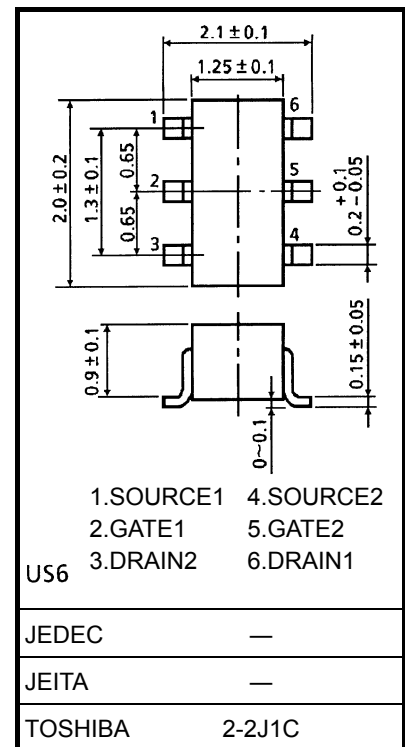
Marking



Equivalent Circuit (top view)



Unit: mm



Handling Precaution

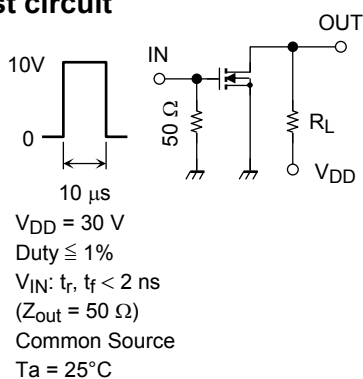
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

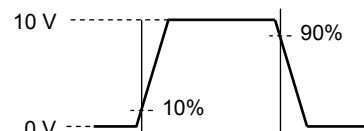
Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit	
Gate leakage current	I_{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$	—	—	± 10	μA	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}, V_{GS} = 0$	60	—	—	V	
Drain cut-off current	I_{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0$	—	—	1	μA	
Gate threshold voltage	V_{th}	$V_{DS} = 10 \text{ V}, I_D = 0.25 \text{ mA}$	1.0	—	2.5	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$	170	—	—	mS	
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = 500 \text{ mA}, V_{GS} = 10 \text{ V}$	—	2.0	3.0	Ω	
		$I_D = 100 \text{ mA}, V_{GS} = 5 \text{ V}$	—	2.1	3.2		
		$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$	—	2.2	3.3		
Input capacitance	C_{iss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	17	—	pF	
Reverse transfer capacitance	C_{rss}		—	1.4	—	pF	
Output capacitance	C_{oss}		—	5.8	—	pF	
Switching time	Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, I_D = 200 \text{ mA}, V_{GS} = 0 \sim 10 \text{ V}$	—	2.4	4.0	ns
	Turn-off delay time	$t_{d(off)}$		—	26	40	

Switching Time Test Circuit

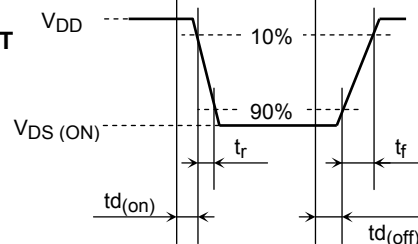
(a) Test circuit



(b) V_{IN}



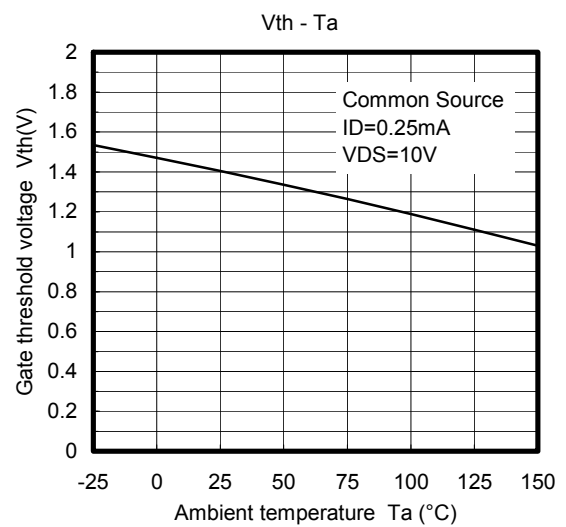
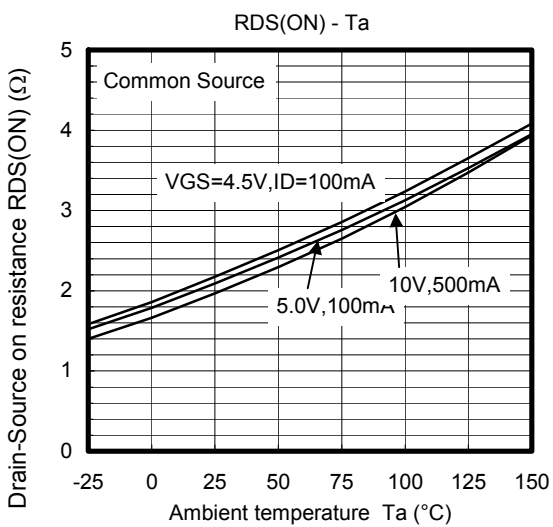
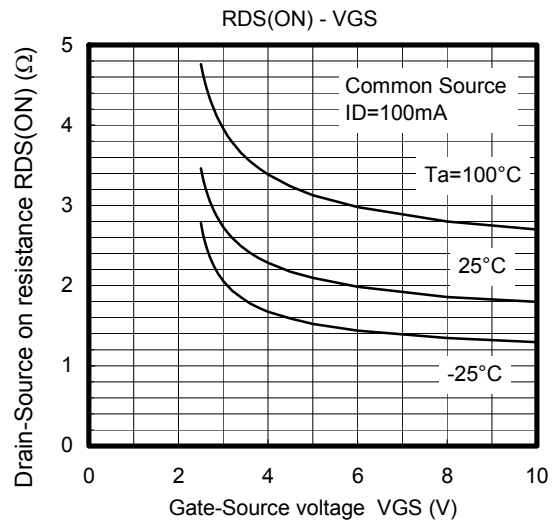
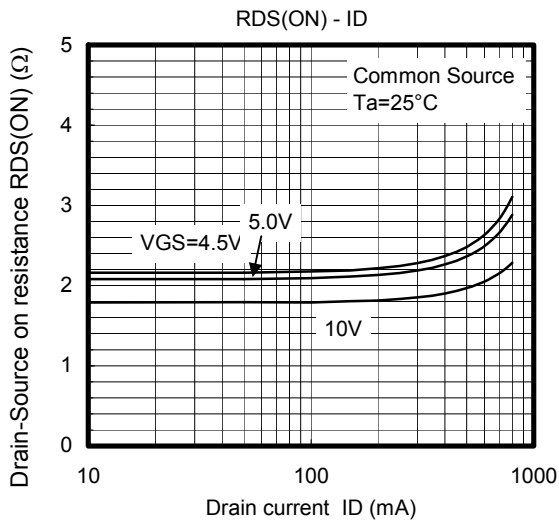
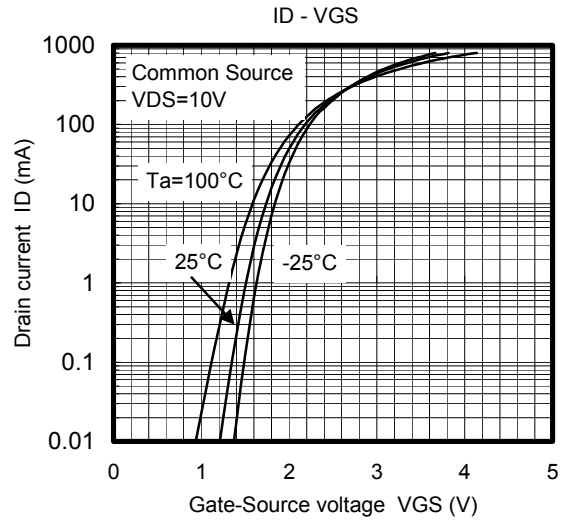
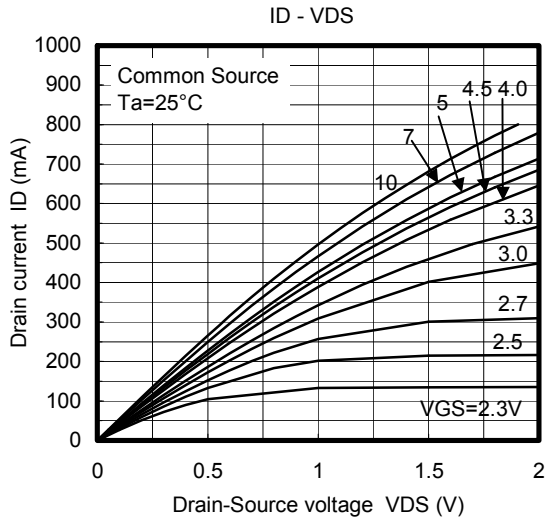
(c) V_{OUT}

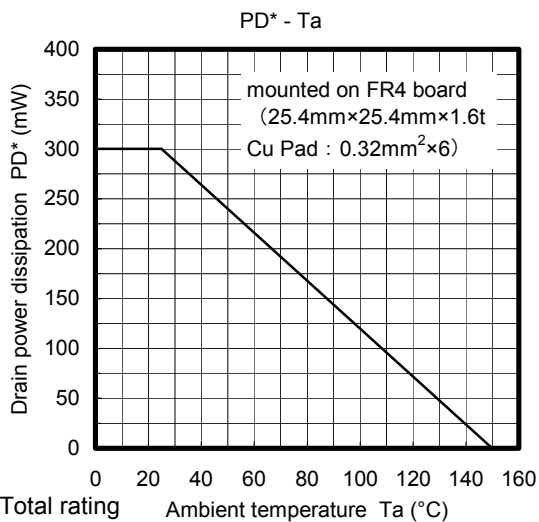
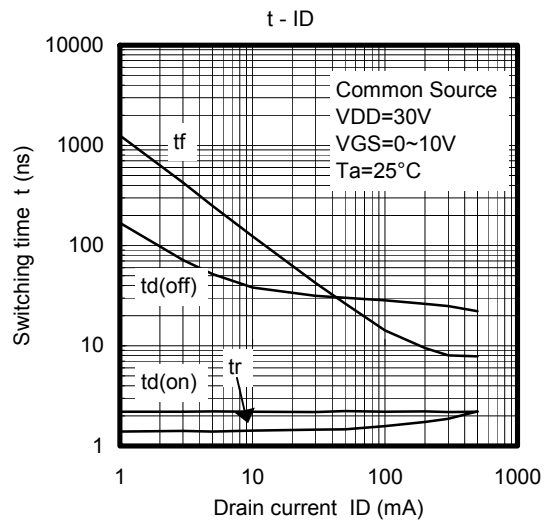
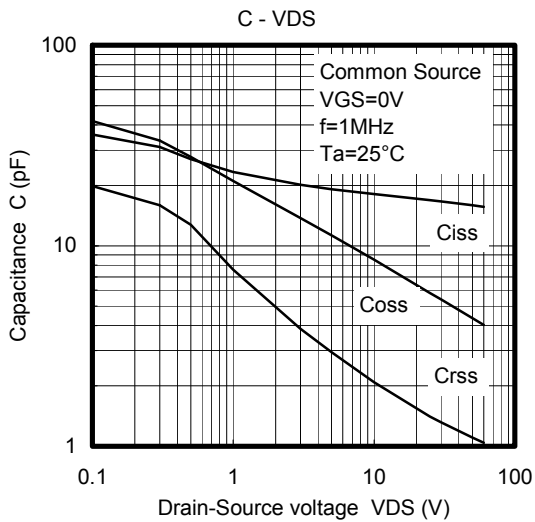
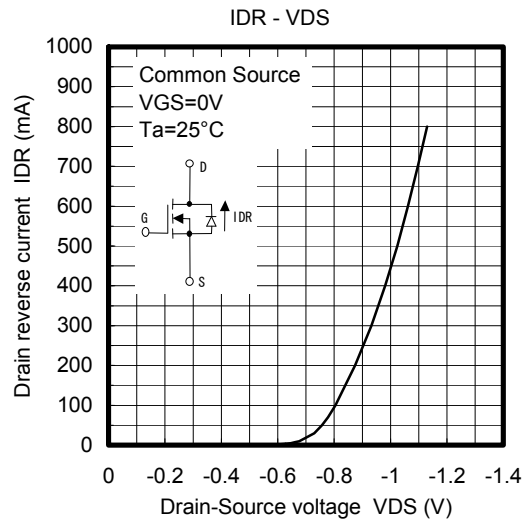
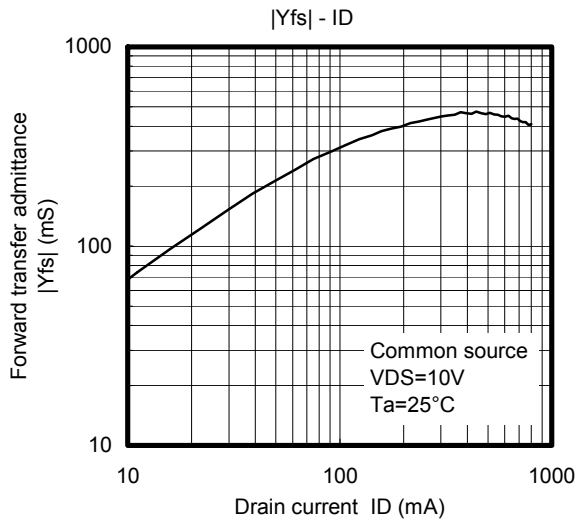


Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 250 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(ON)}$ requires higher voltage than V_{th} and $V_{GS(OFF)}$ requires lower voltage than V_{th} . (Relationship can be established as follows: $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$)

Please take this into consideration for using the device.





* :Total rating

RESTRICTIONS ON PRODUCT USE

20070701-EN GENERAL

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