Triple Channel Video Driver with LPF

The ISL59119 is a triple channel reconstruction filter with a -3dB roll-off frequency of 8MHz. Operating from single supplies ranging from +3.0V to +5.5V and sinking an ultra-low 8mA quiescent current, the ISL59119 is ideally suited for low power, battery-operated applications.

The ISL59119 is designed to meet the needs for micropower and bandwidth required in battery-operated communication, instrumentation and modern industrial applications such as video on demand, cable set-top boxes, and MP3 players.

The ISL59119 is available in an 8 Ld SO package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

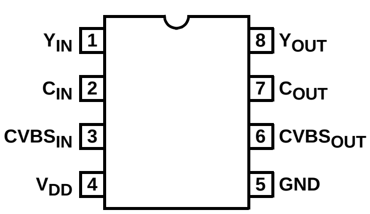
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE(Pb-Free)	PKG. DWG. #
ISL59119IBZ*	59119 IBZ	-40 to +85°C	8 Ld SOIC	MDP0027

*Add "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

ISL59119
(8 LD SO)
TOP VIEW



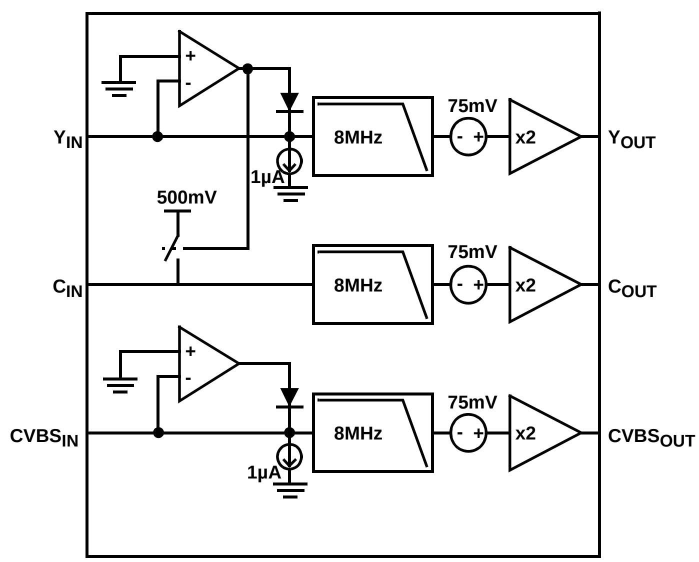
Features

- 5th Order 8MHz Reconstruction Filter
- Low Supply Current (8mA typ)
- Supplies from +3.0V to +5.5V
- Rail-to-Rail Output
- Pb-free (RoHS compliant)

Applications

- Video Amplifiers
- Portable and Handheld Products
- Communications Devices
- Video on Demand
- Cable Set-top Boxes
- Satellite Set-top Boxes
- MP3 Players
- Personal Video Recorder

Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage from V_{DD} to GND 6.0V
Input Voltage . . . . V_{DD} +0.3V to GND -0.3V
Continuous Output Current 40mA

Thermal Information

Storage Temperature . . . .-65°C to +125°C
Ambient Operating Temperature . . . .-40°C to +85°C
Operating Junction Temperature . . . . +125°C
Power Dissipation . . . . See Curves
Pb-free Reflow Profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

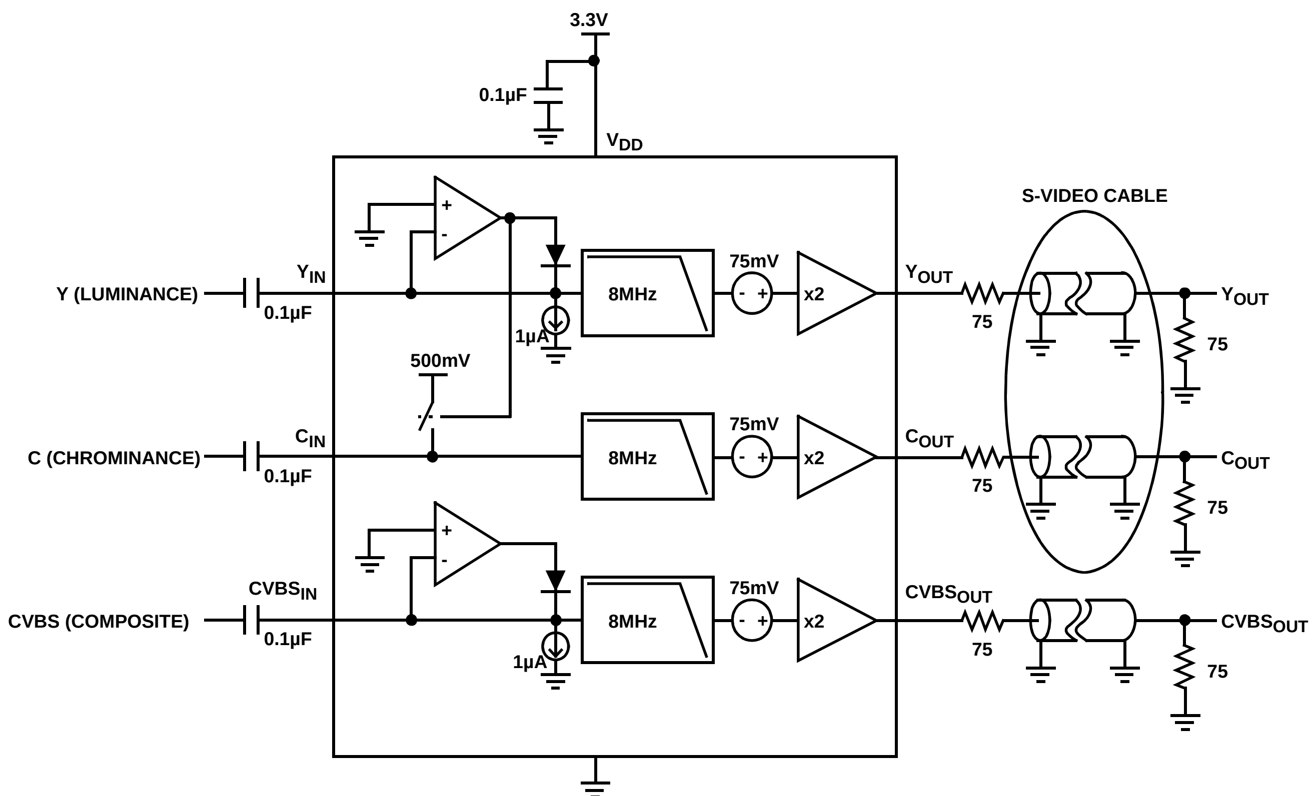
V_{DD} = 3.3V, T_A = +25°C, R_L = 150Ω to GND, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{DD}	Supply Voltage Range		3.0		5.5	V
I_{DD}	Quiescent Supply Current	V_{DD} = 3.3V, V_{IN} = 500mV, no load		8.4	11.5	mA
		V_{DD} = 5.5V, V_{IN} = 500mV, no load		9.5	12.5	mA
V_{Y_CLAMP}	Y Input Clamp Voltage	I_Y = -100µA	-40	0	+40	mV
I_{Y_DOWN}	Y Input Pull-down Current	V_Y = 0.5V	0.5	1	2	µA
I_{Y_CLAMP}	Y Input Clamp Pull-up Current	V_Y = -0.2V		-2.6	-1.5	mA
R_Y	Y Input Resistance	0.5V < V_Y < 1V		10		MΩ
V_{CVBS_CLAMP}	CVBS Input Clamp Voltage	I_{CVBS} = -100µA	-40	0	40	mV
I_{CVBS_DOWN}	CVBS Input Pull-down Current	V_{CVBS} = 0.5V	0.5	1	2	µA
I_{CVBS_CLAMP}	CVBS Input Clamp Pull-up Current	V_{CVBS} = -0.2V		-2.6	-1.5	mA
R_{CVBS}	CVBS Input Resistance	0.5V < V_{CVBS} < 1V		10		MΩ
V_{C_CLAMP}	C Input Clamp Voltage	V_Y < 0.08V, I_C = 0A	420	550	650	mV
I_{C_DOWN}	C Input Clamp Pull-down Current	V_C = 1V, V_Y < 0.08V	-60	-40	-25	µA
I_{C_UP}	C Input Clamp Pull-up Current	V_C = 0V, V_Y < 0.08V	25	40	60	µA
R_C	C Input Resistance	V_Y < 0.08V, 0.25V < V_C < 0.75V	5	7	10	kΩ
I_C	C Input Bias Current	V_Y > 0.2V	-150	0	+150	nA
V_{Y_SYNC}	Y Input Sync Detect Voltage		80	145	200	mV
A_V	Voltage Gain	R_L = 150Ω	1.95	2.0	2.04	V/V
ΔA_V	C-Y-CVBS Channel Mismatch		-2		+2	%
PSRR	DC Power Supply Rejection	V_{DD} = 3.3V	35	44		dB
		V_{DD} = 5.0V	45	48		dB
V_{OS}	Output Level Shift Voltage	V_{IN} = 0V, no load	60	150	240	mV
V_{OH}	Output Voltage High Swing	V_{IN} = 2V, R_L = 75Ω to GND (dual load)	2.6	3.1		V
I_{SC}	Output Short-Circuit Current	V_{IN} = 2V, to GND through 10Ω, sourcing	65			mA
		V_{IN} = 100mV, out short to V_{DD} through 10Ω	65			mA
AC PERFORMANCE						
PB	Passband Flatness	f = 4.2MHz relative to 1.1MHz, R_L = 150Ω, C_L = 5pF	-1	0	+1	dB
BW	-3dB Bandwidth	R_L = 150Ω, C_L = 5pF		8		MHz

Electrical Specifications V_{DD} = 3.3V, T_A = +25°C, R_L = 150Ω to GND, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SB	Normalized Stopband Gain	f = 27MHz relative to 1.1MHz	-60	-50	-40	dB
dG	Differential Gain	NTSC and PAL		0.2		%
dP	Differential Phase	NTSC and PAL		0.5		°
D/DT	Group Delay Variation	f = 100kHz, 5MHz		5.4		ns
XTALK	Crosstalk	f = 1MHz, between any two channels		-70		dB
R_{OUT_AC}	Output Impedance	f = 4.2MHz		1.5		Ω
+SR	Positive Slew Rate	10% to 90%, V_{IN} = 1V step	15	25	45	V/µs
-SR	Negative Slew Rate	90% to 10%, V_{IN} = 1V step	15	20	45	V/µs

Connection Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	Y_{IN}	Luminance Input
2	C_{IN}	Chrominance input
3	$CVBS_{IN}$	Composite Video input
4	V_{DD}	Positive power supply
5	GND	Ground
6	$CVBS_{OUT}$	Composite Video output
7	C_{OUT}	Chrominance output
8	Y_{OUT}	Luminance output

Typical Performance Curves

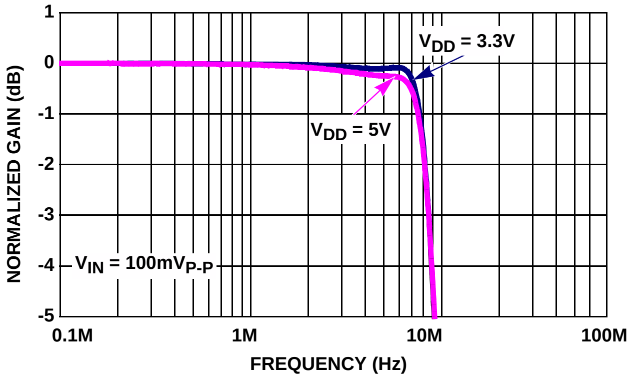


FIGURE 1. SMALL SIGNAL GAIN vs FREQUENCY -0.1dB

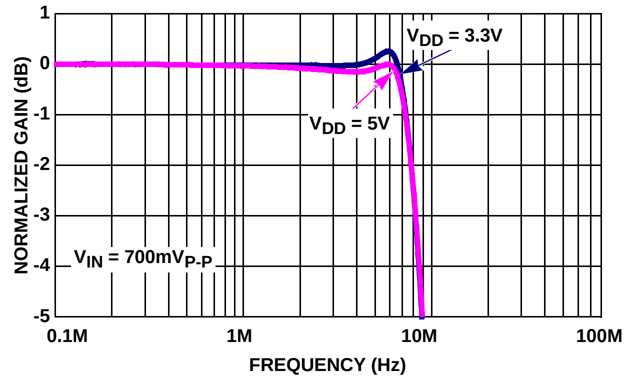


FIGURE 2. LARGE SIGNAL GAIN vs FREQUENCY -0.1dB

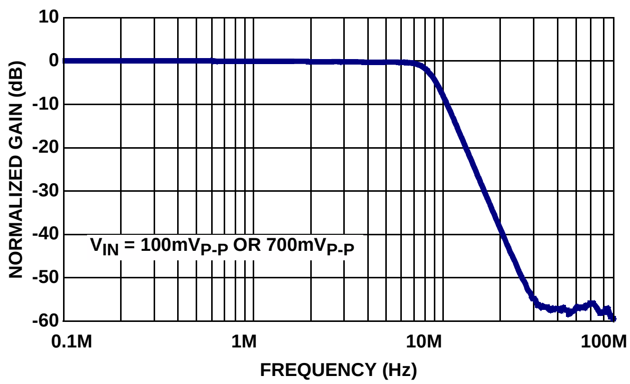


FIGURE 3. GAIN vs FREQUENCY -3dB POINT

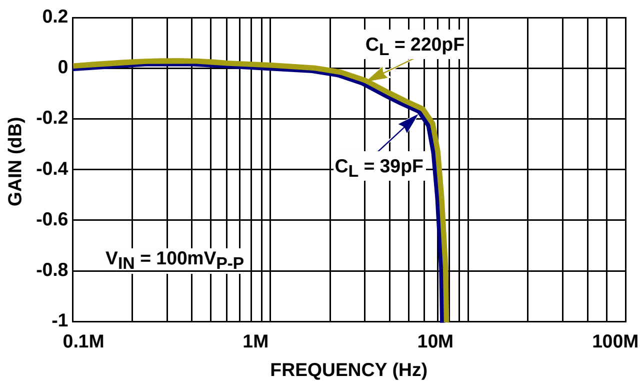


FIGURE 4. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD}

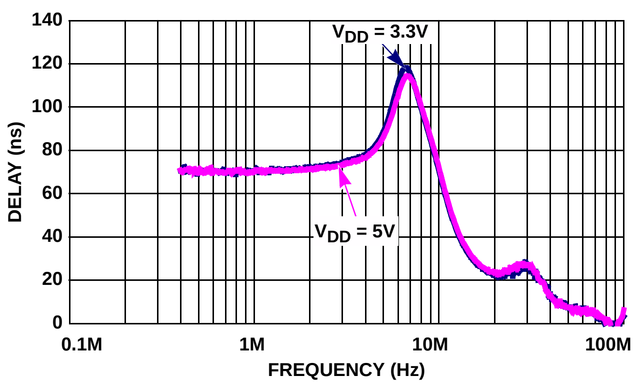


FIGURE 5. GROUP DELAY vs FREQUENCY

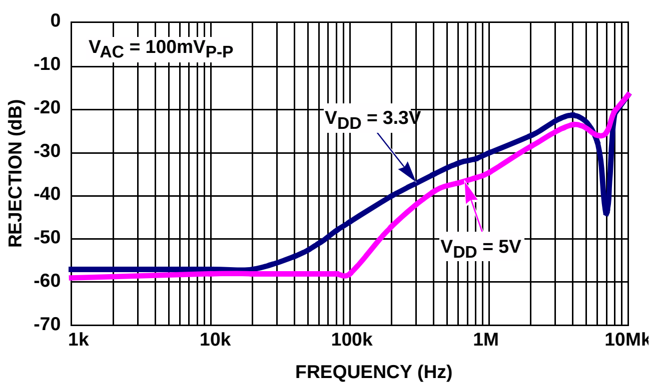


FIGURE 6. PSRR vs FREQUENCY

Typical Performance Curves (Continued)

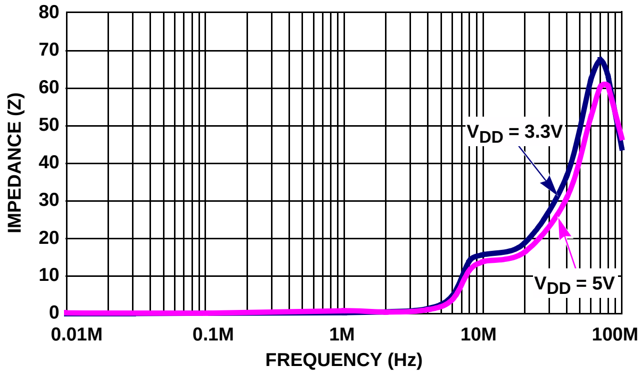


FIGURE 7. OUTPUT IMPEDANCE vs FREQUENCY

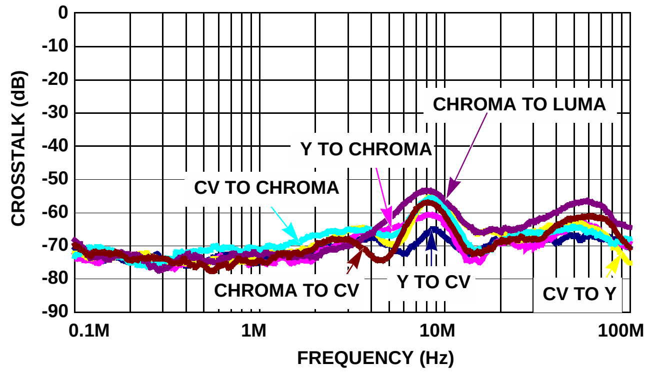


FIGURE 8. CROSSTALK vs FREQUENCY

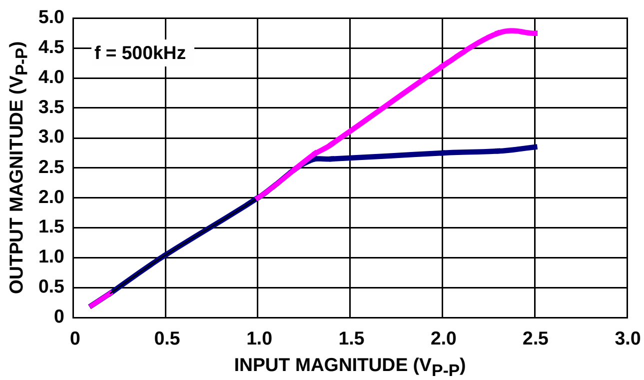


FIGURE 9. MAXIMUM OUTPUT MAGNITUDE vs INPUT MAGNITUDE

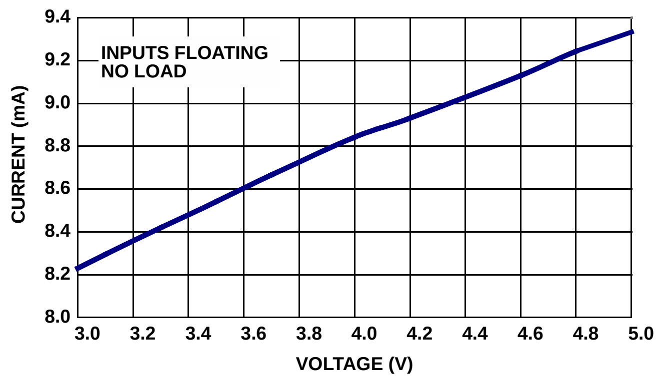


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

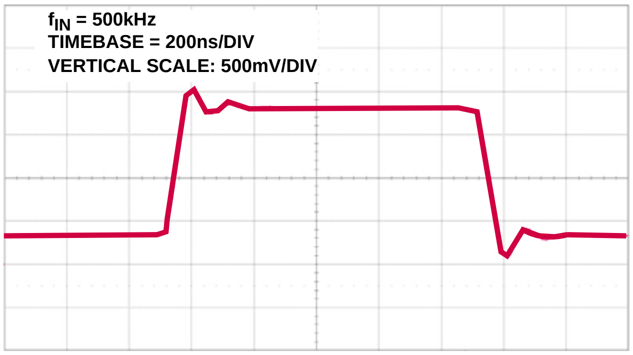


FIGURE 11. LARGE SIGNAL STEP RESPONSE

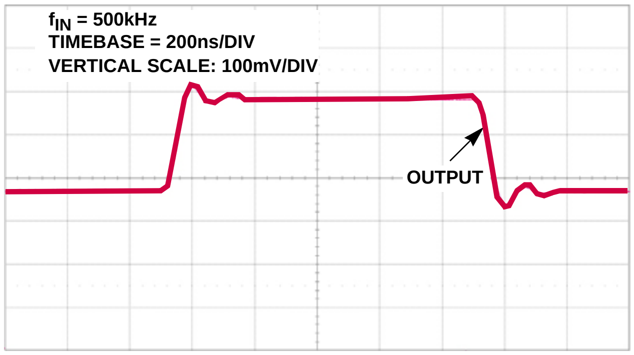


FIGURE 12. SMALL SIGNAL PULSE RESPONSE

Typical Performance Curves (Continued)

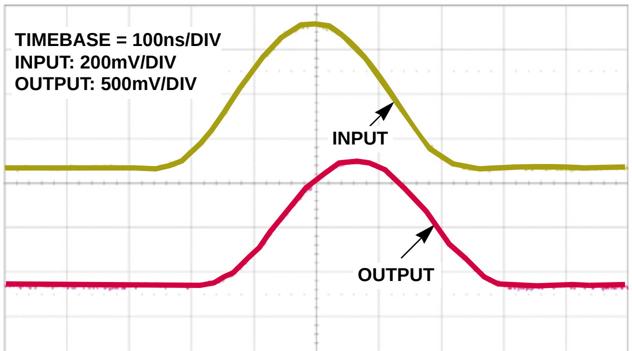


FIGURE 13. 2T RESPONSE

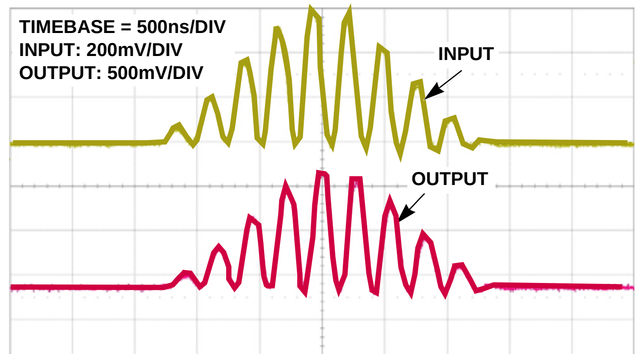


FIGURE 14. 12.5T RESPONSE

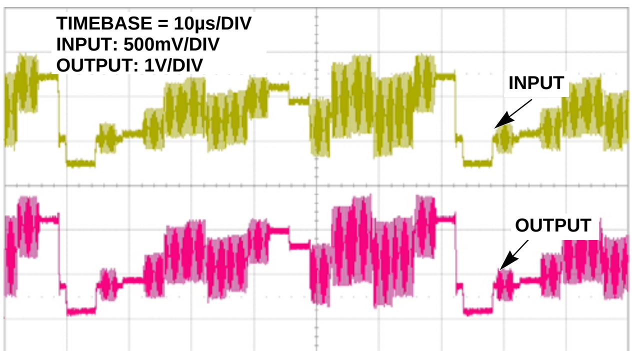


FIGURE 15. NTSC COLOR BAR

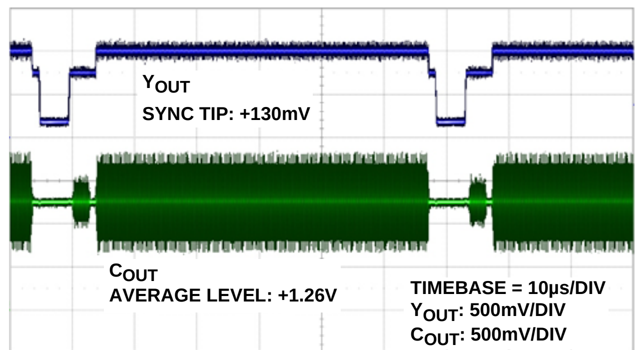


FIGURE 16. S-VIDEO OUTPUT

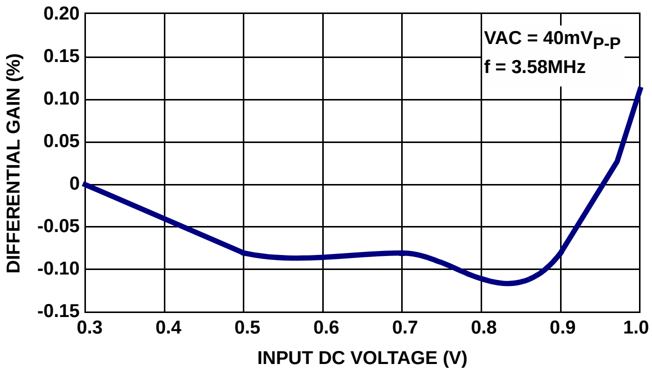


FIGURE 17. DIFFERENTIAL GAIN

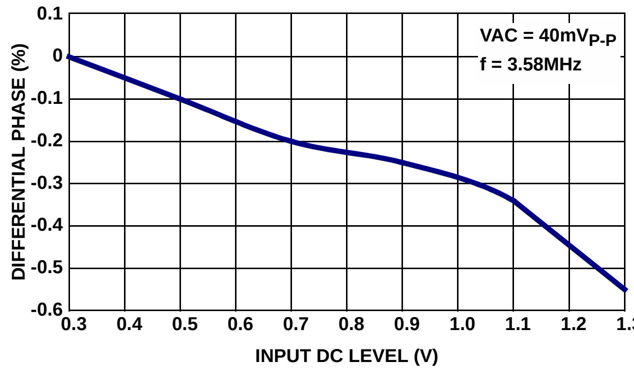


FIGURE 18. DIFFERENTIAL PHASE

Typical Performance Curves (Continued)

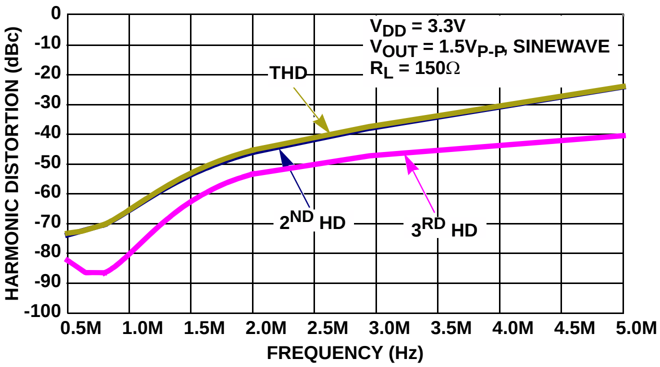


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY

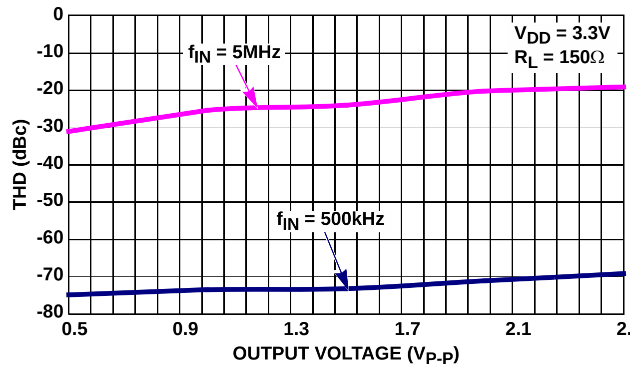


FIGURE 20. HARMONIC DISTORTION vs OUTPUT VOLTAGE

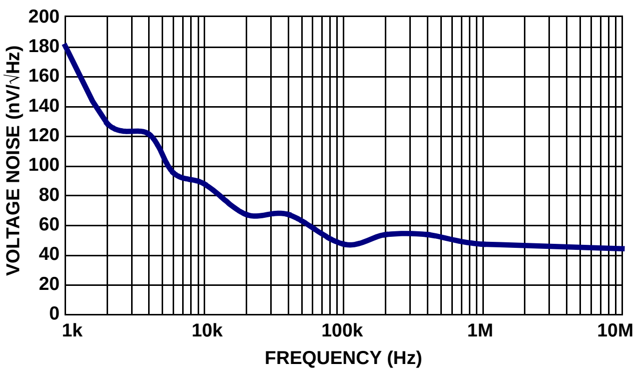


FIGURE 21. OUTPUT VOLTAGE NOISE vs FREQUNCY

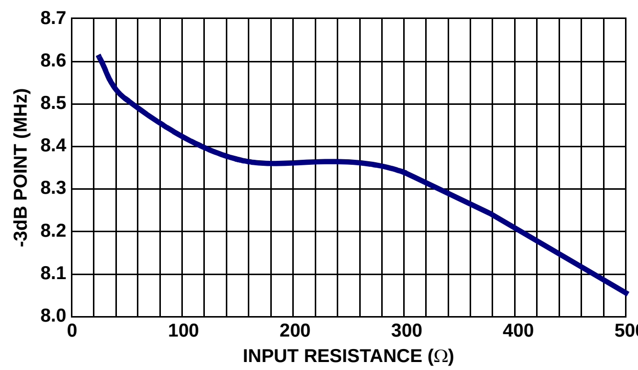


FIGURE 22. -3dB BANDWIDTH vs INPUT RESISTANCE

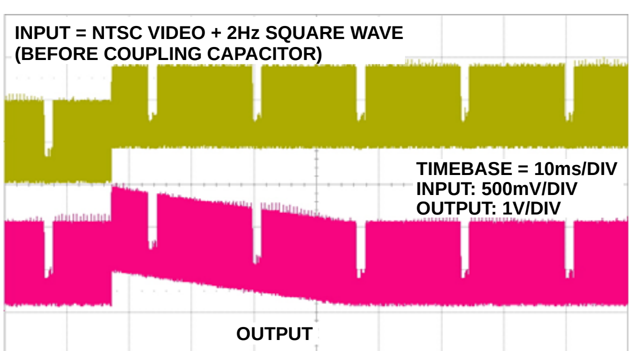


FIGURE 23. RESPONSE TO +500mV DC STEP ON INPUT (SEE FIGURE 27)

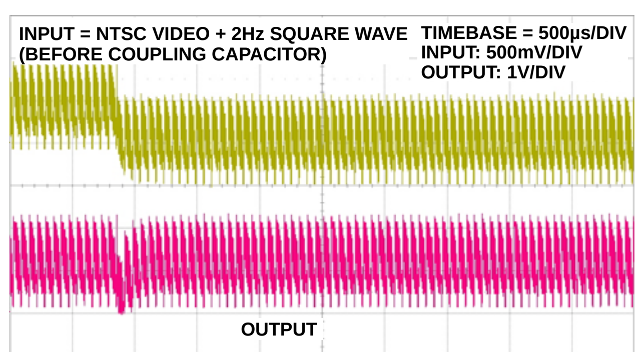


FIGURE 24. RESPONSE TO -500mV DC STEP ON INPUT (SEE FIGURE 27)

Typical Performance Curves (Continued)

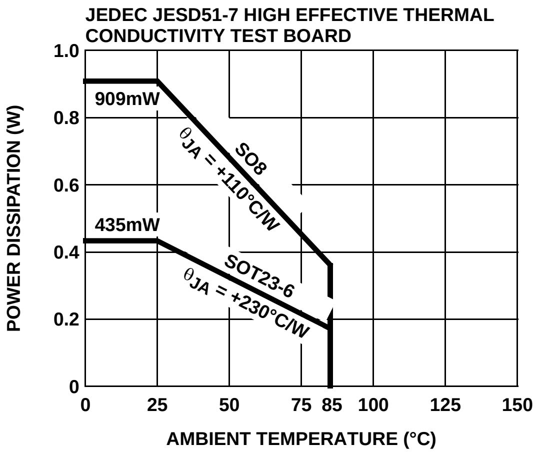


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

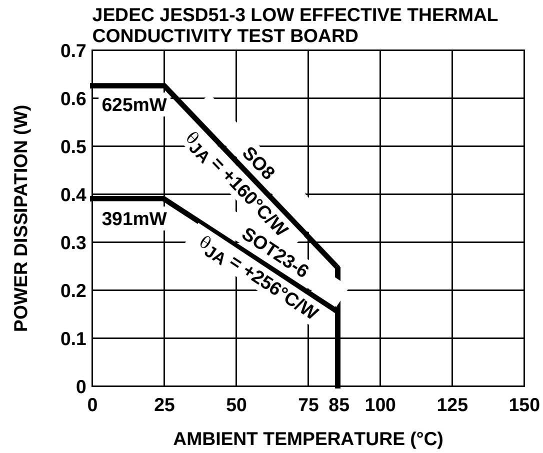


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Application Information

The ISL59119 is a single-supply rail-to-rail triple (one S-video channel and one composite channel) video amplifier with internal sync tip clamps, a typical -3dB bandwidth of 8MHz and slew rate of about 25V/µs. This part is ideally suited for applications requiring high composite and S-video performance with very low power consumption. As the performance characteristics and features illustrate, the ISL59119 is optimized for portable video applications.

Internal Sync Clamp

Embedded video DACs typically use ground as their most negative supply. This places the sync tip voltage at a minimum of 0V. Presenting a 0V input to most single supply amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degraded video image.

The ISL59119 features an internal sync clamp and offset function that level shifts the entire video signal to the optimum level before it reaches the amplifiers' input stage. These features also help avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram on page 1 shows the basic operation of the ISL59119's sync clamp. The Y and CVBS inputs' AC-coupled video sync signal is pulled negative by a current source at the input. When the sync tip goes below the comparator threshold, the comparator output goes high, pulling up on the input through the diode, forcing current into the coupling capacitor until the voltage at the input is again 0V, and the comparator turns off. This forces the sync tip clamp to always be 0V, setting the offset for the entire video signal. The C-Channel is slaved to the Y-Channel and clamped to a 500mV level at the input.

Figure 27 shows the setup for testing the clamp's response to a large step response at the input.

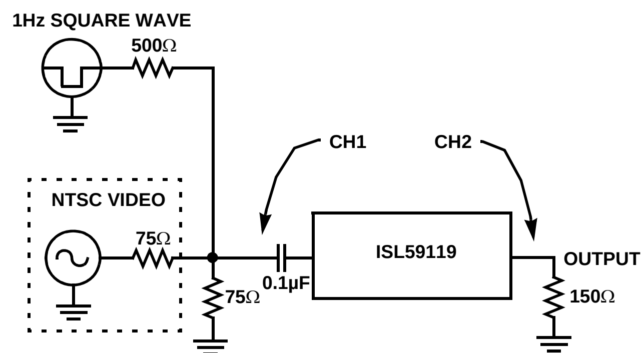


FIGURE 27. DC STEP RESPONSE CIRCUIT

Once the signals are clamped at the input they are level shifted by +65mV before being amplified by a gain of x2.

The Sallen Key Low Pass Filter

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the ISL59119, a three-pole roll-off at 8MHz. The three-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key. The first pole is formed by an RC network, with poles two and three generated with a Sallen Key, creating a nice three-pole roll-off at 8MHz.

Output Coupling

The ISL59119 can be AC or DC coupled to its output. When AC coupling, a 220µF coupling capacitor is recommended to ensure that low frequencies are passed, preventing video "tilt" or "droop" across a line.

The ISL59119's internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, saving board space, cost, and eliminating any "tilt" or offset shift in the output signal. The trade-off is larger supply current draw, since the DC component of the signal is now dissipated in the load resistor. Typical load current for AC coupled signals is 5mA compared to 10mA for DC coupling.

Output Drive Capability

The ISL59119 does not have internal short circuit protection circuitry. If the output is shorted indefinitely, the power dissipation could easily overheat the die or the current could eventually compromise metal integrity. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnect. Note that for transient short circuits, the part is robust.

Short circuit protection can be provided externally with a back match resistor in series with the output placed close as possible to the output pin. In video applications this would be a 75Ω resistor and will provide adequate short circuit protection to the device. Care should still be taken not to stress the device with a short at the output.

Power Dissipation

With the high output drive capability of the ISL59119, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

Θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing use Equation 2:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad \text{(EQ. 2)}$$

for sinking use Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S) \times I_{LOAD} \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

Power Supply Bypassing Printed Circuit Board Layout

As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice.

Printed Circuit Board Layout

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance.

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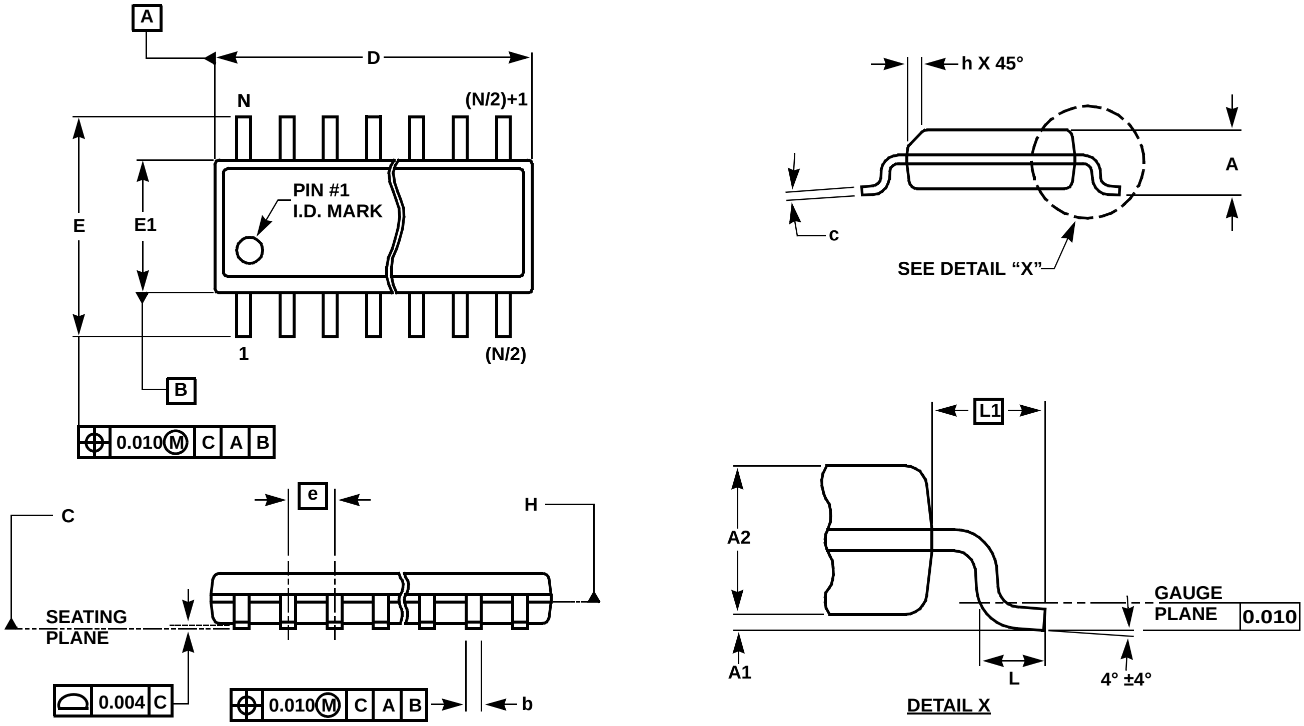
Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994