Data Sheet | March 11, 2008 | FN6616.0

2A Low Quiescent Current 1MHz High Efficiency Synchronous Buck Regulator

The ISL8012 is a high efficiency, monolithic, synchronous step-down DC/DC converter that can deliver up to 2A continuous output current from a 2.7V to 5.5V input supply. It uses a current control architecture to deliver very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL8012 integrates a pair of low ON-resistance P-Channel and N-Channel internal MOSFETs to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 240mV dropout voltage at 2A output current. High 1MHz pulse-width modulation (PWM) switching frequency allows the use of small external components.

The ISL8012 can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference while discontinuous mode provides high efficiency by reducing switching losses at light loads.

Fault protection is provided by internal current limiting during short circuit and overcurrent conditions, an output over voltage comparator and over-temperature monitor circuit. A power good output voltage monitor indicates when the output is in regulation.

The ISL8012 offers a 1ms Power Good (PG) timer at power-up. When shutdown, ISL8012 discharges the output capacitor. Other features include internal soft-start, internal compensation, overcurrent protection, and thermal shutdown.

The ISL8012 is offered in a space saving 3mmx3mm 10 Ld DFN package lead free package with exposed pad lead frames for low thermal. The complete converter occupies less than 0.35in^2 area.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL8012IRZ*	012Z	-40 to +85	10 Ld 3x3 DFN	L10.3x3C

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

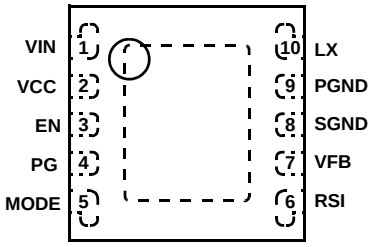
- High Efficiency Synchronous Buck Regulator with up to 95% Efficiency
- Power-Good (PG) Output with a 1ms Delay
- 2.7V to 5.5V Supply Voltage
- 3% Output Accuracy Over-Temperature/Load/Line
- 2A Guaranteed Output Current
- Start-up with Pre-Biased Output
- Internal Soft-Start - 1ms
- Soft-Stop Output Discharge During Disabled
- 40µA Quiescent Supply Current in PFM Mode
- Selectable Forced PWM Mode and PFM Mode
- Less than 1µA Logic Controlled Shutdown Current
- 100% Maximum Duty Cycle
- Internal Current Mode Compensation
- Peak Current Limiting and Hiccup Mode Short Circuit Protection
- Over-Temperature Protection
- Small 10 Ld 3mmx3mm DFN
- Pb-Free (RoHS Compliant)

Applications

- DC/DC POL Modules
- µC/µP, FPGA and DSP Power
- Plug-in DC/DC Modules for Routers and Switchers
- Portable Instruments
- Test and Measurement Systems
- Li-ion Battery Powered Devices
- Small Form Factor (SFP) Modules
- Bar Code Readers

Pinout

ISL8012
(10 LD DFN)
TOP VIEW



Typical Application

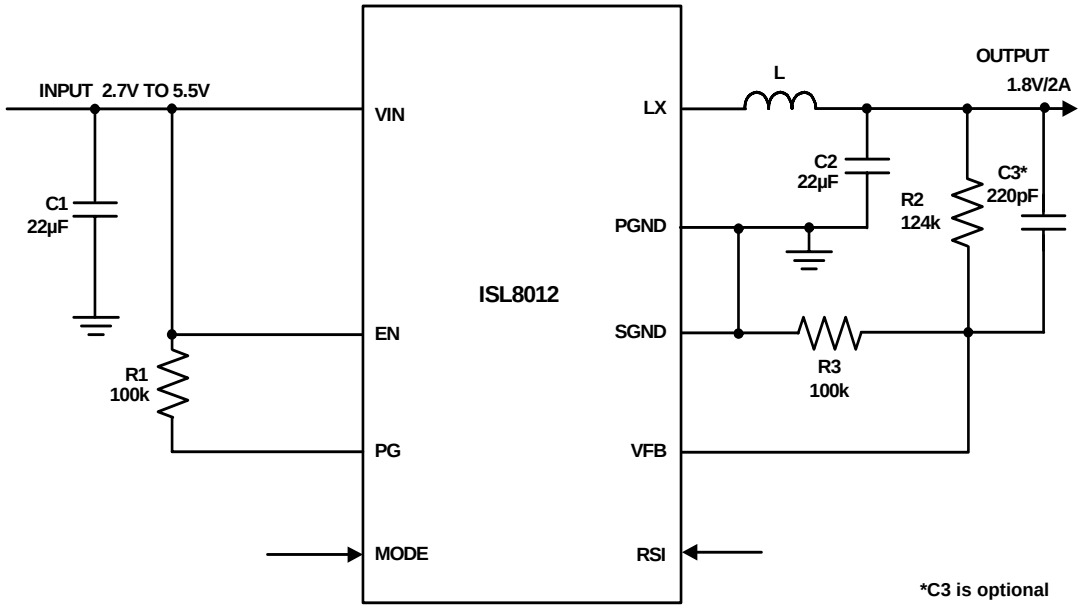


FIGURE 1. TYPICAL APPLICATION DIAGRAM

Block Diagram

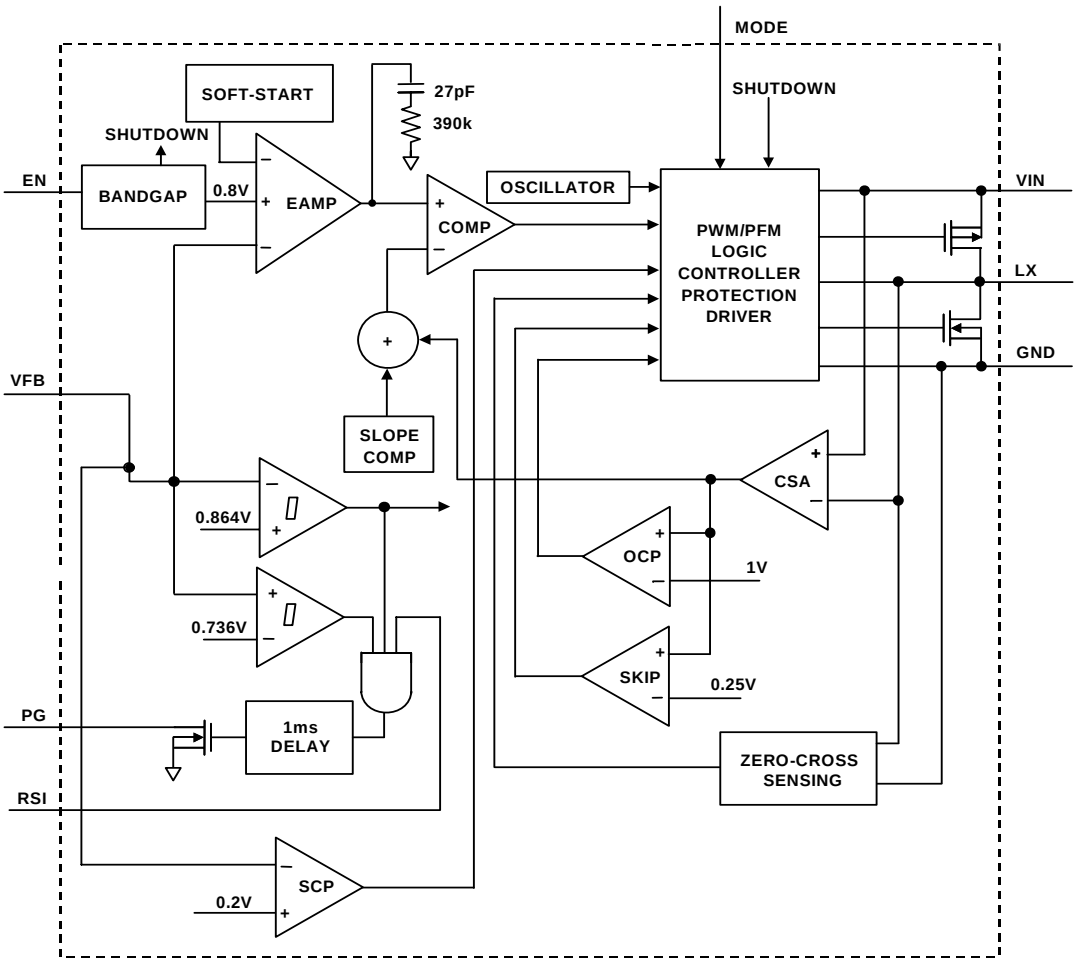


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Absolute Maximum Ratings (Reference to GND)

VIN, VCC . . . . . -0.3V to 6V
EN, RSI, PG. . . . . -0.3V to VIN+0.3V
LX. . . . . -1.5V (100ns)/-0.3V (DC) to 6.5V
VFB . . . . . -0.3V to 2.7V

Recommended Operating Conditions

V_{IN} Supply Voltage Range. . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 2A
Ambient Temperature Range. . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package	49	5.5

Junction Temperature Range. . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.
3. Limits established by characterization and are not production tested.
4. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Electrical Specifications

Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = VCC, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
INPUT SUPPLY						
VIN Under Voltage Lockout Threshold	V_{UVLO}	Rising		2.5	2.7	V
		Falling	2.2	2.4		V
Quiescent Supply Current	I_{VIN}	MODE = VIN, no load at the output		40	60	µA
		MODE = VIN, no load at the output and no switches switching; design info only		15		µA
		MODE = SGND, no load at the output		6	8	mA
Shut Down Supply Current	I_{SD}	V_{IN} = 5.5V, EN = low		0.1	2	µA
OUTPUT REGULATION						
VFB Regulation Voltage	V_{VFB}	T_A = 0°C to +85°C	0.784	0.8	0.816	V
VFB Bias Current	I_{VFB}	VFB = 0.75V		0.1		µA
Output Voltage Accuracy		$V_{IN} = V_O$ + 0.5V to 5.5V, I_O = 0A to 2A (Note 3)	-3		3	%
Line Regulation		$V_{IN} = V_O$ + 0.5V to 5.5V (minimal 2.7V), I_{OUT} = 400mA		0.2		%/V
COMPENSATION						
Error Amplifier Trans-Conductance		Adjustable version, design info only		20		µA/V
LX						
P-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		0.12	0.22	Ω
		V_{IN} = 2.7V, I_O = 200mA		0.21	0.27	Ω
N-Channel MOSFET ON-Resistance		V_{IN} = 5.5V, I_O = 200mA		0.11	0.22	Ω
		V_{IN} = 2.7V, I_O = 200mA		0.13	0.27	Ω
P-Channel MOSFET Peak Current Limit	I_{PK}		2.65	3.00	3.50	A
LX Maximum Duty Cycle				100		%
PWM Switching Frequency	f_S	T_A = 0°C to +85°C	0.840	1	1.16	MHz

Electrical Specifications Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specifications are measured at the following conditions: T_A = -40°C to +85°C, V_{IN} = 3.6V, EN = VCC, unless otherwise noted. Typical values are at T_A = +25°C. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
LX Minimum On-Time		MODE = low (forced PWM mode)		80	100	ns
Soft-Start-Up Time		V_{IN} = 3.6V		1.1		ms
PG						
Output Low Voltage		Sinking 1mA, VFB = 0.7V			0.3	V
Delay Time				1		ms
PG Pin Leakage Current		PG = VIN = 3.6V		0.01	0.1	µA
Minimum Supply Voltage for Valid PG Signal			1.2			V
Internal PGOOD Low Rising Threshold		Percentage of nominal regulation voltage	89	92	95	%
Internal PGOOD Low Falling Threshold		Percentage of nominal regulation voltage	85	88	91	%
Internal PGOOD High Rising Threshold		Percentage of nominal regulation voltage	107	110	113	%
Internal PGOOD High Falling Threshold		Percentage of nominal regulation voltage	104	107	110	%
Internal PGOOD Delay Time				30		µs
EN, MODE, RSI						
Logic Input Low					0.4	V
Logic Input High			1.4			V
Logic Input Leakage Current		Pulled up to 5.5V		0.1	1	µA

Pin Descriptions

VIN (Pin 1)

Input supply voltage. Connect a 10µF ceramic capacitor to power ground.

VCC (Pin 2)

Input supply for the logic. Connect to VIN.

EN (Pin 3)

Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low. Do not leave this pin floating.

PG (Pin 4)

1ms timer output. At power-up or EN HI, this output is a 1ms delayed Power-Good signal for the output voltage. This output can be reset by a low RSI signal. 1ms starts when RSI goes to high.

MODE (Pin 5)

Mode Selection pin. Connect to logic high or input voltage VIN for PFM mode; connect to logic low or ground for forced PWM mode. Do not leave this pin floating.

RSI (Pin 6)

This input resets the 1ms timer. When the output voltage is within the PGOOD window, an internal timer is started and generates a PG signal 1ms later when RSI is low. A high RSI resets PG and RSI high to low transition restarts the internal counter if the output voltage is within the window, otherwise the counter is reset by the output voltage condition.

VFB (Pin 7)

Buck regulator output feedback. Connect to the output through a resistor divider for adjustable output voltage (ISL8012-ADJ). For preset output voltage, connect this pin to the output.

SGND (Pin 8)

System ground for the control logic. All voltage levels are measured with respect to this pin.

PGND (Pin 9)

Ground connect for the IC and thermal relief for the package. The exposed pad must be connected to PGND and soldered to the PCB.

LX (Pin 10)

Switching node connection. Connect to one terminal of inductor.

Exposed Pad

The exposed pad must be connected to the PGND and SGND pin for proper electrical performance. The exposed pad must also be connected to as much as possible for optimal thermal performance.

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.5V to 5.5V, EN = V_{IN}, MODE = 0V, L = 1.5µH, C_1 = 2x10µF, C_2 = 2x10µF, I_{OUT} = 0A to 2A).

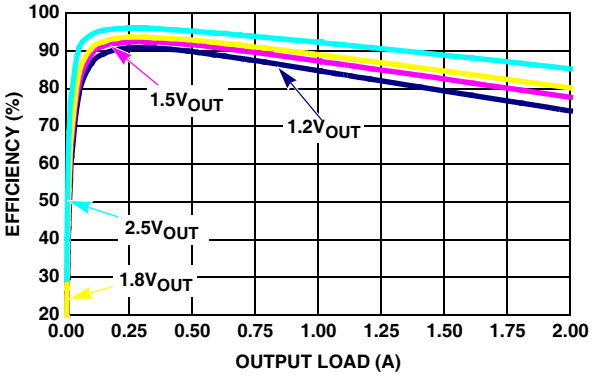


FIGURE 3. EFFICIENCY vs LOAD (1MHz 3.3V_{IN} PWM)

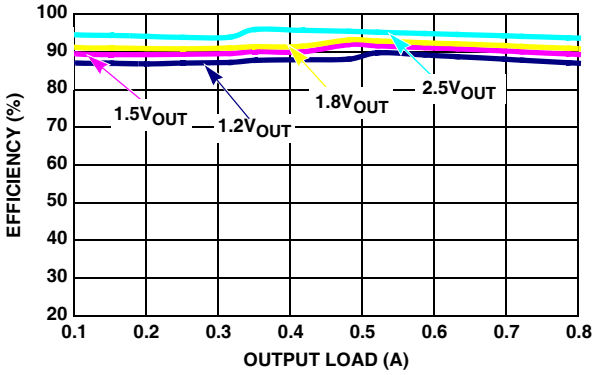


FIGURE 4. EFFICIENCY vs LOAD (1MHz 3.3V_{IN} PFM)

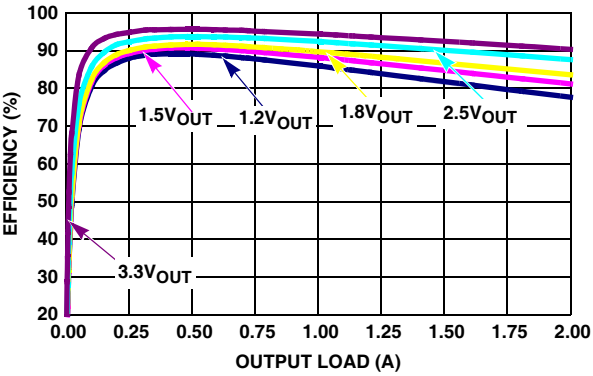


FIGURE 5. EFFICIENCY vs LOAD (1MHz 5V_{IN} PWM)

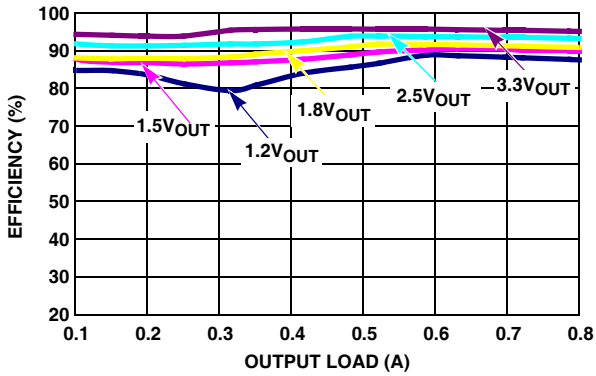


FIGURE 6. EFFICIENCY vs LOAD (1MHz 5V_{IN} PFM)

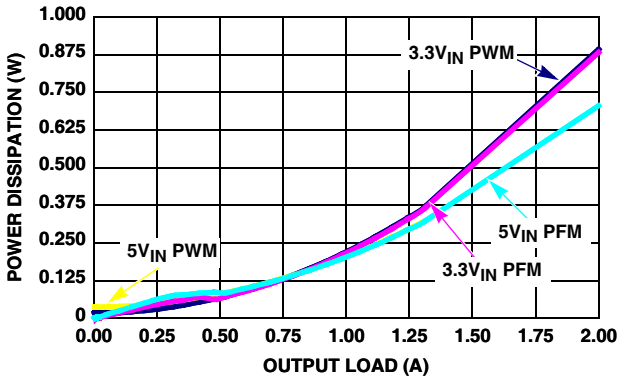


FIGURE 7. POWER DISSIPATION vs LOAD (1MHz, V_{OUT} = 1.8V)

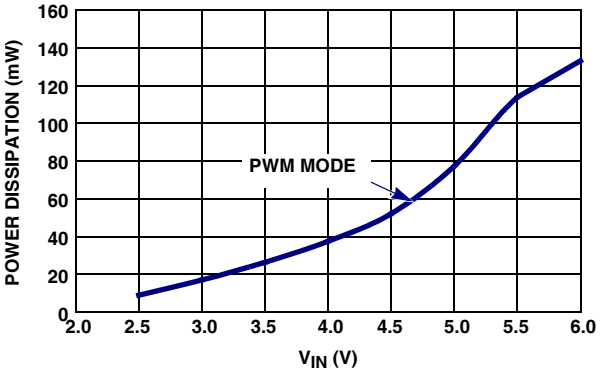


FIGURE 8. POWER DISSIPATION WITH NO LOAD vs V_{IN} (PWM V_{OUT} = 1.8V)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.5V to 5.5V, EN = V_{IN}, MODE = 0V, L = 1.5µH, C_1 = 2x10µF, C_2 = 2x10µF, I_{OUT} = 0A to 2A). **(Continued)**

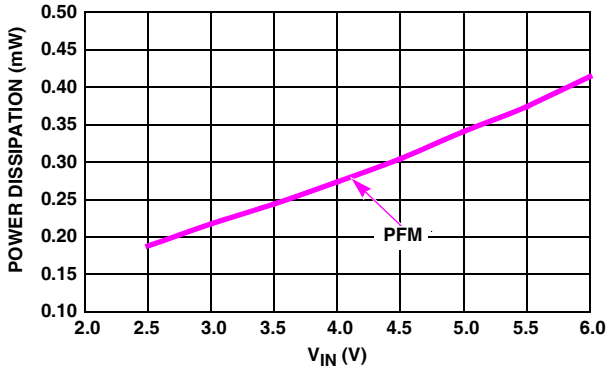


FIGURE 9. POWER DISSIPATION WITH NO LOAD vs V_{IN} (PFM V_{OUT} = 1.8V)

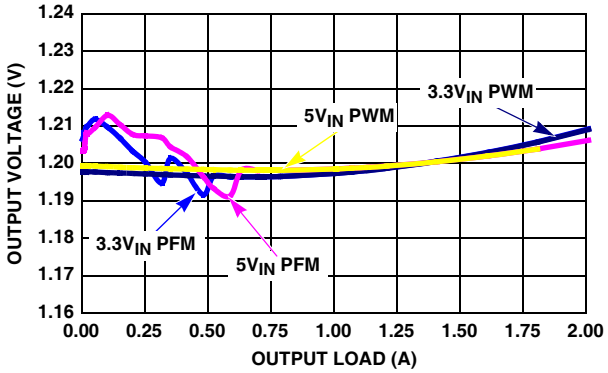


FIGURE 10. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.2V)

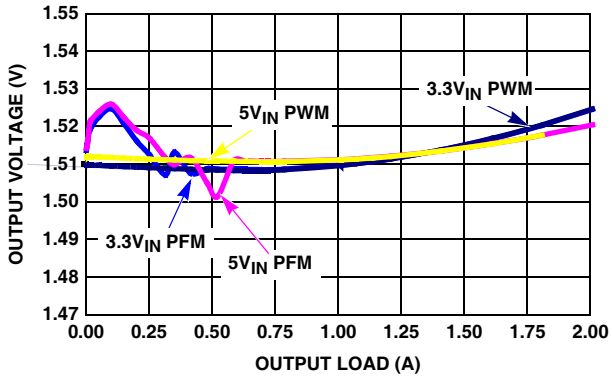


FIGURE 11. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.5V)

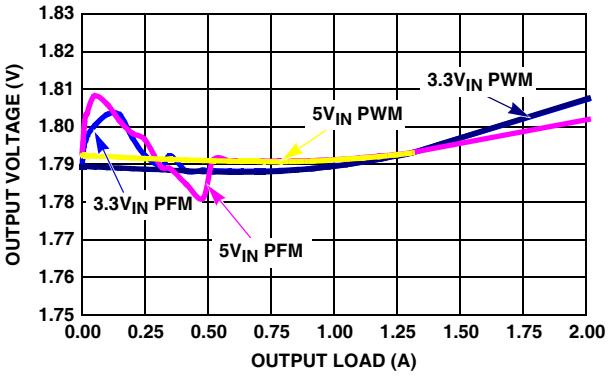


FIGURE 12. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 1.8V)

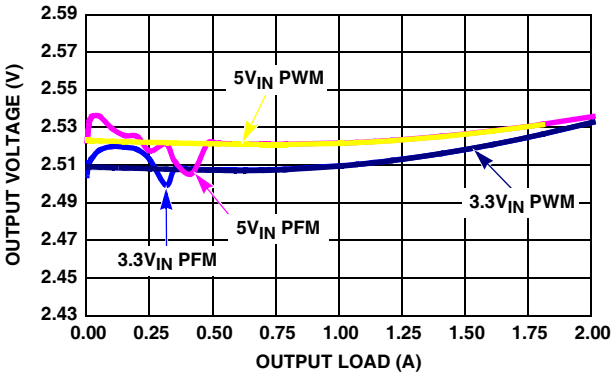


FIGURE 13. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 2.5V)

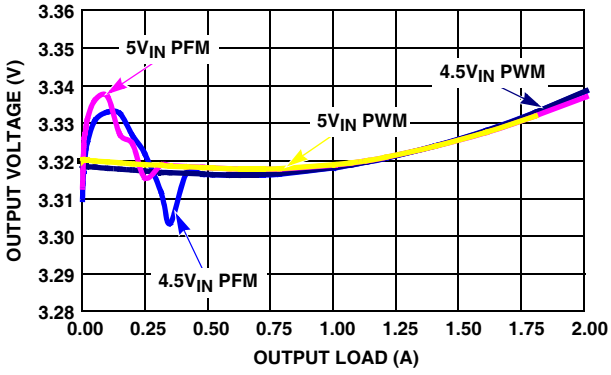


FIGURE 14. V_{OUT} REGULATION vs LOAD (1MHz, V_{OUT} = 3.3V)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.5V to 5.5V, EN = V_{IN}, MODE = 0V, L = 1.5µH, C_1 = 2x10µF, C_2 = 2x10µF, I_{OUT} = 0A to 2A). **(Continued)**

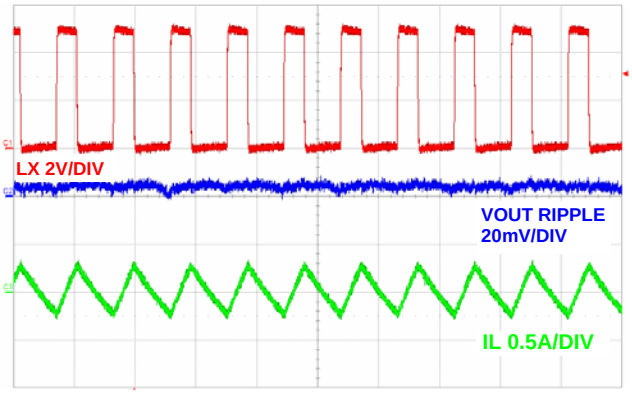


FIGURE 15. STEADY STATE OPERATION AT NO LOAD (PWM), (1µs/DIV)

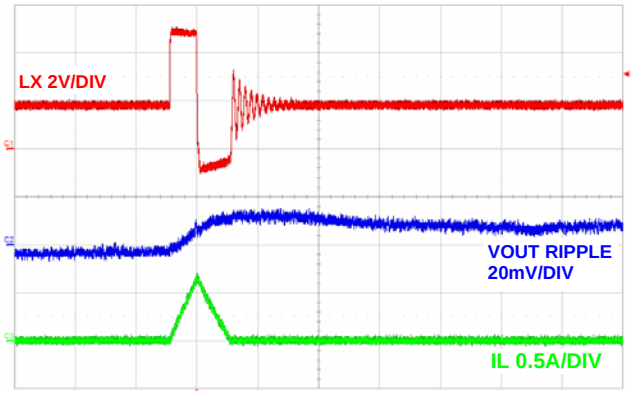


FIGURE 16. STEADY STATE OPERATION AT NO LOAD (PFM), (1µs/DIV)

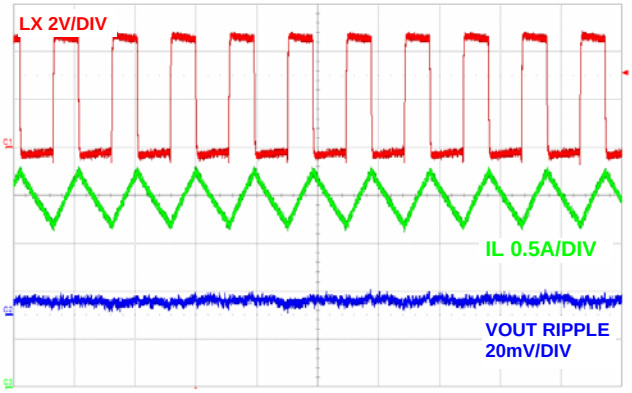


FIGURE 17. STEADY STATE OPERATION WITH FULL LOAD, (5µs/DIV)

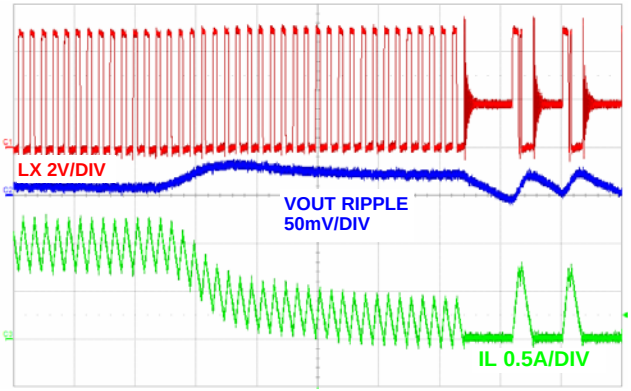


FIGURE 18. MODE TRANSITION CCM TO DCM, (5µs/DIV)

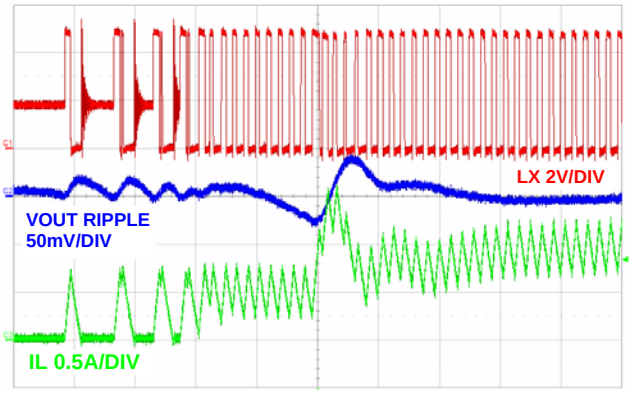


FIGURE 19. MODE TRANSITION DCM TO CCM, (50µs/DIV)

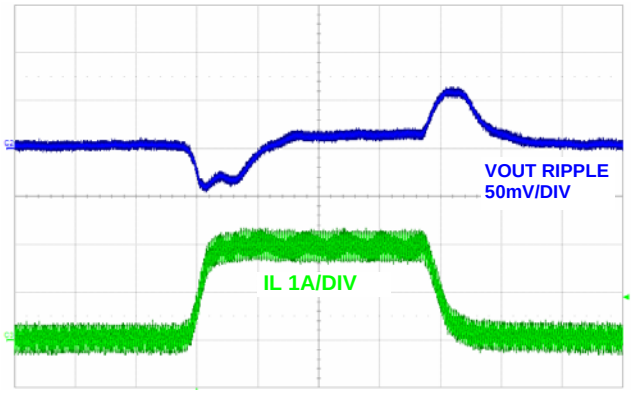


FIGURE 20. LOAD TRANSIENT (PWM), (50µs/DIV)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.5V to 5.5V, EN = V_{IN}, MODE = 0V, L = 1.5µH, C_1 = 2x10µF, C_2 = 2x10µF, I_{OUT} = 0A to 2A). **(Continued)**

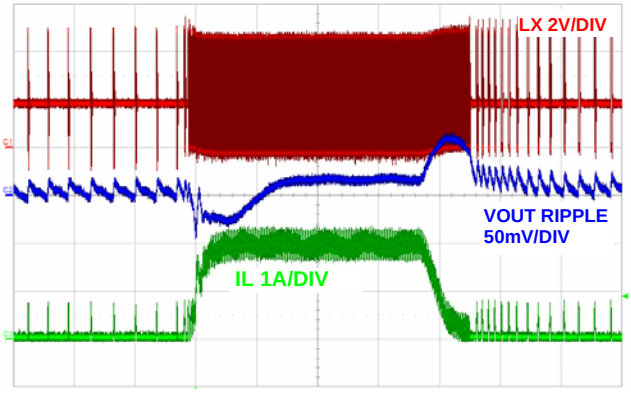


FIGURE 21. LOAD TRANSIENT (PFM), (500µs/DIV)

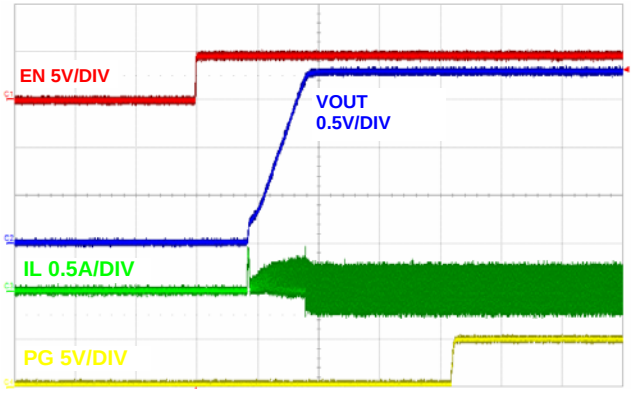


FIGURE 22. SOFT-START WITH NO LOAD (PWM), (500µs/DIV)

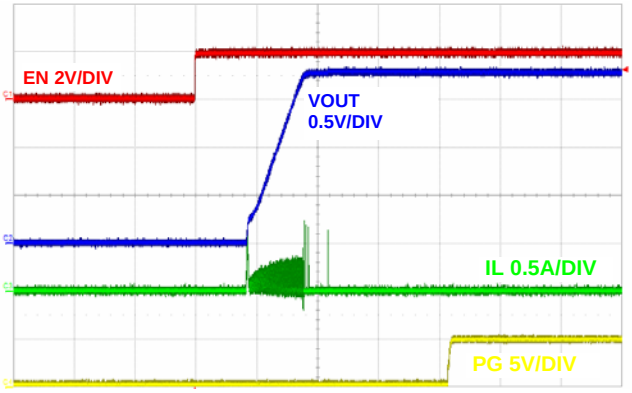


FIGURE 23. SOFT-START AT NO LOAD (PFM), (500µs/DIV)

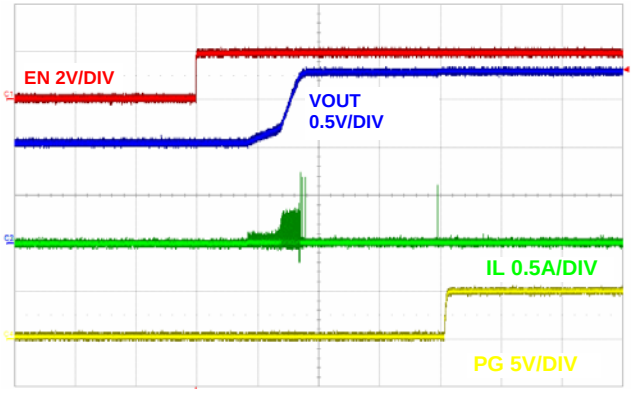


FIGURE 24. SOFT-START WITH PRE-BIASED 1V, (500µs/DIV)

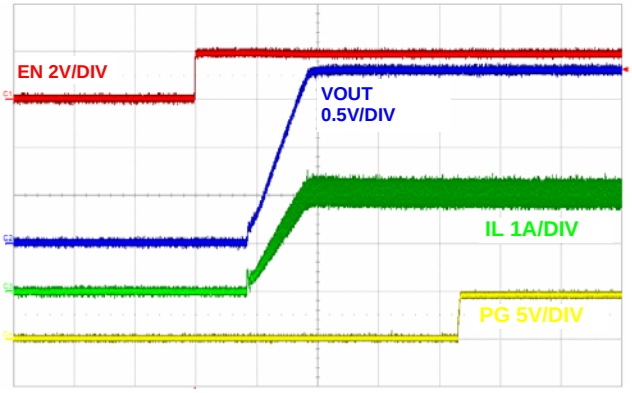


FIGURE 25. SOFT-START AT FULL LOAD, (2ms/DIV)

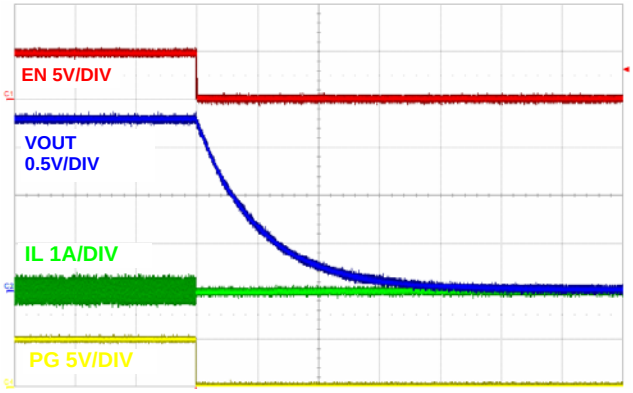


FIGURE 26. SOFT-DISCHARGE SHUTDOWN, (2ms/DIV)

Typical Operating Performance (Unless otherwise noted, operating conditions are: T_A = +25°C, V_{VIN} = 2.5V to 5.5V, EN = V_{IN}, MODE = 0V, L = 1.5µH, C_1 = 2x10µF, C_2 = 2x10µF, I_{OUT} = 0A to 2A). **(Continued)**

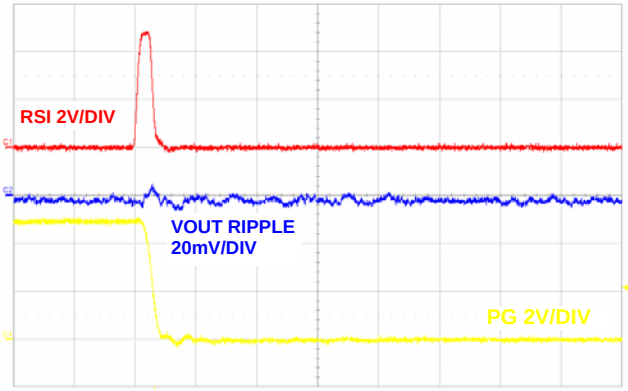


FIGURE 27. RSI RESET, (200µs/DIV)

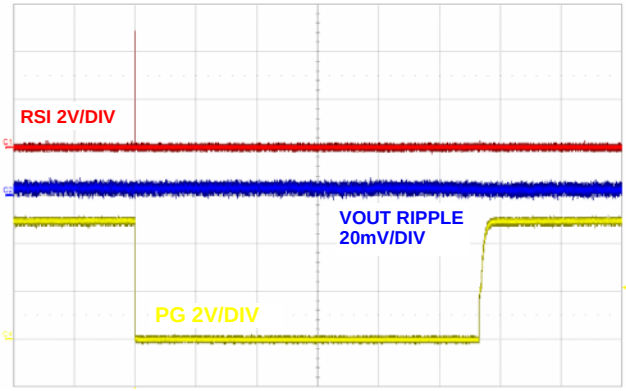


FIGURE 28. RSI RESET (ZOOM OUT), (200µs/DIV)

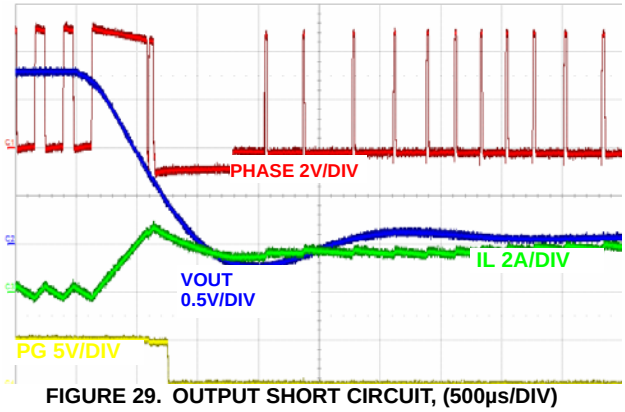


FIGURE 29. OUTPUT SHORT CIRCUIT, (500µs/DIV)

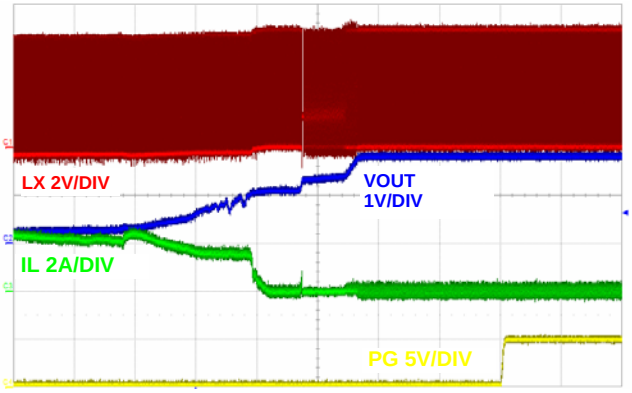


FIGURE 30. OUTPUT SHORT CIRCUIT RECOVERY, (500µs/DIV)

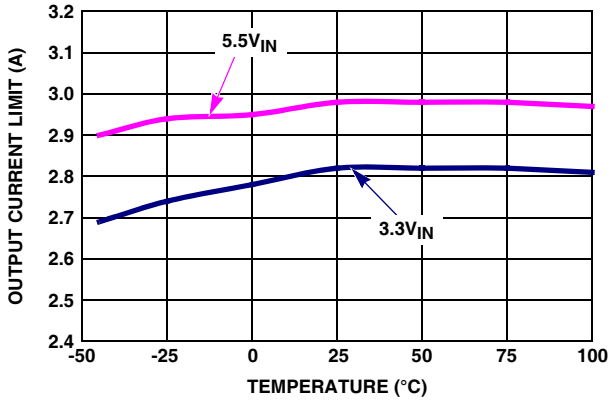


FIGURE 31. OUTPUT CURRENT LIMIT vs TEMPERATURE

Theory of Operation

The ISL8012 is a step-down switching regulator optimized for battery-powered handheld applications. The regulator operates at 1MHz fixed switching frequency under heavy load conditions to allow smaller external inductors and capacitors to be used for minimal printed-circuit board (PCB) area. At light load, the regulator reduces the switching frequency (unless forced to the fixed frequency) to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 40µA. The supply current is typically only 0.1µA when the regulator is shut down.

PWM Control Scheme

Pulling the MODE pin LOW (<0.4V) forces the converter into PWM mode, regardless of output current. The ISL8012 employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 2 shows the block diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The gain for the current sensing circuit is typically 285mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp-up. When the sum of the current amplifier CSA and the slope compensation (675mV/µs) reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-MOSFET and turn on the N-Channel MOSFET. The N-MOSFET stays on until the end of the PWM cycle. Figure 32 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.8V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 390kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.47V.

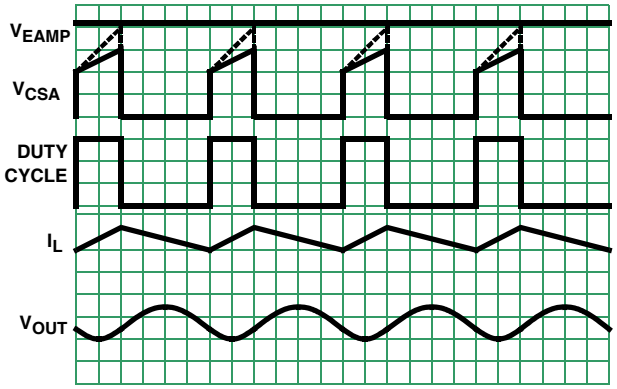


FIGURE 32. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the MODE pin HIGH (>1.4V) forces the converter into PFM mode. The ISL8012 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 33 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 2 monitors the N-MOSFET current for zero crossing. When 8 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the skip mode. During the 8 detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 2. Each pulse cycle is still synchronized by the PWM clock. The P-MOSFET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak Skip current limit value. Then the inductor current is discharging to zero Ampere and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-MOSFET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

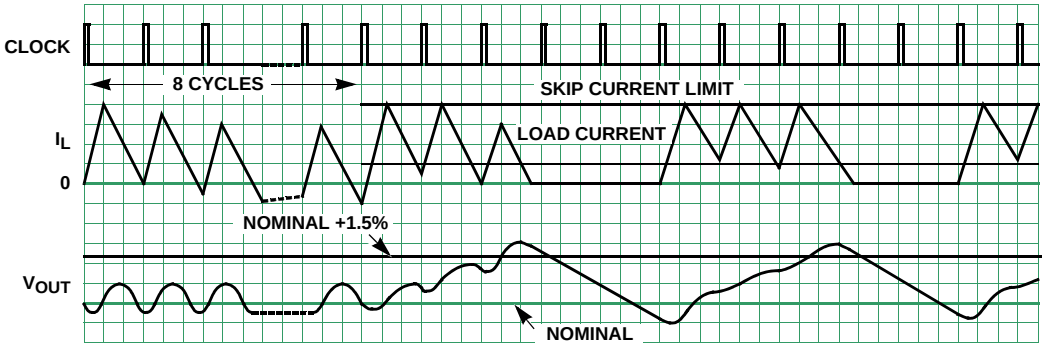


FIGURE 33. SKIP MODE OPERATION WAVEFORMS

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Mode Control

The ISL8012 has a MODE pin that controls the operation mode. When the MODE pin is driven to low or shorted to ground, the regulator operates in a forced PWM mode. The forced PWM mode remains the fixed PWM frequency at light load instead of entering the skip mode.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 2. The current sensing circuit has a gain of 285mV/A, from the P-MOSFET current to the CSA output. When the CSA output reaches 1V, which is equivalent to 2.9A for the switch current (0.15V offset), the OCP comparator is tripped to turn off the P-MOSFET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle.

Short-Circuit Protection

The short-circuit protection SCP comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.2V, the SCP comparator forces the PWM oscillator frequency to drop to minimum value to reduce the power dissipation. This comparator is effective during start-up or an output short-circuit event.

RSI/PG Function

When powering up, the open-collector Power-Good output holds low for about 1ms after V_O reaches the preset voltage. When the active-HI reset signal RSI is issued, PG goes to low immediately and holds for the same period of time after RSI comes back to LOW. The output voltage is unaffected. Please refer to the timing diagram in Figure 34. When the function is not used, connect RSI to ground and leave the pull-up resister R_4 open at the PG pin.

The PG output also serves as a 1ms delayed Power-Good signal when the pull-up resister R_1 is installed. The RSI pin needs to be directly (or indirectly through a resistor) connected to Ground for PG to be actively monitoring the output voltage.

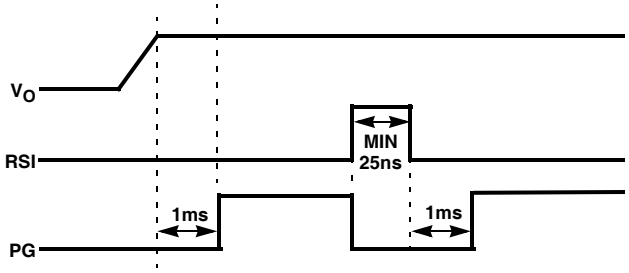


FIGURE 34. RSI AND PG TIMING DIAGRAM

UVLO

When the input voltage is below the undervoltage lock-out (UVLO) threshold, the regulator is disabled.

Soft Start-Up

The soft-start-up reduces the in-rush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed so that the output voltage rises in a controlled fashion. When VFB is less than 0.2V at the beginning of the soft-start, the switching frequency is reduced to 1/3 of the nominal value so that the output can start up smoothly at light load condition. During soft-start, the IC operates in the SKIP mode to support pre-biased output condition.

Enable

The enable (EN) input allows the user to control the turning on or off the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600µs delay for waking up the bandgap reference and then the soft-start-up begins.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-MOSFET is typically 120mΩ and the ON-resistance for the N-MOSFET is typically 110mΩ.

100% Duty Cycle

The ISL8012 features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8012 can no longer maintain the regulation at the output, the regulator completely turns on the P-MOSFET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-MOSFET.

Thermal Shut-Down

The ISL8012 has built-in thermal protection. When the internal temperature reaches +140°C, the regulator is completely shut down. As the temperature drops to +115°C, the ISL8012 resumes operation by stepping through the soft-start.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, ISL8012 typically uses a 2.2µH output inductor. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value

can be increased. It is recommended to set the ripple inductor current approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 1:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_S} \quad \text{(EQ. 1)}$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8012 protects the typical peak current 6A. The saturation current needs be over 7A for maximum output current application.

ISL8012 uses internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 1.

TABLE 1. OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT} (V)	C_{OUT}	L
0.8	22µF	1.5µH~3.3µH
1.2	22µF	1.5µH~3.3µH
1.5	22µF	1.8µH~3.3µH
1.8	22µF	2.2µH~3.3µH
2.5	22µF	2.2µH~4.7µH
3.3	22µF	2.2µH~4.7µH
3.6	22µF	2.2µH~4.7µH

In Table 1, the minimum output capacitor value is given for the different output voltage to make sure that the whole converter system is stable.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 1.

The output voltage programming resistor, R_3, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 2.

$$R_3 = \frac{R_2 \times 0.8V}{V_{OUT} - 0.8V} \quad \text{(EQ. 2)}$$

If the output voltage desired is 0.8V, then R_3 is left unpopulated and R_2 is shorted. For better performance, add 220pF in parallel with R_2 (124kΩ).

Input Capacitor Selection

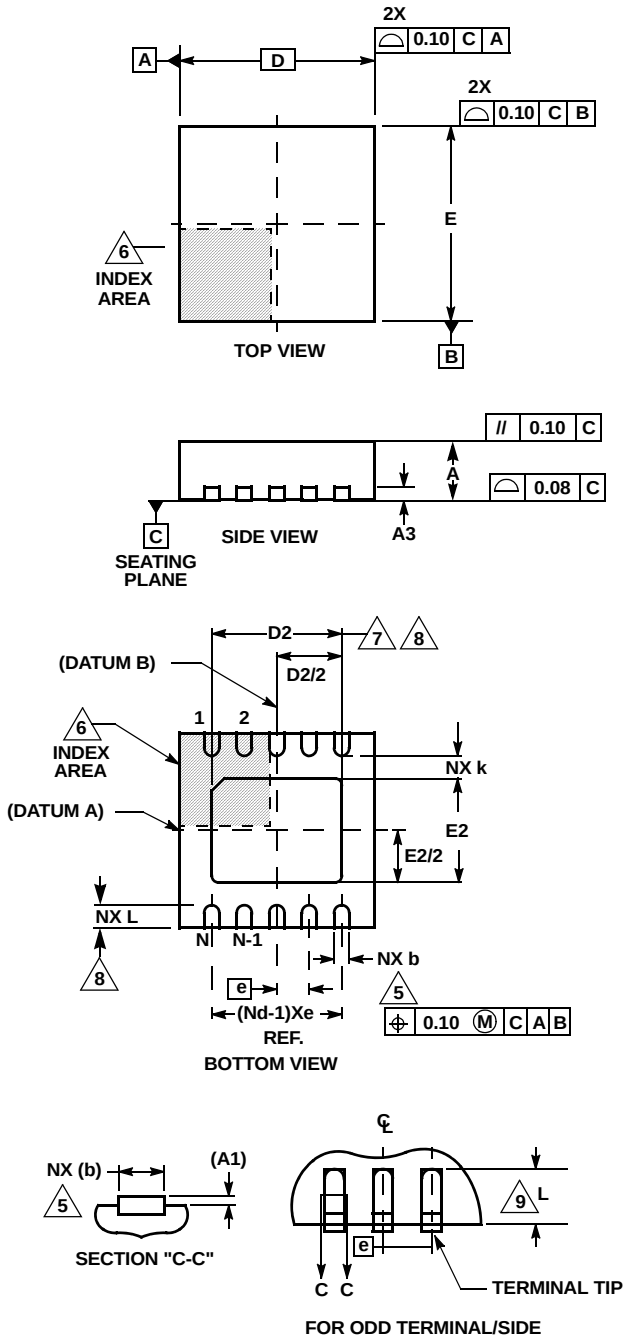
The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current from flowing back to the battery rail. One 22µF X5R or X7R ceramic capacitor is a good starting point for the input capacitor selection.

Layout Recommendation

The layout is a very important converter design step to make sure the designed converter works well. For ISL8012 buck converter, the power loop is composed of the output inductor L, the output capacitor C_{OUT}, LX pin and SGND pin. It is necessary to make the power loop as small as possible.

The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal epad is preferable. In addition, a solid ground plane on the second layer is helpful for EMI performance. Then connect the epad to the ground plane with at lease 5 vias for best thermal performance.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D		3.00 BSC		-
D2	2.33	2.38	2.43	7, 8
E		3.00 BSC		-
E2	1.59	1.64	1.69	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N		10		2
Nd		5		3

Rev. 1 4/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.