

# 6.0-18.0 GHz GaAs MMIC Power Amplifier

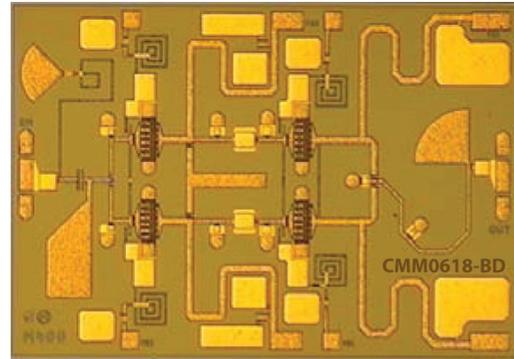
## Features

- ✕ Wide Band Power Amplifier
- ✕ Positive Gain Slope
- ✕ 10.5 dB Small Signal Gain
- ✕ +29.0 dBm P1dB Compression Point
- ✕ +36.0 dBm Third Order Intercept
- ✕ 100% Visual Inspection to MIL-STD-883 Method 2010

## General Description

Mimix Broadband's two stage 6.0-18.0 GHz GaAs MMIC power amplifier has a small signal gain of 10.5 dB with a +29.0 dBm P1dB output compression point and is ideal for use in a balanced configuration. This MMIC uses Mimix Broadband's 0.3  $\mu$ m GaAs PHEMT device model technology, and is based upon electron beam lithography to ensure high repeatability and uniformity. The chip has surface passivation to protect and provide a rugged part with backside via holes and gold metallization to allow either a conductive epoxy or eutectic solder die attach process. This device is well suited for Test Instrumentation, Military, Space, Microwave Point-to-Point Radio, SATCOM and VSAT applications.

## Chip Device Layout



## Absolute Maximum Ratings

Supply Voltage (Vd)	+8.0 VDC
Supply Current (Id1,2)	500, 500 mA
Gate Bias Voltage (Vg)	+0.0 VDC
Input Power (Pin)	+25.0 dBm
Storage Temperature (Tstg)	-65 to +165 °C
Operating Temperature (Ta)	-55 to MTTF Graph <sup>1</sup>
Channel Temperature (Tch)	MTTF Graph <sup>1</sup>

(1) Channel temperature affects a device's MTTF. It is recommended to keep channel temperature as low as possible for maximum life.

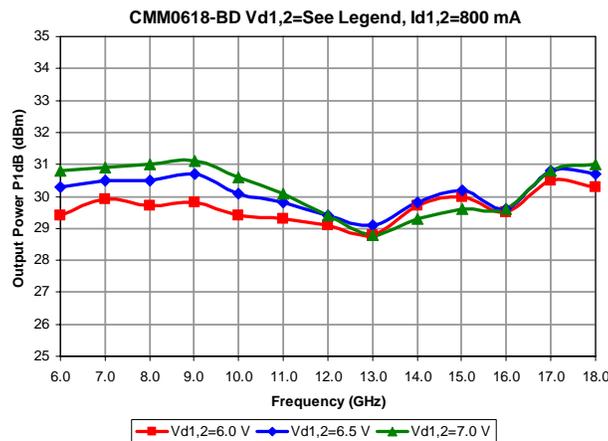
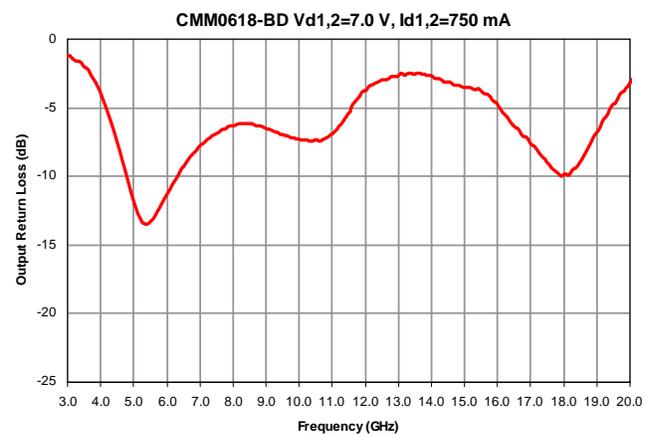
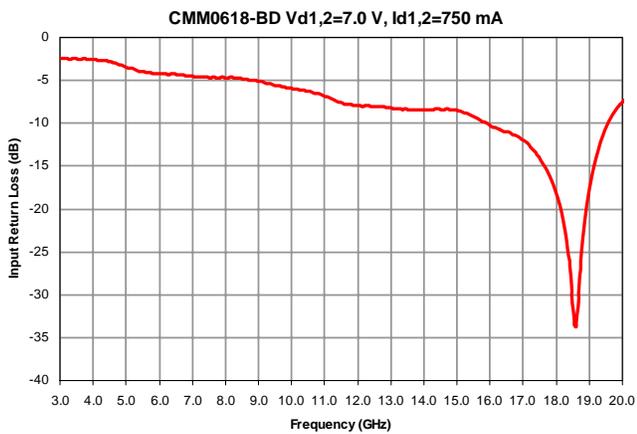
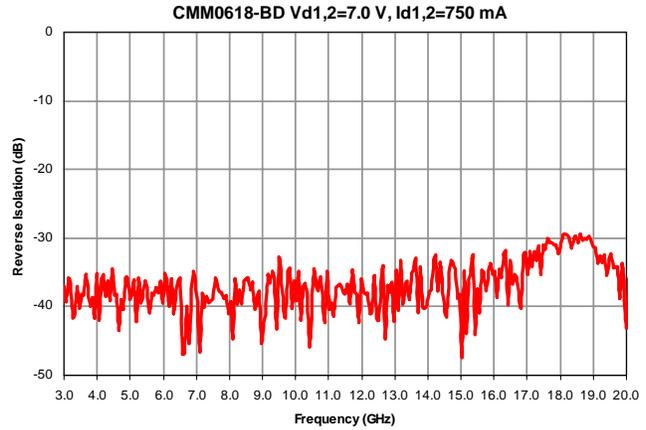
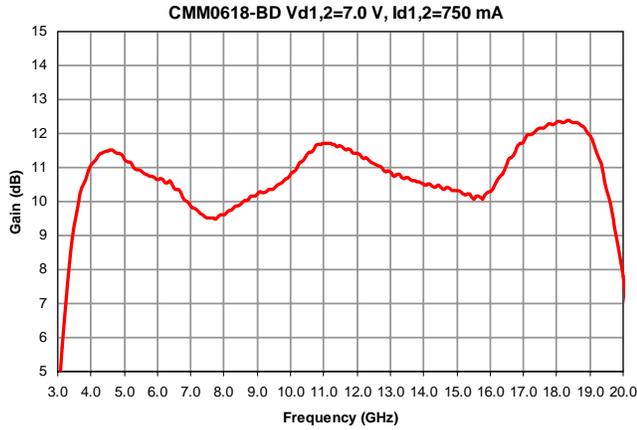
## Electrical Characteristics (Ambient Temperature T = 25 °C)

Parameter	Units	Min.	Typ.	Max.
Frequency Range (f)	GHz	6.0	-	18.0
Input Return Loss (S11)	dB	-	7.0	-
Output Return Loss (S22)	dB	-	5.0	-
Small Signal Gain (S21)	dB	-	10.5	-
Gain Flatness ( $\Delta$ S21)	dB	-	+/-1.5	-
Reverse Isolation (S12)	dB	-	40.0	-
Output Power for 1dB Compression (P1dB)	dBm	-	+29.0	-
Output Third Order Intermods (OIP3)	dBm	-	+36.0	-
Saturated Output Power (Psat)	dBm	-	+30.0	-
Drain Bias Voltage (Vd1,2)	VDC	-	+6.0	+7.5
Gate Bias Voltage (Vg1,2)	VDC	-2.0	-0.8	-0.1
Supply Current (Id1) (Vd=7.0 V, Vg=-0.8 V Typical)	mA	-	375	425
Supply Current (Id2) (Vd=7.0 V, Vg=-0.8 V Typical)	mA	-	375	425

100% on-wafer DC testing and 100% RF wafer qualification. Wafer qualification includes sample testing from each quadrant with an 80% pass rate required.

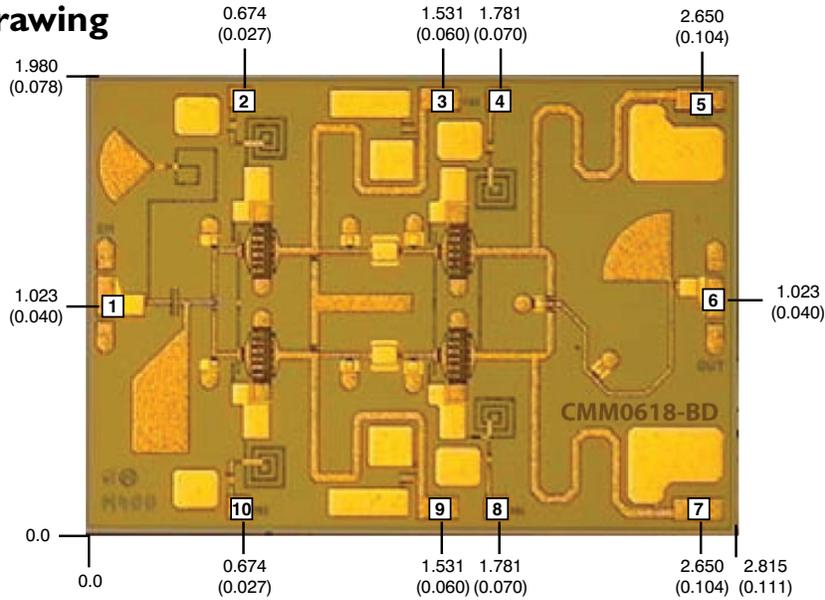
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## Power Amplifier Measurements



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## Mechanical Drawing



(Note: Engineering designator is M400)

Units: millimeters (inches) Bond pad dimensions are shown to center of bond pad.

Thickness: 0.110 +/- 0.010 (0.0043 +/- 0.0004), Backside is ground, Bond Pad/Backside Metallization: Gold  
All Gate DC Bond Pads are 0.100 x 0.100 (0.004 x 0.004). All RF/Drain DC Bond Pads are 0.100 x 0.200 (0.004 x 0.008).

Bond pad centers are approximately 0.109 (0.004) from the edge of the chip.

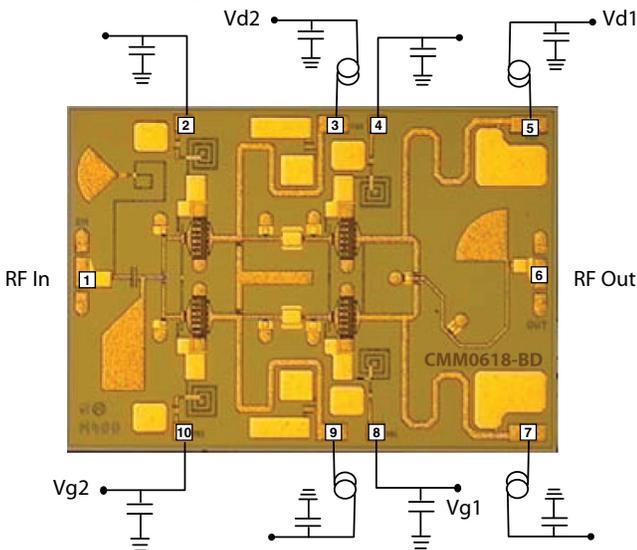
Dicing tolerance: +/- 0.005 (+/- 0.0002). Approximate weight: 3.455 mg.

Bond Pad #1 (RF In)  
Bond Pad #2 (Vg2 Bypass)  
Bond Pad #3 (Vd2)

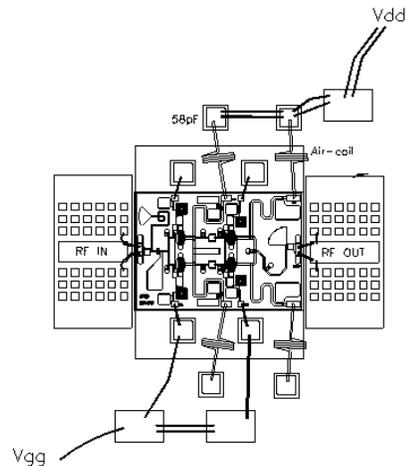
Bond Pad #4 (Vg1 Bypass)  
Bond Pad #5 (Vd1)  
Bond Pad #6 (RF Out)

Bond Pad #7 (Vd1 Bypass)  
Bond Pad #8 (Vg1)  
Bond Pad #9 (Vd2 Bypass)  
Bond Pad #10 (Vg2)

## Bias Arrangement



Bypass Capacitors - See App Note [2]



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August 2007 - Rev 30-Aug-07

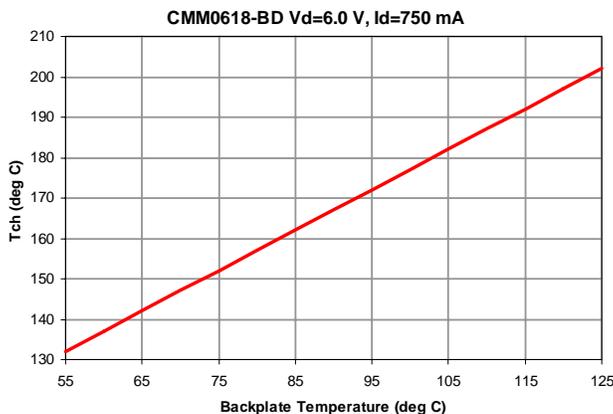
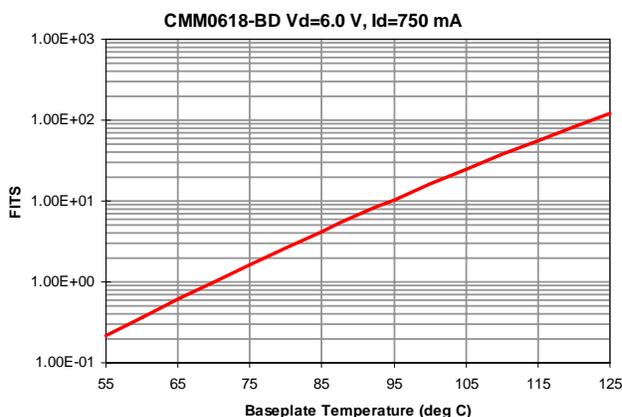
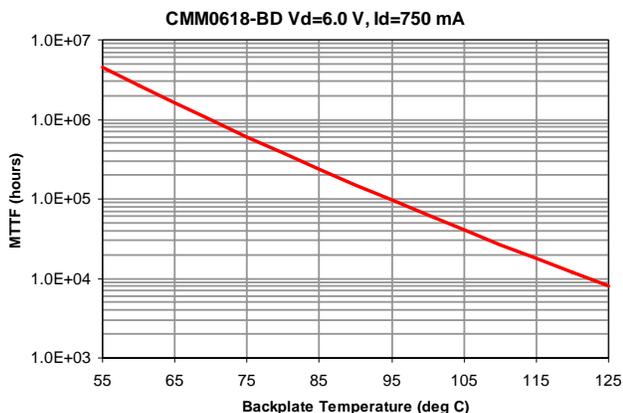
**CMM0618-BD**

**App Note [1] Biasing** - Note bias can be applied from either side of the device. It is recommended to separately bias each amplifier stage Vd1 through Vd2 at Vd(1,2)=6.0V with Id1=375 mA, and Id2=375 mA. Separate biasing is recommended if the amplifier is to be used at high levels of saturation, where gate rectification will alter the effective gate control voltage. For non-critical applications it is possible to parallel all stages and adjust the common gate voltage for a total drain current Id(total)=750 mA. It is also recommended to use active biasing to keep the currents constant as the RF power and temperature vary; this gives the most reproducible results. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -0.8V. Typically the gate is protected with Silicon diodes to limit the applied voltage. Also, make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

**App Note [2] Bias Arrangement** - Each DC pad (Vd1,2 and Vg1,2) needs to have DC bypass capacitance (~100-200 pF) as close to the device as possible. The drain (Vd1,2) bypass paths must also include a 2-3 turn gold air coil as shown. Additional DC bypass capacitance (~0.01 uF) is also recommended.

## MTTF Graphs

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.



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## Handling and Assembly Information

**CAUTION!** - Mimix Broadband MMIC Products contain gallium arsenide (GaAs) which can be hazardous to the human body and the environment. For safety, observe the following procedures:

- *Do not ingest.*
- *Do not alter the form of this product into a gas, powder, or liquid through burning, crushing, or chemical processing as these by-products are dangerous to the human body if inhaled, ingested, or swallowed.*
- *Observe government laws and company regulations when discarding this product. This product must be discarded in accordance with methods specified by applicable hazardous waste procedures.*

**Life Support Policy** - Mimix Broadband's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President and General Counsel of Mimix Broadband. As used herein: (1) Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user. (2) A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ESD** - Gallium Arsenide (GaAs) devices are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic containers, which should be opened in cleanroom conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickups or, with care, sharp tweezers.

**Die Attachment** - GaAs Products from Mimix Broadband are 0.100 mm (0.004") thick and have vias through to the backside to enable grounding to the circuit. Microstrip substrates should be brought as close to the die as possible. The mounting surface should be clean and flat. If using conductive epoxy, recommended epoxies are Tanaka TS3332LD, Die Mat DM6030HK or DM6030HK-Pt cured in a nitrogen atmosphere per manufacturer's cure schedule. Apply epoxy sparingly to avoid getting any on to the top surface of the die. An epoxy fillet should be visible around the total die periphery. For additional information please see the Mimix "Epoxy Specifications for Bare Die" application note. If eutectic mounting is preferred, then a fluxless gold-tin (AuSn) preform, approximately 0.001 thick, placed between the die and the attachment surface should be used. A die bonder that utilizes a heated collet and provides scrubbing action to ensure total wetting to prevent void formation in a nitrogen atmosphere is recommended. The gold-tin eutectic (80% Au 20% Sn) has a melting point of approximately 280 °C (Note: Gold Germanium should be avoided). The work station temperature should be 310 °C +/- 10 °C. Exposure to these extreme temperatures should be kept to minimum. The collet should be heated, and the die pre-heated to avoid excessive thermal shock. Avoidance of air bridges and force impact are critical during placement.

**Wire Bonding** - Windows in the surface passivation above the bond pads are provided to allow wire bonding to the die's gold bond pads. The recommended wire bonding procedure uses 0.076 mm x 0.013 mm (0.003" x 0.0005") 99.99% pure gold ribbon with 0.5-2% elongation to minimize RF port bond inductance. Gold 0.025 mm (0.001") diameter wedge or ball bonds are acceptable for DC Bias connections. Aluminum wire should be avoided. Thermo-compression bonding is recommended though thermosonic bonding may be used providing the ultrasonic content of the bond is minimized. Bond force, time and ultrasonics are all critical parameters. Bonds should be made from the bond pads on the die to the package or substrate. All bonds should be as short as possible.

Part Number for Ordering	Description
CMM0618-BD-000V	RoHS compliant die packed in vacuum release gel packs
PB-CMM0618-BD-0000	CMM0618-BD evaluation module