CY2037

High-Accuracy EPROM Programmable PLL Die for Crystal Oscillators

Features

- EPROM-programmable die for in-package programming of crystal oscillators
- High resolution PLL with 12-bit multiplier and 10-bit divider
- EPROM-programmable capacitor tuning array with shadow register
- Twice programmable die (CY2037A, CY2037B[1], and CY2037-2)
- Simple 2-wire programming interface
- On-chip oscillator runs from 10 - 30 MHz fundamental tuned crystal
- EPROM-selectable TTL or CMOS duty cycle levels
- Operating frequency:
  - 1 - 133 MHz at 5V
  - 1 - 100 MHz at 3.3V
  - 1 - 66.6 MHz at 2.7V
- Sixteen selectable post divide options, using PLL or reference oscillator output
- Programmable power down (PD#) or OE pin (CY2037A, CY2037B, and CY2037-2)
- Frequency select (CY2037-3)
- Programmable asynchronous or synchronous OE and power down (PD#) modes (CY2037A, CY2037B, and CY2037-2)
- Low jitter outputs typically:
  - < ± 100 ps (pk-pk) at 5V and f>33 MHz
  - < ± 125 ps (pk-pk) at 3.3V and f>33 MHz
- 3.3V or 5V operation
- Small die
- Controlled rise and fall times and output slew rate

Benefits

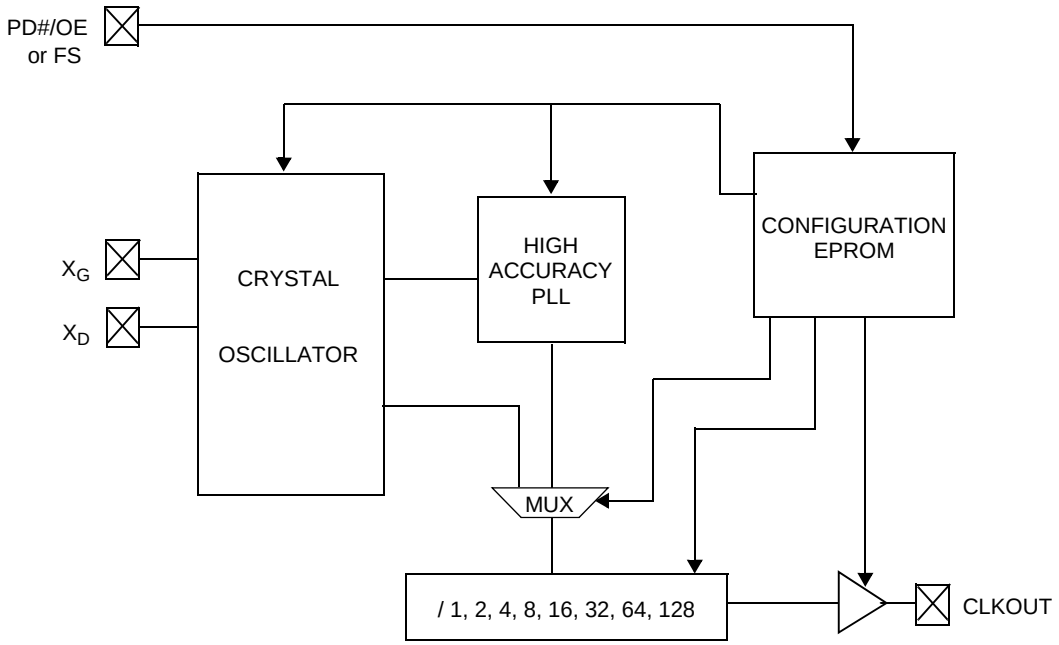
- Enables quick turnaround of custom oscillators
- Lowers inventory costs through stocking of blank parts
- Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM
- Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
- Enables reprogramming of programmed part to correct errors, and control excess inventory
- Enables programming of output frequency after packaging
- Lowers cost of oscillator because PLL may be programmed to a high frequency using a low frequency, low cost crystal
- Duty cycle centered at 1.4V or $V_{DD}/2$
- Provides flexibility to service most TTL or CMOS applications
- Provides flexibility in output configurations and testing
- Enables low power operations or output enable functions
- Enables two frequency options for meeting different industry standards, that is, PAL/NTSC
- Provides flexibility for system applications through selectable instantaneous or synchronous change in outputs
- Suitable for most PC, consumer, and networking applications
- Lowers inventory costs because the same die services both applications
- Enables encapsulation in small size, surface mount packages
- Has lower EMI than oscillators

Table 1. Device Functionality: Output Frequencies

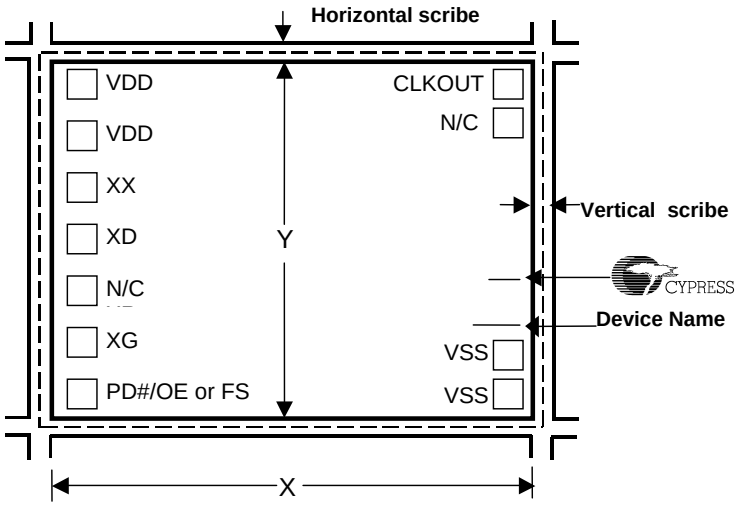
Parameter	Description	Condition	Min	Max	Unit
Fo	Output frequency	V_{DD} = 4.5V–5.5V	1	133	MHz
		V_{DD} = 3.0V–3.6V	1	100	MHz
		V_{DD} = 2.7V–3.0V	1	66	MHz

Note
1. CY2037A and CY2037B are identical. However, CY2037B is recommended for all new designs.

Logic Block Diagram



Die Pad Description



Note
Active die size: X = 55.9 mils / 1420.1 μm

Scribe: X (horizontal) = 2.6 mils / 65.6 μm
Y (vertical) = 3.0 mils / 76.9 μm
Bond pad opening: 85 μm x 85 μm
Pad pitch: 125 μm x 125 μm
(pad center to pad center)

Die Pad Summary

Name	Die Pad	X Coordinate (μm)	Y Coordinate (μm)	Description
V_{DD}	1, 2	124.7	855.6, 731	Voltage supply
V_{SS}	8, 9	1291.35	99.6, 225.2	Ground
X_D	4	124.7	481.8	Crystal connection
X_X	3	124.7	606.4	No connect [2]
X_G	6	124.7	232.6	Crystal connection
PD#/OE or FS	7	124.7	108	CY2037A, CY2037B, and CY2037-2: EPROM-programmable power down or output enable pad CY2037-3: Frequency select. Serves as V_{PP} in programming mode for all devices
CLKOUT	11	1282.45	901.8	Clock output. Also serves as three-state input during programming.
N/C	5, 10	124.7,1282.45	357.2, 769.4	No connect (so do not bond to these pads)

Note
2. For customers not bonding the X_D or X_G pad to external pins, an alternative bonding option would be shorting the Xx pad to the X_D pad.

Functional Description

CY2037 is an EPROM-programmable, high accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low cost 10 - 30 MHz crystal and can be packaged into a 4-pin through-hole or surface mount packages. The oscillator devices may be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

CY2037 contains an on-chip oscillator and a unique oscillator tuning circuit for fine-tuning of the output frequency. The crystal C_{load} may be selectively adjusted by programming a set of seven EPROM bits. This feature is used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

CY2037 uses EPROM programming with a simple 2-wire, 4-pin interface that includes V_{SS} and V_{DD}. Clock outputs may be generated up to 133 MHz at 5V or up to 100 MHz at 3.3V. The entire configuration can be reprogrammed once, which allows the programmed inventory to be altered or reused.

CY2037 PLL die is designed for very high resolution. It has a 12-bit feedback counter multiplier and a 10-bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The clock is further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64, and 128. The divider input can be selected as the PLL or crystal oscillator output, providing a total of 16 separate output options. For further flexibility, the ouput is selectable between TTL and CMOS duty cycle levels.

CY2037, CY2037B, and CY2037-2 also contain flexible power management controls. These parts include both power down (PD#) and OE features with integrated pull up resistors. The PD# and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PD# or OE modes are enabled, CLKOUT is pulled low by a weak pull down. The weak pull down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable CY2037 to have low jitter and accurate outputs, making it suitable for most PC, networking, and consumer applications.

On the other hand, CY2037-3 contains a frequency select function in place of the power down and output enable modes. For example, consumer products often require frequency compatibility with different electrical standards around the world. With this frequency select feature, a product that incorporates CY2037-3 could be compatible with both NTSC for North American, and PAL for Europe by simply changing the FS line. The twice programmable feature is also absent in CY2037-3, because the second EPROM row is now being used for the alternate frequency.

EPROM Configuration Block

Table 2 summarizes the features that are configurable by EPROM. Refer “7C8038x/7C8034X Programming Specification” for further details. This specification can be obtained from your Cypress factory representative.

Table 2. EPROM Adjustable Features

Adjustable Features	
Adjust Frequency	Feedback Counter Value (P)
	Reference Counter Value (Q)
	Output Divider Selection
Oscillator Tuning (Load Capacitance Values)	
Duty Cycle Levels (TTL or CMOS)	
Power Management Mode (OE or PD#)	
Power Management Timing (Synchronous or Asynchronous)	

PLL Output Frequency

CY2037 contains a high resolution PLL with 12-bit multiplier and 10-bit divider. The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P + 5)}{(Q + 2)} \bullet F_{REF}$$

In this formula, P is the feedback counter value and Q is the reference counter value. P and Q are EPROM programmable values.

Power Management Features (except CY2037-3)

CY2037 contains EPROM-programmable PD# and OE functions. If power down is selected, all active circuitry on the chip is shut down when the control pin goes LOW. The oscillator and PLL circuits must relock when the part leaves the power down mode. If output enable mode is selected, the output is tri-stated and weakly pulled low when the control pin goes low. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the control input is deasserted.

In addition, the PD# and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power down or output disable occurs immediately (allowing for logic delays), regardless of the position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before the power down or output enable signal is initiated, thus preventing output glitches. In asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Crystal Oscillator Tuning Circuit

CY2037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM-programmable and may be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in Table 3. Refer to "7C8038x/7C8034x Programming Specification" for further details.

Figure 1. Crystal Oscillator Tuning Circuit

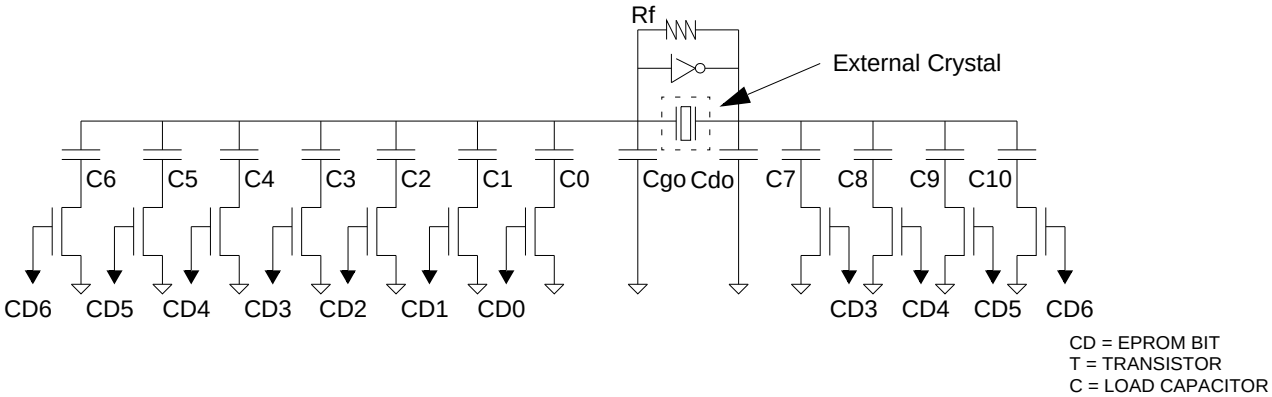


Table 3. Crystal Oscillator Parameter

Parameter	Description	Min	Typ.	Max	Unit
R_f	Feedback resistor, V_{DD} = 4.5–5.5V Feedback resistor, V_{DD} = 2.7–3.6V	0.5 1.0	2 4	3.5 9.0	MΩ MΩ
Capacitors have ± 20% tolerance					
C_g	Gate capacitor		13		pF
C_d	Drain capacitor		9		pF
C_0	Series cap		0.27		pF
C_1	Series cap		0.52		pF
C_2	Series cap		1.00		pF
C_3	Series cap		0.7		pF
C_4	Series cap		1.4		pF
C_5	Series cap		2.6		pF
C_6	Series cap		5.0		pF
C_7	Series cap		0.45		pF
C_8	Series cap		0.85		pF
C_9	Series cap		1.7		pF
C_{10}	Series cap		3.3		pF

CY2037A/CY2037B Versus CY2037-2

CY2037A and CY2037B contain a shadow register in addition to the EPROM register. The shadow register is an exact copy of the EPROM register and is the default register when the Valid bit is not set. It is useful when the prototype or production environment calls for measuring and adjusting the CLKOUT frequency several times. Multiple adjustments can be performed with the shadow register. After the required frequency is achieved the EPROM register is permanently programmed.

Some production flows do not require the use of the shadow register. If this is the case, then CY2037-2 is the chosen device and CY2037-2 has a disabled shadow register. CY2037-3 contains the shadow register.

Frequency Select Feature of CY2037-3

CY2037-3 contains a frequency select function in place of the powerdown and the output enable functions. With the frequency select feature, customers can switch two different frequencies that are configured in the two EPROM rows. Table 4 lists the definition of the frequency select pin (FS).

Table 4. Frequency Select Pin Decoding for CY2037-3

FS Pin	Output Frequency
0	From EPROM row 0 configuration
1	From EPROM row 1 configuration

Inkless Die Pick Map (DPM) Format

Cypress ships inkless wafers to customers with an accompanying die pick map, which is used to determine the good die for assembly and programming. Customers can also access individual DPM files at their convenience through ftp.cypress.com with a valid user account login and password. Contact your local Cypress Field Application Engineer (FAE) or sales representative for a customer FTP account. The DPM files are named with the fab lot number and wafer number scribed on the wafer. The DPM files are transferred to the customer's FTP account when the factory ships out the wafers against their purchase order (PO).

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.[3]

Supply voltage ..... –0.5 to +7.0V

Input voltage ..... –0.5V to V_{DD}+0.5

Storage temperature (non-condensing) ..... 55°C to +150°C

Junction temperature ..... –40°C to +100°C

Static discharge voltage ..... 2000V (per MIL-STD-883, Method 3015)

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage (3.3V) Supply voltage (5.0V)	2.7 4.5	3.6 5.5	V V
T_{AJ} [4]	Operating temperature, Junction	–10	+100	°C
C_{TTL}	Max. capacitive load on outputs for TTL levels V_{DD} = 4.5–5.5V, output frequency = 1 - 40 MHz V_{DD} = 4.5–5.5V, output frequency = 40 - 133 MHz		 50 25	 pF pF
C_{CMOS}	Max. capacitive load on outputs for CMOS levels V_{DD} = 4.5–5.5V, output frequency = 1 - 66.6 MHz V_{DD} = 4.5–5.5V, output frequency = 66.6 - 133 MHz V_{DD} = 3.0–3.6V, output frequency = 1 - 40 MHz V_{DD} = 3.0–3.6V, output frequency = 40 - 100 MHz V_{DD} = 2.7–3.0V, output frequency = 1 - 66 MHz		 50 25 30 15 15	 pF pF pF pF pF
X_{REF}	Reference frequency, input crystal. Fundamental tuned crystals only	10	30	MHz
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics

Over the Operating Range[5]

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
V_{IL}	Low level input voltage	V_{DD} = 4.5V - 5.5V V_{DD} = 2.7V - 3.6V			0.8 0.2V_{DD}	V V
V_{IH}	High level input voltage	V_{DD} = 4.5V - 5.5V V_{DD} = 2.7V - 3.6V	2.0 0.7V_{DD}			V V
V_{OL}	Low level output voltage	V_{DD} = 4.5V - 5.5V, I_{OL}= 16 mA V_{DD} = 2.7V - 3.6V, I_{OL}= 8 mA			0.4 0.4	V V
V_{OHCMOS}	High level output voltage, CMOS levels	V_{DD} = 4.5V - 5.5V, I_{OH} = –16 mA V_{DD} = 2.7V - 3.6V, I_{OH} = –8 mA	V_{DD} – 0.4 V_{DD} – 0.4			V V
V_{OHTTL}	High level output voltage, TTL levels	V_{DD} = 4.5V - 5.5V, I_{OH} = –8 mA	2.4			V
I_{IL}	Input low current	V_{IN} = 0V			10	µA
I_{IH}	Input high current	V_{IN} = V_{DD}			5	µA
I_{DD}	Power supply current, Unloaded	V_{DD} = 4.5V - 5.5V, output frequency <= 133 MHz V_{DD} = 2.7V - 3.6V, output frequency <= 100 MHz			45 25	mA mA
I_{DDS}[6]	Standby current	V_{DD} = 2.7V - 3.6V		10	50	µA
R_{UP}	Input pull up resistor	V_{DD} = 4.5V - 5.5V, V_{IN} = 0V V_{DD} = 4.5V - 5.5V, V_{IN} = 0.7V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ
I_{OE_CLKOUT}	CLKOUT pull down current	V_{DD} = 5.0		20		µA

Notes

3. Stresses greater than listed can impair the life of the device.
4. This product is sold in die form so operating conditions are specified for the die, or junction temperature.
5. This part was characterized in a 20-pin SOIC package with external crystal, Electrical Characteristics can change with other package types.
6. If external reference is used, it is required to stop the reference (set reference to LOW) during power down.

Output Clock Switching Characteristics

Over the Operating Range[7]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
t_{1w}	Output duty cycle at 1.4V, V_{DD} = 4.5–5.5V $t_{1w} = t_{1A} \div t_{1B}$	1 - 40 MHz, C_L <=50 pF 40 - 66 MHz, C_L <=15 pF 66 - 125 MHz, C_L <=25 pF 125 - 133 MHz, C_L <=15 pF	45 45 40 40		55 55 60 60	% % % %
t_{1x}	Output duty cycle at $V_{DD}/2$, V_{DD} = 4.5–5.5V $t_{1x} = t_{1A} \div t_{1B}$	1 - 66.6 MHz, C_L <=25 pF 66.6 - 125 MHz, C_L <=25 pF 125 - 133 MHz, C_L <=15 pF	45 40 40		55 60 60	% % %
t_{1y}	Output duty cycle at $V_{DD}/2$, V_{DD} = 3.0–3.6 $t_{1y} = t_{1A} \div t_{1B}$	1 - 40 MHz, C_L <=30 pF 40 - 100 MHz, C_L <=15 pF	45 40		55 60	% %
t_{1z}	Output duty cycle at $V_{DD}/2$, V_{DD} = 2.7–3.0 $t_{1y} = t_{1A} \div t_{1B}$	1 - 40 MHz, C_L <=15 pF 40 - 66.6 MHz, C_L <=10 pF	40 40		60 60	% %
t_2	Output clock rise time	Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 50 pF Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 25 pF Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 15 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 4.5V - 5.5V, C_L = 50 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 3.0V - 3.6V, C_L = 30 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 2.7V - 3.6V, C_L = 15 pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_3	Output clock fall time	Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 50 pF Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 25 pF Between 0.8V - 2.0V, V_{DD} = 4.5V - 5.5V, C_L = 15 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 4.5V - 5.5V, C_L = 50 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 3.0V - 3.6V, C_L = 30 pF Between 0.2V_{DD} - 0.8V_{DD}, V_{DD} = 2.7V - 3.6V, C_L = 15 pF			1.8 1.2 0.9 3.4 4.0 2.4	ns ns ns ns ns ns
t_4	Startup time out of power down	PD# pin LOW to HIGH[8]		1	2	ms
t_{5a}	Power down delay time (synchronous setting)	PD# pin LOW to output LOW (T = period of output clk)		T/2	T+10	ns
t_{5b}	Power down delay time (asynchronous setting)	PD# pin LOW to output LOW		10	15	ns
t_6	Power up time	From power on[8]		1	2	ms
t_{7a}	Output disable time (synchronous setting)	OE pin LOW to output Hi-Z (T = period of output clk)		T/2	T+10	ns
t_{7b}	Output disable time (asynchronous setting)	OE pin LOW to output Hi-Z		10	15	ns
t_8	Output enable time (always synchronous enable)	OE pin LOW to HIGH (T = period of output clk)		T	1.5T+2 5	ns
t_9	Peak-to-peak period jitter	V_{DD} = 4.5V - 5.5V, Fo > 33 MHz, VCO > 100 MHz V_{DD} = 2.7V - 3.6V, Fo > 33 MHz, VCO > 100 MHz V_{DD} = 2.7V - 5.5V, Fo < 33 MHz		±100 ±125 ±250	±125 ±200 1% of F_O	ps ps ps

Notes

7. Not all parameters measured in production testing.
8. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70 ohms.

Switching Waveforms

Figure 2. Duty Cycle Timing (t_{1w}, t_{1x}, t_{1y}, t_{1z})

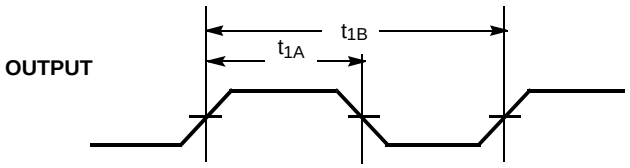


Figure 3. Output Rise/Fall Time

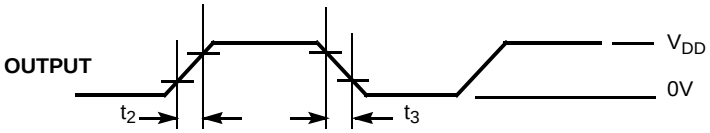


Figure 4. Power Down Timing (synchronous and asynchronous modes)

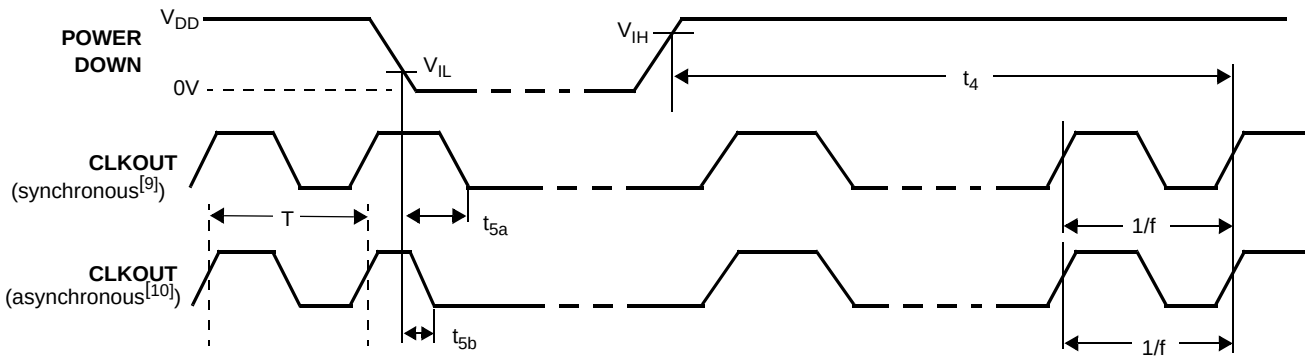
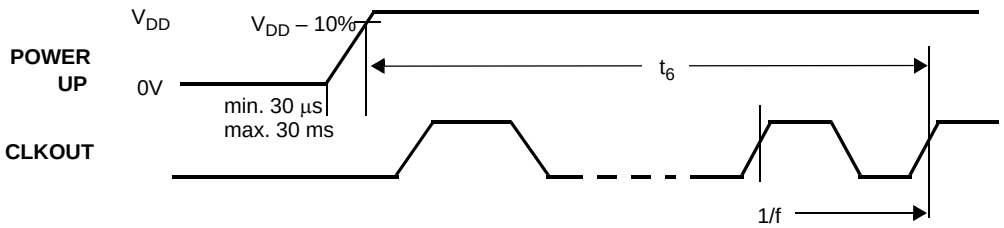


Figure 5. Power Up Timing



Notes
9. In synchronous mode the power down or output tri-state is not initiated until the next falling edge of the output clock.
10. In asynchronous mode the power down or output tri-state occurs within 25 ns regardless of position in the output clock cycle.

Ordering Information[11]

Ordering Code	Status	Type	Wafer Thickness	Operating Range
CY2037AWAF	Obsolete	Inked Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037-2WAF	Obsolete	Inked Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037-3WAF	Obsolete	Inked Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037BWAF	Obsolete	Inked Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037B-11WAF	Obsolete	Inked Wafer	11 ± 0.5 mils	–10°C to +100°C
CY2037BWAF-IL	Active	Inkless Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037B-11WAF-IL	Active	Inkless Wafer	11 ± 0.5 mils	–10°C to +100°C
CY2037-2WAF-IL	Obsolete, CY2037BWAF-IL is recommended for new designs	Inkless Wafer	14 ± 0.5 mils	–10°C to +100°C
CY2037-3WAF-IL	Obsolete	Inkless Wafer	14 ± 0.5 mils	–10°C to +100°C

Notes

11. The only difference between the CY2037A/CY2037B, and the CY2037-2 is that the CY2037-2 has the shadow register disabled. CY2037-3 replaces the power down options with a frequency select and contains the shadow register.

Document History Page

Document Title: CY2037 High-Accuracy EPROM Programmable PLL Die for Crystal Oscillators Document Number: 38-07354				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	112248	03/01/02	DSG	Change from Spec number: 38-00679 to 38-07354
*A	121857	12/14/02	RBI	Power up requirements added to Operating Conditions Information
*B	291092	See ECN	RGL	Updated Min. Operating Temperature, Junction
*C	522769	See ECN	RGL	Added CY2037B information. Updated absolute maximum Junction temperature specification. Updated Ordering information table. Added Die Pad description and coordinates
*D	804376	See ECN	RGL	Minor Change: To post on web
*E	2192266	See ECN	DPF/PYRS	Added Inkless Die information.