CY7C1011CV33

2-Mbit (128K x 16) Static RAM

Features

- Temperature ranges
  - Commercial: 0°C to 70°C
  - Industrial: –40°C to 85°C
  - Automotive-A: –40°C to 85°C
- Pin and function compatible with CY7C1011BV33
- High speed
  - t_{AA} = 10 ns
- Low active power
  - 360 mW (max)
- Data Retention at 2.0
- Automatic power down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free and non Pb-free 44-pin TSOP II, 44-pin TQFP and 48-Ball VFBGA packages

Functional Description

The CY7C1011CV33 is a high performance CMOS static RAM organized as 131,072 words by 16 bits. This device has an automatic power down feature that significantly reduces power consumption when deselected.

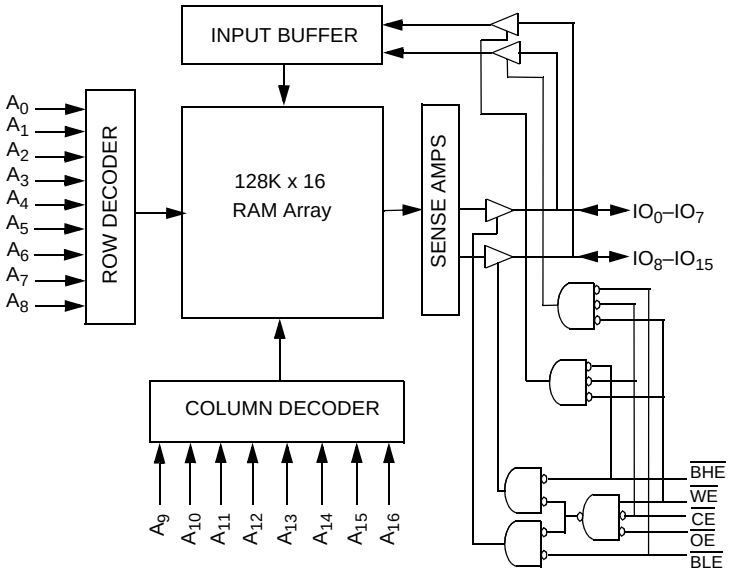
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{16}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. For more information, see the "Truth Table" on page 9 for a complete description of Read and Write modes.

The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.

Logic Block Diagram



Pin Configuration

Figure 1. 44-Pin TSOP II [1]

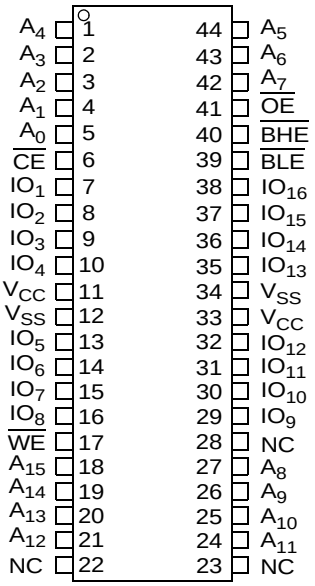


Figure 2. 48-Ball FBGA Pinout [1]

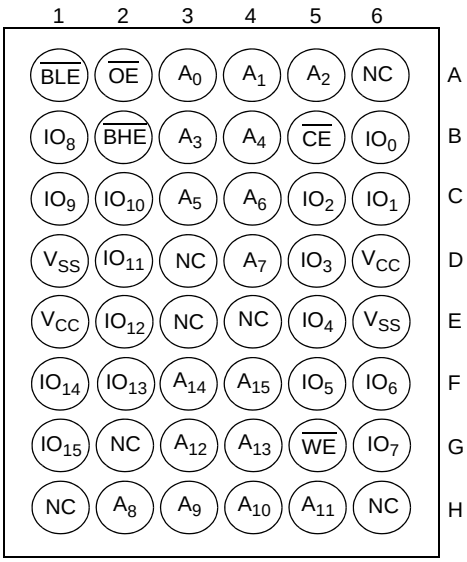
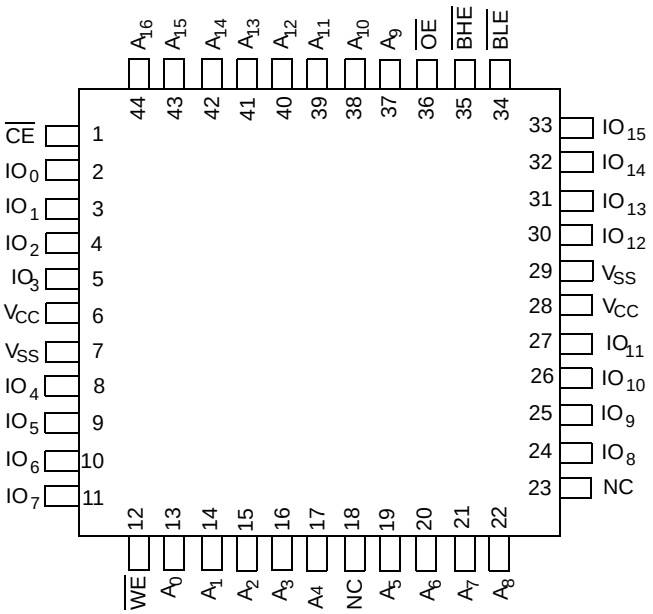


Figure 3. 44-Pin TQFP II



Note
1. NC pins are not connected on the die.

Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Comm'l	90	85	80	mA
	Ind'l	100	95		mA
	Auto-A	100			mA
Maximum CMOS Standby Current	Comm'l/Ind'l	10	10	10	mA
	Auto-A	10			mA

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[2].....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[2].....–0.5V to V_{CC}+0.5V

DC Input Voltage[2] .....–0.5V to V_{CC}+0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	
Automotive-A	–40°C to +85°C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	µA
			Auto-A	–1	+1					
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output disabled	Com'l/Ind'l	–1	+1	–1	+1	–1	+1	µA
			Auto-A	–1	+1					
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		90		85		80	mA
			Ind'l		100		95			
			Auto-A		100					
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		40		40		40	mA
			Auto-A		40					
I_{SB2}	Automatic CE Power Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		10		10		10	mA
			Auto-A		10					

Note
2. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	Output Capacitance		8	pF

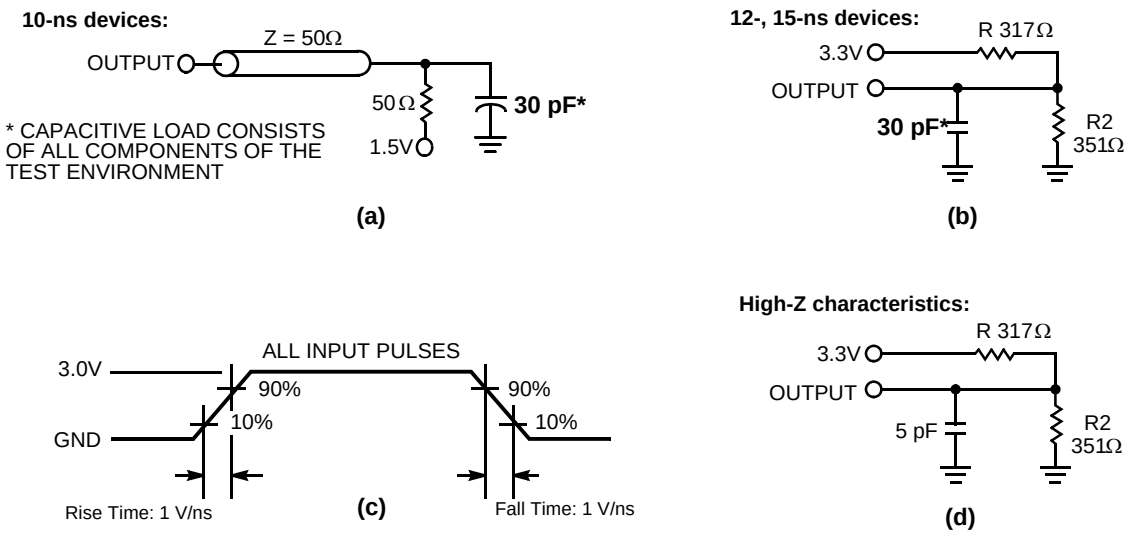
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	TQFP	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	44.56	42.66	46.98	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		10.75	14.64	9.63	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms [3]



Note

3. AC characteristics (except High-Z) for 10-ns parts are tested using the load conditions shown in Figure 4 (a). All other speeds are tested using the Thevenin load shown in Figure 4 (b). High-Z characteristics are tested for all speeds using the test load shown in Figure 4 (d).

Switching Characteristics

Over the Operating Range [4]

Parameter	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{power}[5]	V_{CC}(Typical) to the First Access	1		1		1		µs
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[6]	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		ns
t_{HZBE}	Byte Disable to High Z		5		6		7	ns
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		10		ns
t_{AW}	Address Setup to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Setup to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		10		ns
t_{SD}	Data Setup to Write End	5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[6]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		5		6		7	ns
t_{BW}	Byte Enable to End of Write	7		8		10		ns

Notes

4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V.
5. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
6. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
7. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 5. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$/$\overline{BLE}$ must be LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 5. Read Cycle No. 1 (Address Transition Controlled)[10, 11]

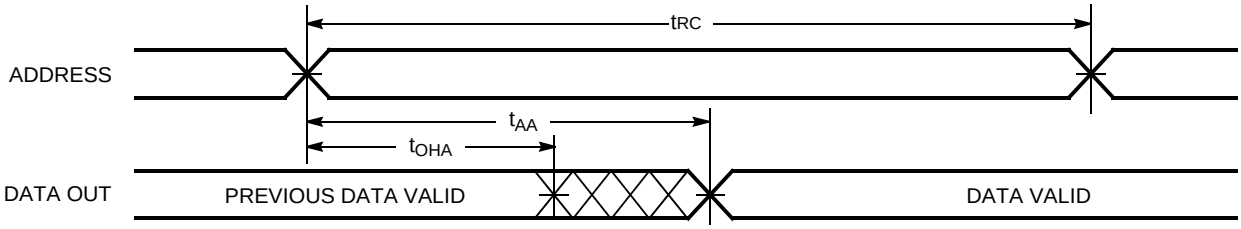
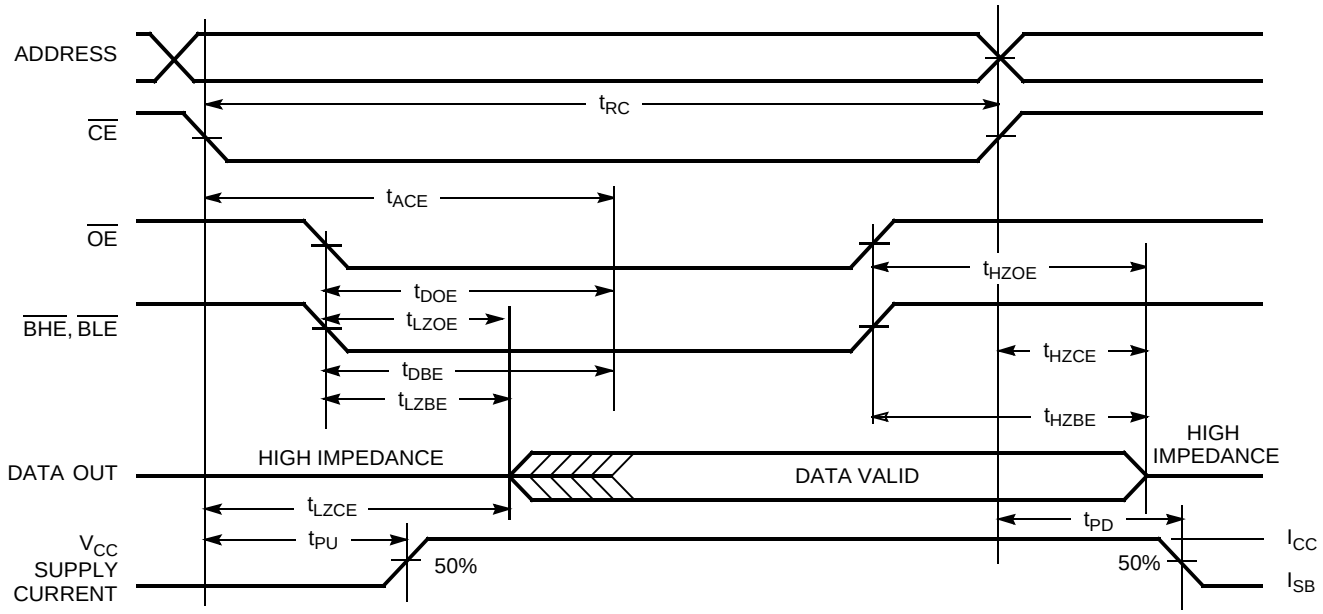


Figure 6. Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 12]



Notes
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ($\overline{CE}$ Controlled)[13, 14]

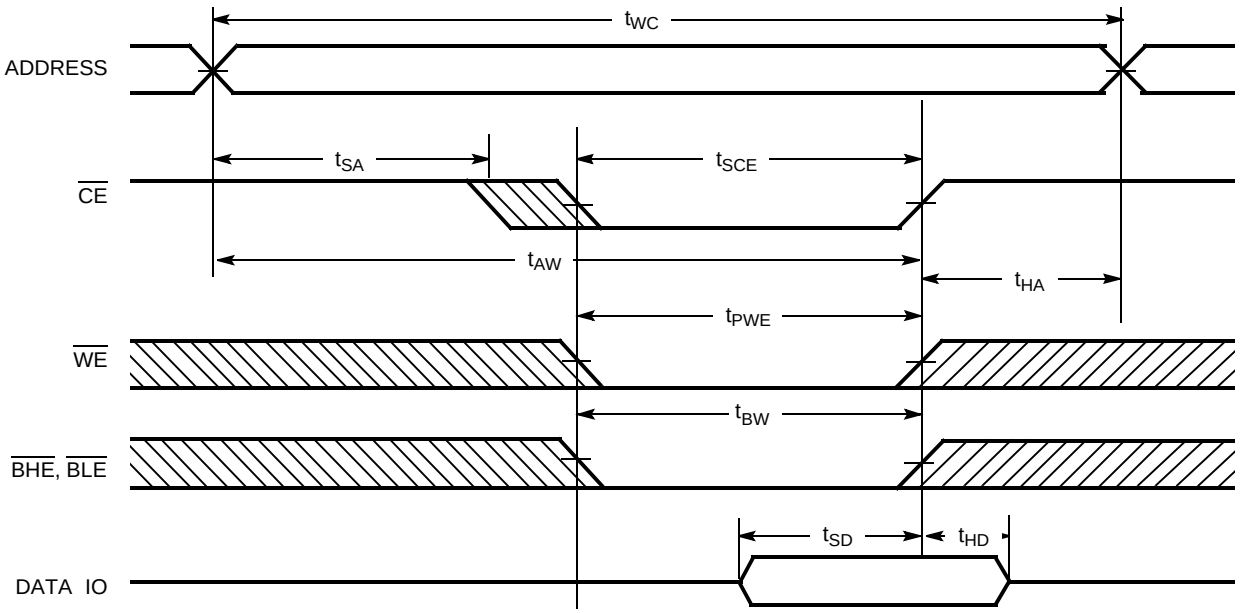
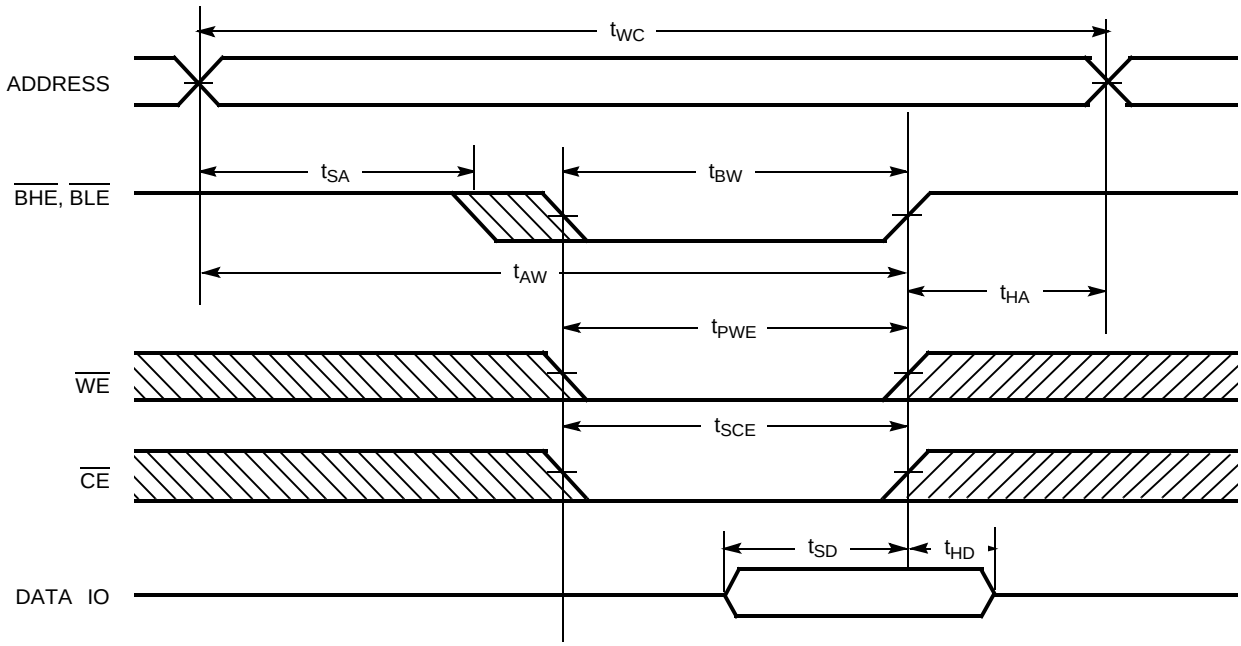


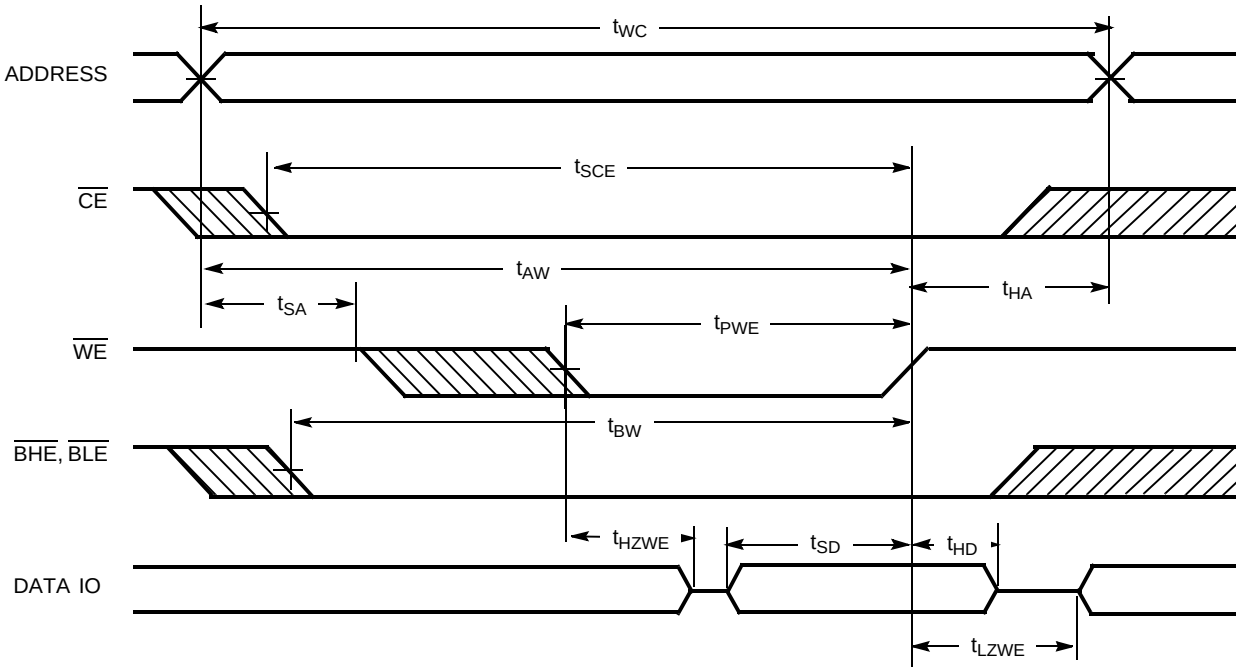
Figure 8. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
13. Data IO is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	IO_0–IO_7	IO_8 – IO_{15}	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

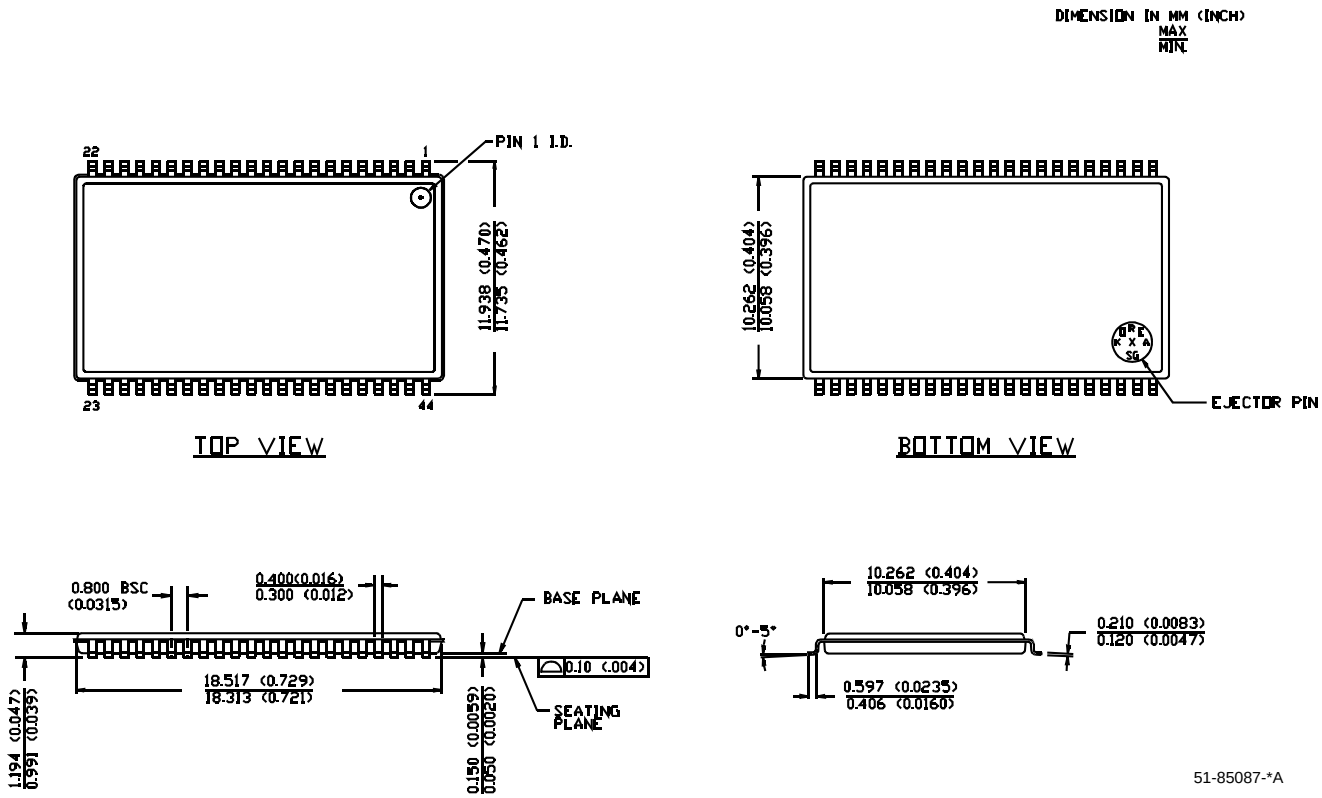
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1011CV33-10ZC	51-85087	44-pin TSOP II	Commercial
	CY7C1011CV33-10ZXC		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-10ZXI	51-85087	44-pin TSOP II (Pb-Free)	Industrial
	CY7C1011CV33-10BVI	51-85150	48-ball (6 x 8 x 1 mm) VFBGA	
	CY7C1011CV33-10ZSXA	51-85087	44-pin TSOP II (Pb-Free)	Automotive-A
12	CY7C1011CV33-12ZC	51-85087	44-pin TSOP II	Commercial
	CY7C1011CV33-12ZXC		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-12ZI	51-85087	44-pin TSOP II	Industrial
	CY7C1011CV33-12ZXI		44-pin TSOP II (Pb-Free)	
	CY7C1011CV33-12AXI	51-85064	44-pin TQFP (Pb-Free)	
	CY7C1011CV33-12BVI	51-85150	48-ball (6 x 8 x 1 mm) VFBGA	
15	CY7C1011CV33-15ZXC	51-85087	44-pin TSOP II (Pb-Free)	Commercial

The 44 pin TSOP II package containing the Automotive grade device is designated as “ZS”, while the same package containing the Commercial/Industrial grade device is “Z”.

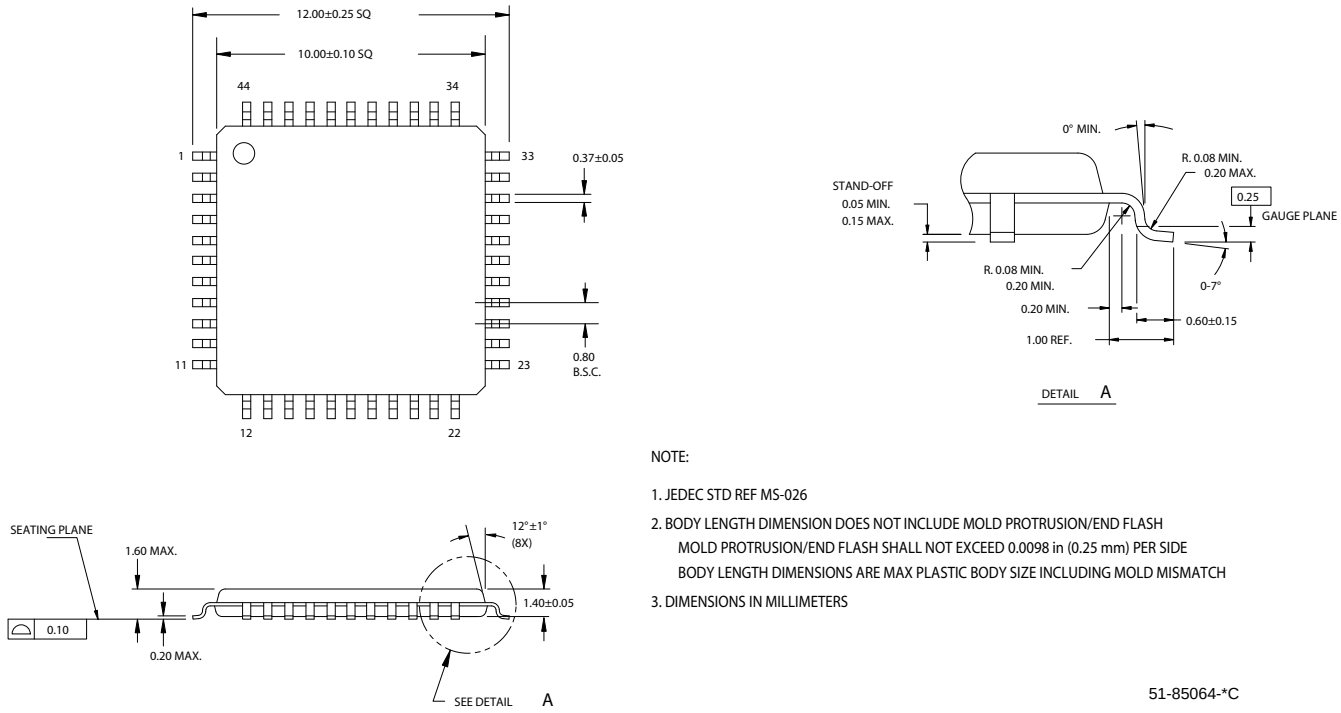
Package Diagrams

Figure 10. 44-Pin Thin Small Outline Package Type II



Package Diagrams (continued)

Figure 11. 44-pin Thin Plastic Quad Flat Pack



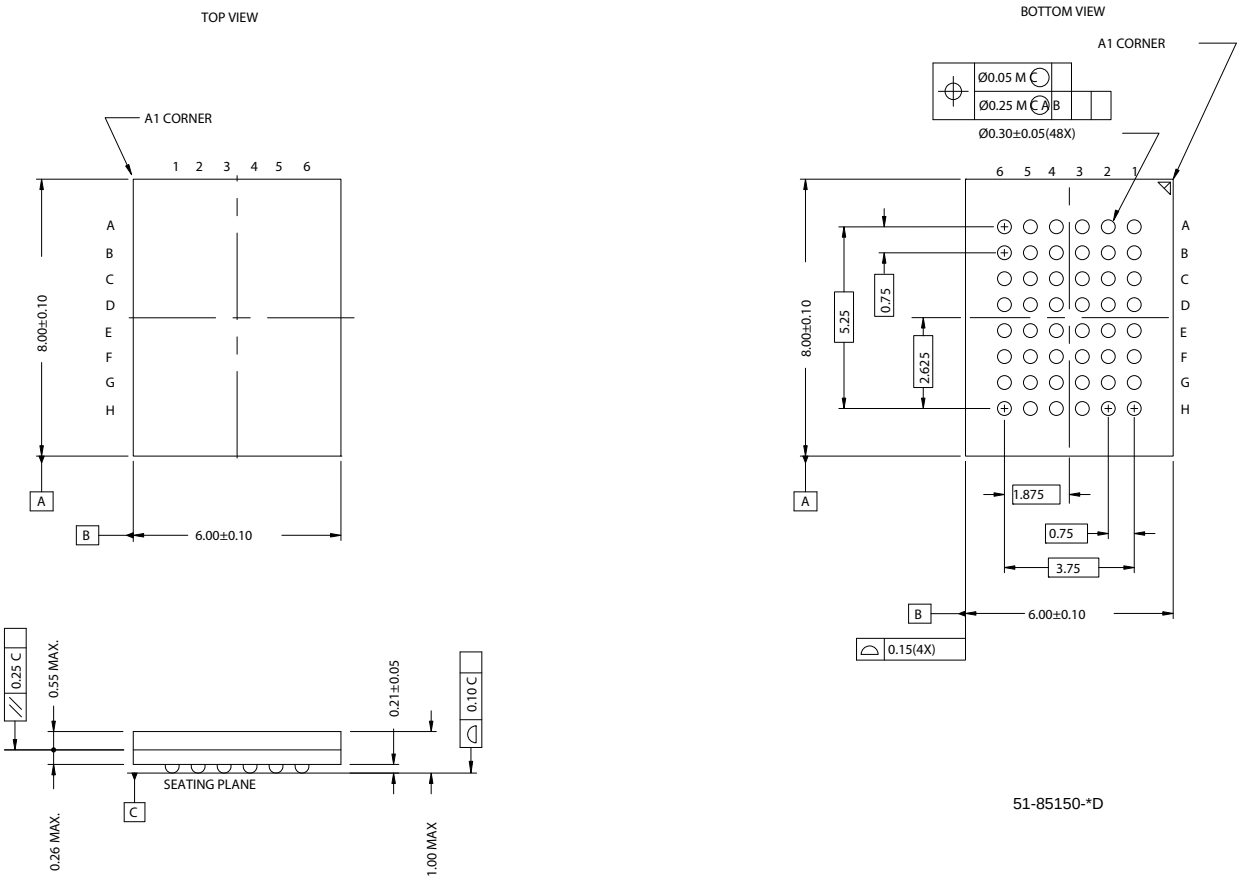
NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
   BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064-*C

Package Diagrams (continued)

Figure 12. 48-Ball FBGA (6 x 8 x 1 mm)



Document History Page

Document Title: CY7C1011CV33, 2-Mbit (128K x 16) Static RAM Document Number: 38-05232				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	117132	07/31/02	HGK	New Data Sheet
*A	118057	08/19/02	HGK	Pin configuration for 48-ball FBGA correction
*B	119702	10/11/02	DFP	Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA
*C	386106	See ECN	PCI	Added lead-free parts in Ordering Information Table
*D	498501	See ECN	NXR	Corrected typo in the Logic Block Diagram on page# 1 Included the Maximum Ratings for Static Discharge Voltage and Latch up Current on page# 3 Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table
*E	522620	See ECN	VKN	Added Thermal Resistance Table
*F	1891366	See ECN	VKN/AESA	Added -10ZSXA part Updated Ordering Information table