

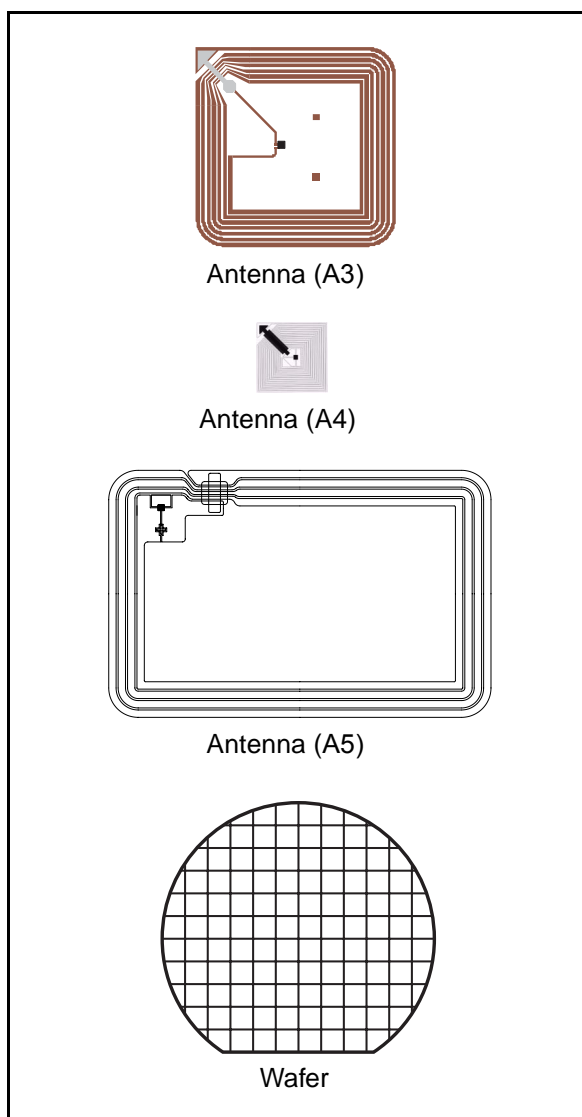


13.56-MHz Short-range Contactless Memory Chip with 512-bit EEPROM and Anti-Collision functions

Data Brief

Features

- ISO 14443 - 2 Type B Air Interface Compliant
- ISO 14443 - 3 Type B Frame Format Compliant
- 13.56MHz Carrier Frequency
- 847kHz Sub-carrier Frequency
- 106 kbit/second Data Transfer
- 8-bit Chip_ID based anticollision system
- 2 Count-Down Binary Counters with automated Anti-tearing protection
- 64-bit Unique Identifier
- 512-bit EEPROM with Write Protect feature
- Read Block and Write Block (32 bits)
- Internal Tuning Capacitor
- 1million Erase/Write Cycles
- 40-Year Data Retention
- Self-Timed Programming Cycle
- 5ms Typical Programming Time

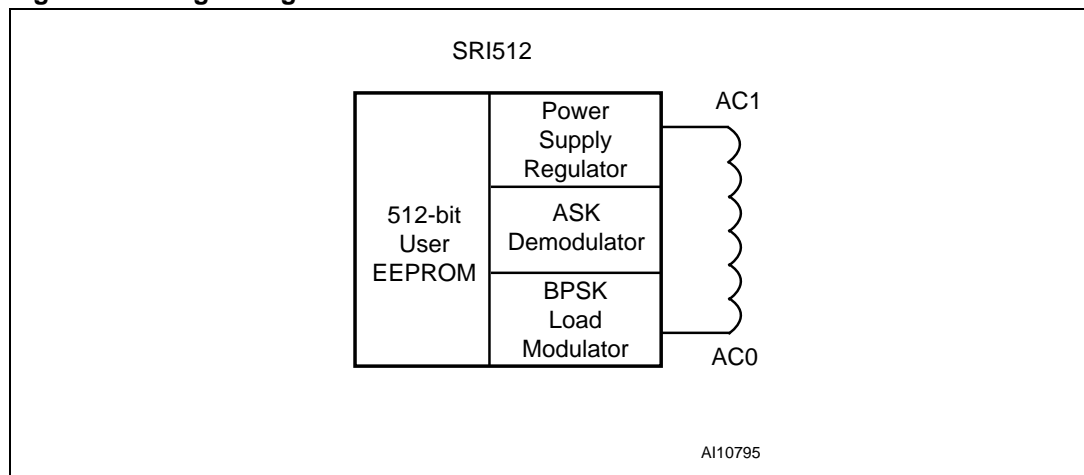


Summary description

The SRI512 is a contactless memory, powered by an externally transmitted radio wave. It contains a 512-bit user EEPROM fabricated with STMicroelectronics CMOS technology. The memory is organized as 16 blocks of 32 bits. The SRI512 is accessed via the 13.56MHz carrier. Incoming data are demodulated and decoded from the received Amplitude Shift Keying (ASK) modulation signal and outgoing data are generated by load variation using Bit Phase Shift Keying (BPSK) coding of a 847kHz sub-carrier. The received ASK wave is 10% modulated. The Data transfer rate between the SRI512 and the reader is 106kbit/s in both reception and emission modes.

The SRI512 follows the ISO 14443 part 2 type B recommendation for the radio-frequency power and signal interface.

Figure 1. Logic Diagram



The SRI512 is specifically designed for short range applications that need re-usable products. The SRI512 includes an anti-collision mechanism that allows it to detect and select tags present at the same time within range of the reader. Using the STMicroelectronics single chip coupler, CRX14, it is easy to design a reader and build a contactless system.

Table 1. Signal Names

AC1	Antenna Coil
AC0	Antenna Coil

The SRI512 contactless EEPROM can be randomly read and written in block mode (each block containing 32 bits). The instruction set includes the following nine commands:

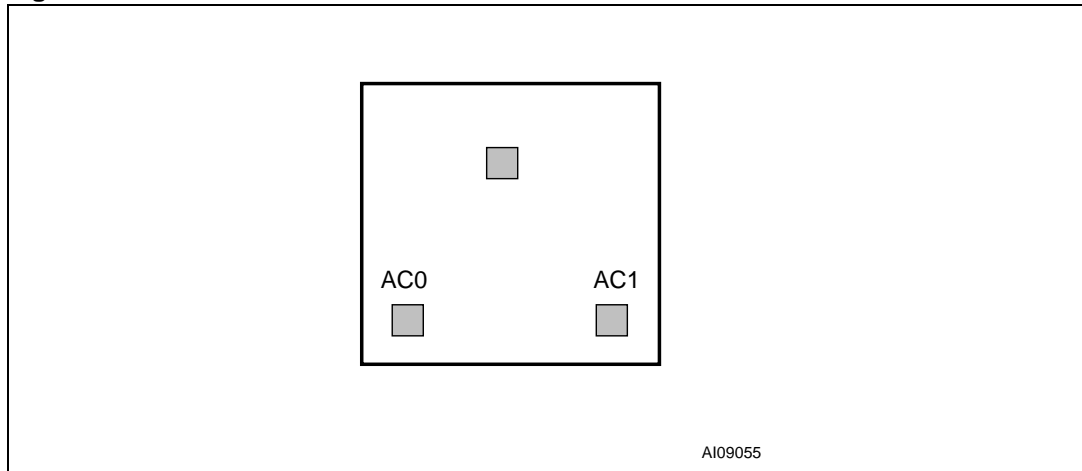
- READ_BLOCK
- WRITE_BLOCK
- INITIATE
- PCALL16
- SLOT_MARKER
- SELECT
- COMPLETION
- RESET_TO_INVENTORY
- GET_UID

The SRI512 memory is organized in three areas. The first area is a resettable OTP (one-time programmable) area in which bits can only be switched from 1 to 0. Using a special command, it is possible to erase all bits of this area to 1. Optionally, this area can be set as an EEPROM area where all blocks behave as User blocks. This option is set by ST on request.

The second area provides two 32-bit binary counters that can only be decremented from FFFFFFFFh to 00000000h, and gives a capacity of 4,294,967,296 units per counter.

The last area is the EEPROM memory. It is accessible by block of 32 bits and includes an auto-erase cycle during each WRITE_BLOCK command.

Figure 2. Die Floor Plan



Memory mapping

The SRI512 is organized as 16 blocks of 32 bits as shown in [Table 2](#). All blocks are accessible by the READ_BLOCK command. Depending on the write access, they can be updated by the WRITE_BLOCK command. A WRITE_BLOCK updates all the 32 bits of the block.

Table 2. SRI512 memory mapping

Block Addr	Msb b ₃₁	32 bits Block				Lsb b ₀	Description
		b ₁₆	b ₁₅	b ₁₄	b ₈ b ₇		
0		32 bits Boolean Area (option: User Area)					Resettable OTP bits (option: lockable EEPROM)
1		32 bits Boolean Area (option: User Area)					
2		32 bits Boolean Area (option: User Area)					
3		32 bits Boolean Area (option: User Area)					
4		32 bits Boolean Area (option: User Area)					
5		32 bits binary counter					Count down Counter
6		32 bits binary counter					
7		User Area					Lockable EEPROM
8		User Area					
9		User Area					
10		User Area					
11		User Area					
12		User Area					
13		User Area					
14		User Area					
15		User Area					
255		OTP_Lock_Reg	OTP_Config	ST Reserved	Fixed Chip_ID (Option)	System OTP bits	
UID0		64 bits UID Area				ROM	
UID1							

Part numbering

Table 3. Ordering Information Scheme

Example:	SRI512	–	W4 / XXX
Device Type	SRI512		
Package	W4 = 180 μm ± 15 μm Unsaun Wafer SBN18 = 180μm ± 15 μm Bumped and Sawn Wafer on 8-inch Frame A3T = 38mm x 38mm Copper Antenna on Continuous Tape A3S = 38mm x 38mm Copper Singulated Adhesive Antenna on Tape A4T = 15mm x 15mm Copper Antenna on Continuous Tape A4S = 15mm x 15mm Copper Singulated Adhesive Antenna on Tape A5T = 42mm x 65mm Copper Antenna on Continuous Tape A5S = 42mm x 65mm Copper Singulated Adhesive Antenna on Tape		
Customer Code	XXX = Given by STMicroelectronics		

Note: Devices are shipped from the factory with the memory content bits erased to 1.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Revision history

Table 4. Document revision history

Date	Revision	Changes
23-Mar-2006	1	Initial release.
18-Apr-2006	2	Added <i>Memory mapping on page 4.</i>

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