μA108A • μA208A • μA308A
μA108 • μA208 • μA308
SUPER BETA OPERATIONAL AMPLIFIERS
FAIRCHILD LINEAR INTEGRATED CIRCUITS

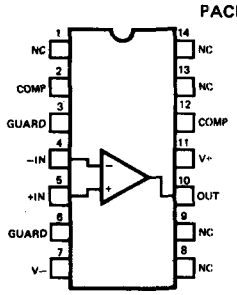
GENERAL DESCRIPTION – The 108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. High input impedance, low noise, input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The 108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT OFFSET CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT**
- **LOW BIAS CURRENT**
- **OPERATION OVER WIDE SUPPLY RANGE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
μA108A, μA108, μA208A, μA208	±20 V
μA308A, μA308	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (μA108A, μA108)	−55°C to +125°C
Industrial (μA208A, μA208)	−25°C to +85°C
Commercial (μA308A, μA308)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	300°C
Output Short Circuit Duration (Note 4)	Indefinite

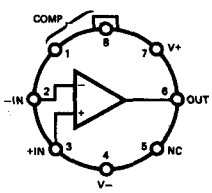
14-LEAD DIP **
(TOP VIEW)
PACKAGE OUTLINE 6A
PACKAGE CODE D



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AD
μA108	μA108D
μA208A	μA208AD
μA208	μA208D
μA308A	μA308AD
μA308	μA308D

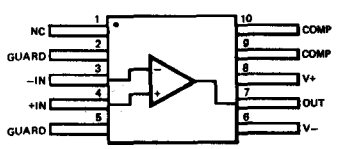
CONNECTION DIAGRAMS
8-LEAD METAL CAN
(TOP VIEW)
PACKAGE OUTLINE 6S
PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μA108A	μA108AH
μA108	μA108H
μA208A	μA208AH
μA208	μA208H
μA308A	μA308AH
μA308	μA308H

10-LEAD FLATPAK**
(TOP VIEW)
PACKAGE OUTLINE 3F
PACKAGE CODE F



ORDER INFORMATION

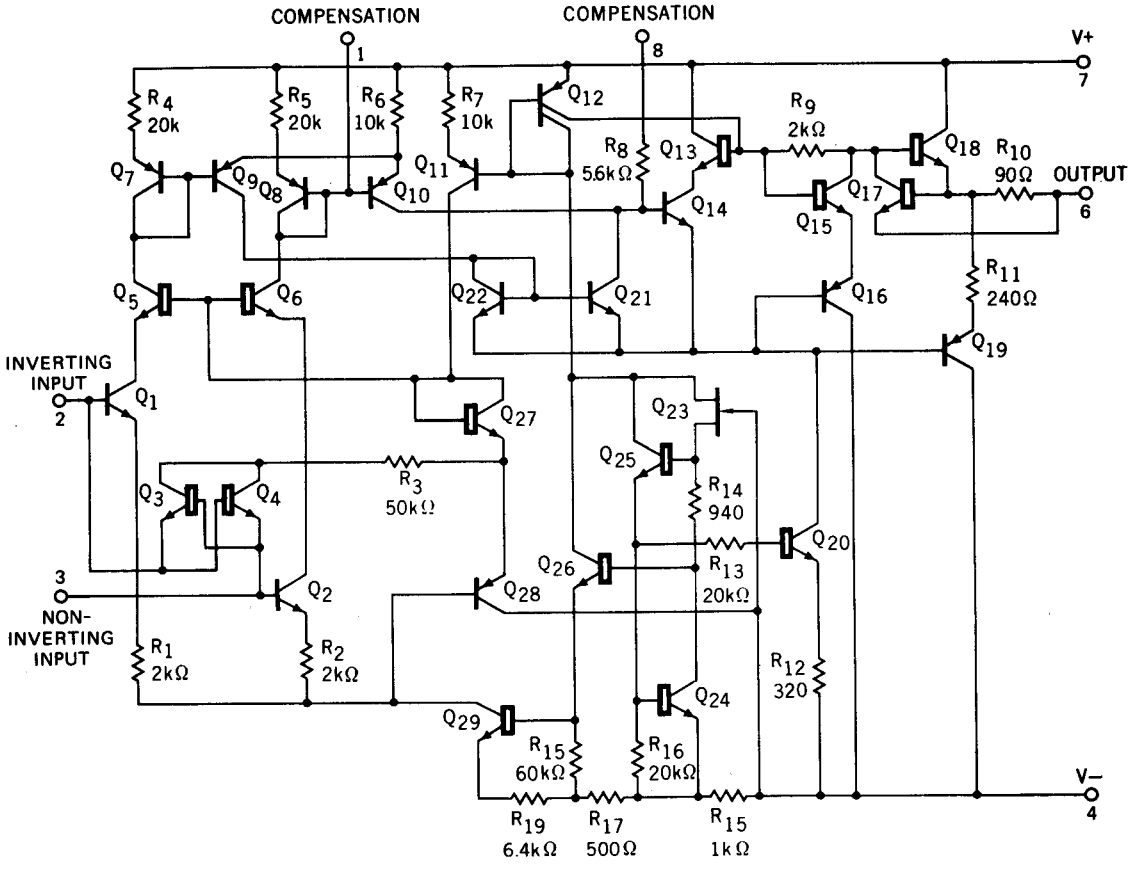
TYPE	PART NO.
μA108A	μA108AF
μA108	μA108F
μA208A	μA208AF
μA208	μA208F

** Available on special order

See notes on following pages.

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



Pin numbers are for metal can only

12

ELECTRICAL CHARACTERISTICS FOR μA108A AND μA208A ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.6	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	80,000	300,000		V/V
The following specifications apply for $-55°C \leq T_A \leq +125°C$ (Note 5)					
Input Offset Voltage				1.0	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current			0.8	3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$ $V_{OUT} = \pm 10\ V$	40,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$	±13	±14		V

ELECTRICAL CHARACTERISTICS FOR μA308A ($\pm 5\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	80,000	300,000		V/V
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage				0.73	mV
Average Input Offset Voltage Drift			1.0	5.0	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	60,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$	±13	±14		V

NOTES:

1. The maximum junction temperature of the 108A/108 is 150°C, while that of the 208A/208 is 100°C, and 308A/308 is 85°C. For operating at elevated temperatures, devices in the TO-99 package must be derated based on thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flatpak package maximum rating of 300 mW applies and derating is based on a thermal resistance of 185°C/W when mounted on a 1/16 inch thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the Dual In-line Package is 100°C/W, junction to ambient.
2. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
3. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
4. Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
5. For the 208A/208, all temperature specifications apply over $-25°C \leq T_A \leq 85°C$.

ELECTRICAL CHARACTERISTICS FOR μA108 AND μA208 ($\pm 5\ V \leq V_S \leq \pm 20\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.7	2.0	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.6	mA
Large Signal Voltage Gain	$R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$ $V_S = \pm 15\ V$	50,000	300,000		V/V
The following specifications apply for $-55°C \leq T_A \leq 125°C$ (Note 5)					
Input Offset Voltage				3.0	mV
Average Input Offset Voltage Drift			3.0	15	μV/°C
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	pA/°C
Input Bias Current				3.0	nA
Supply Current	$T_A = +125°C$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		85	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	25,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		V

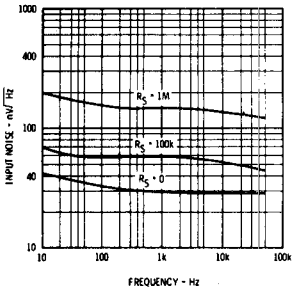
ELECTRICAL CHARACTERISTICS FOR μA308 ($\pm 5\ V \leq V_S \leq \pm 15\ V$, $T_A = 25°C$, $C_C = 30\ pF$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		MΩ
Supply Current	$V_S = \pm 15\ V$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	25,000	300,000		V/V
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage				10	mV
Average Input Offset Voltage Drift			6.0	30	μV/°C
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	pA/°C
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\ V$	±13.5			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 10\ k\Omega$, $V_{OUT} = \pm 10\ V$	15,000			V/V
Output Voltage Swing	$V_S = \pm 15\ V$, $R_L = 10\ k\Omega$	±13	±14		V

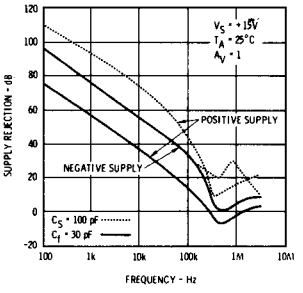
12

TYPICAL PERFORMANCE CURVES FOR μA108 SERIES

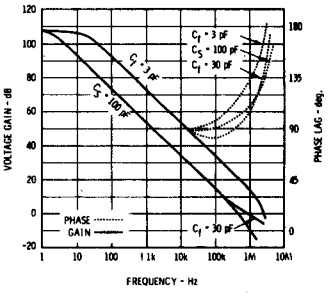
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



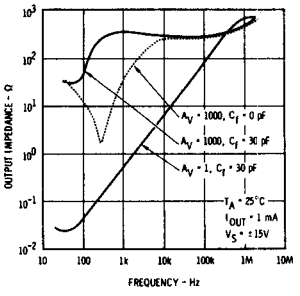
POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY



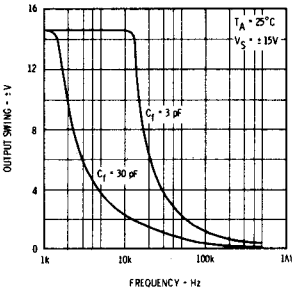
OPEN LOOP FREQUENCY RESPONSE



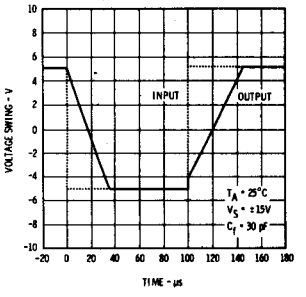
CLOSED LOOP OUTPUT IMPEDANCE



LARGE SIGNAL FREQUENCY RESPONSE

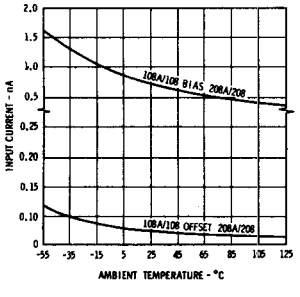


VOLTAGE FOLLOWER PULSE RESPONSE

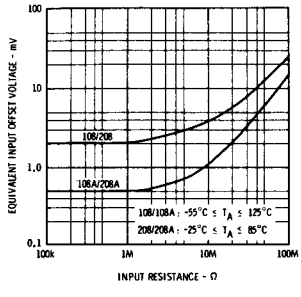


TYPICAL PERFORMANCE CURVES FOR μA108A • μA208A • μA108 • μA208 (Unless Otherwise Specified)

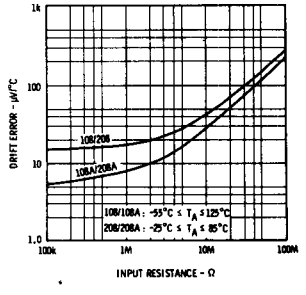
INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



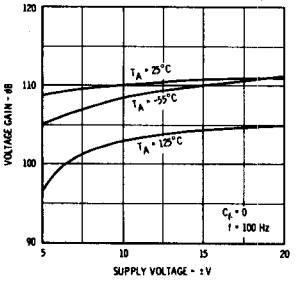
MAXIMUM OFFSET ERROR



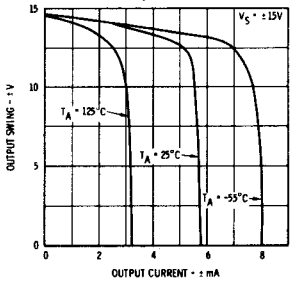
MAXIMUM DRIFT ERROR



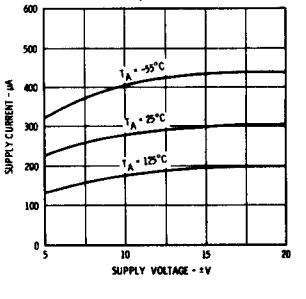
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE μA108



OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT μA108

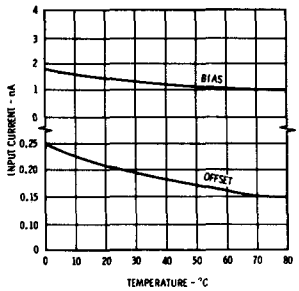


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE μA108

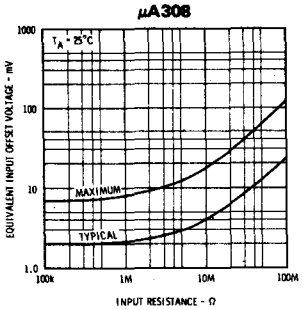


TYPICAL PERFORMANCE CURVES FOR μA308A AND μA308 (Unless Otherwise Specified)

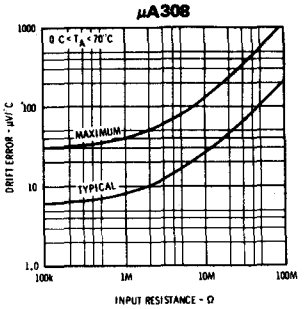
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



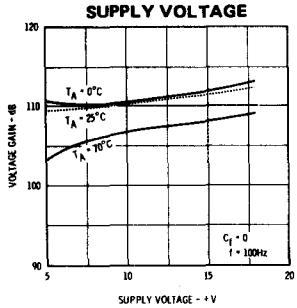
MAXIMUM OFFSET ERROR μA308



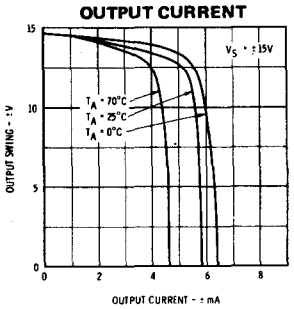
MAXIMUM DRIFT ERROR μA308



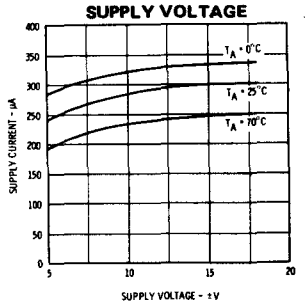
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



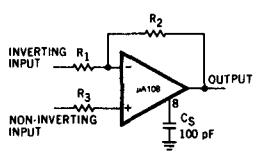
OUTPUT SWING AS A FUNCTION OF OUTPUT CURRENT

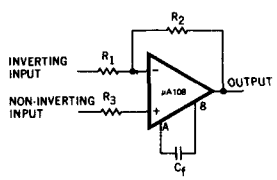


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



STANDARD COMPENSATION CIRCUITS

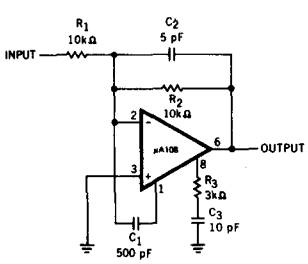




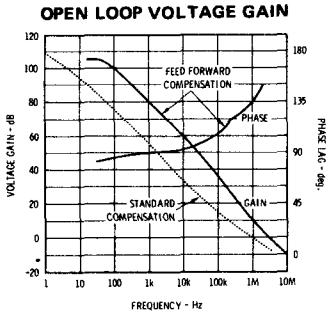
$$C_f \geq 30\left(\frac{1}{1+\frac{R_2}{R_1}}\right)$$

FEEDFORWARD COMPENSATION HIGHER SLEW RATES AND WIDER BANDWIDTH

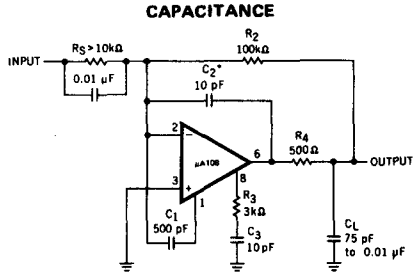
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION FOR DECOUPLING LOAD CAPACITANCE



*$C_2 > \frac{5 \times 10^5}{R_2}$ pF

GUARDING

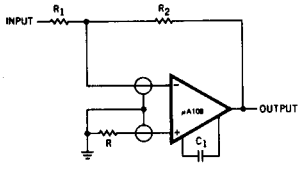
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the Dual In-line Package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard μA741 and 101A pin configuration).

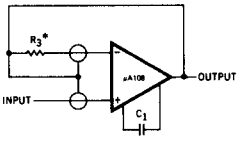
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



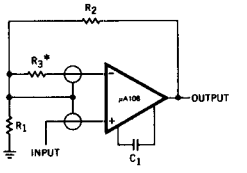
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



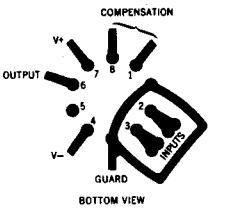
*Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER



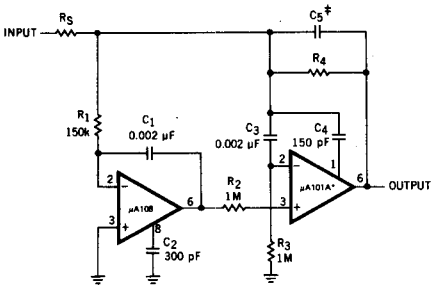
NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE (BOTTOM VIEW)



TYPICAL APPLICATIONS

FAST† SUMMING AMPLIFIER WITH LOW INPUT CURRENT

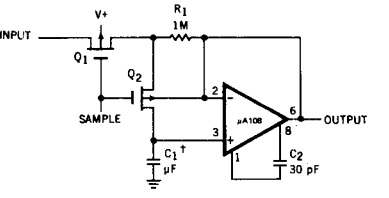


*In addition to increasing speed, the 101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

‡ $C_5 = \frac{6 \times 10^{-6}}{R_1}$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s
† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor