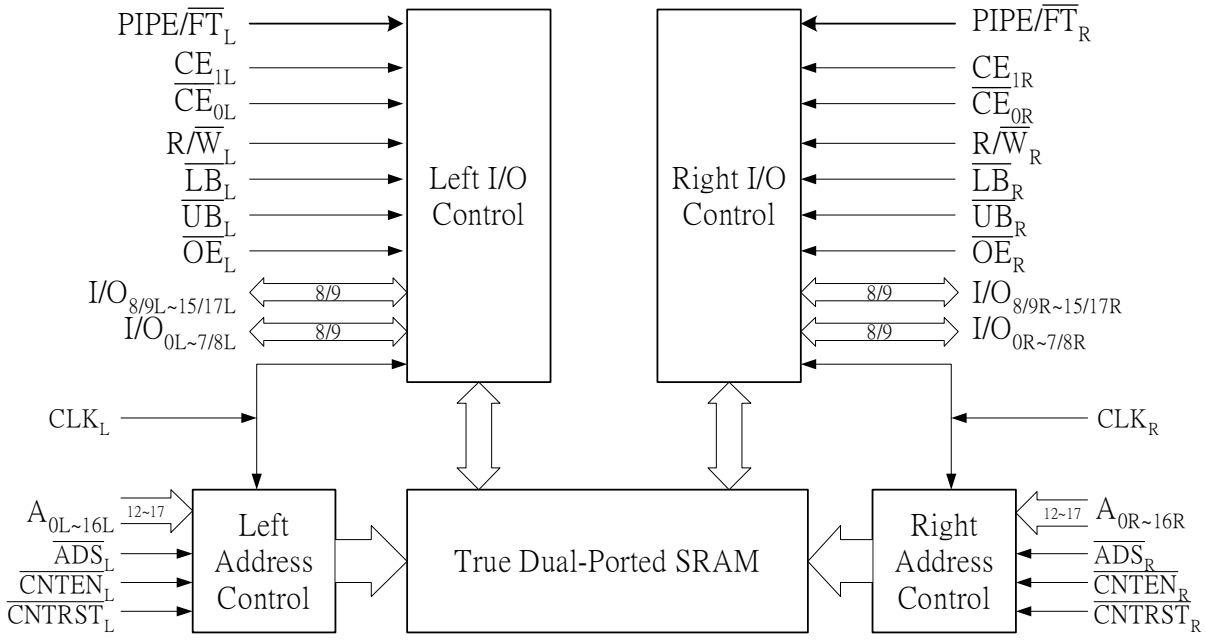
3.3V Synchronous Dual-Port SRAM
4K/8K/16K/32K/64K/128K x 8/9/16/18-bit

Features

- True dual ported memory cells
- 17 Flow-Through/Pipelined devices:
  -- 4K/8K/16K/32K/64K x 18-bit organization (AL5DS9349V/59V/69V/79V/89V)
  -- 16K/32K/64K x 16-bit organization (AL5DS9269V/79V/89V)
  -- 8K/16K/32K/64K/128K x 9-bit organization (AL5DS9159V/69V/79V/89V/99V)
  -- 16K/32K/64K/128K x 8-bit organization (AL5DS9069V/79V/89V/99V)
- Supports byte write/read for 16/18 bit devices
- Separate upper-byte and lower-byte controls for bus matching (16/18 bit devices only)
- 3 modes supported:
  -Pipelined
  -Flow-Through
  -Burst
- Counter enable and reset
- Fast (100-MHz) operation on both ports in Pipelined output mode
- Supports depth and width expansion
- 0.25-micron CMOS for optimum speed / power
- High speed clock to data access
- 3.3V low operating power
- Pin-compatible and functionally equivalent to IDT or Cypress
- Available in 100 or 128 pin TQFP

Architecture



Note 1: $\overline{LB}_R$ and $\overline{UB}_R$ are for 16/18 bit devices only.
Note 2: $I/O_{0\sim7}$ for 8/16 bit devices, $I/O_{0\sim8}$ for 9/18 bit devices, $I/O_{8\sim15}$ for 16 bit devices, and $I/O_{9\sim17}$ for 18 bit devices.
Note 3: $A_{0\sim11}$ for 4K, $A_{0\sim12}$ for 8K, $A_{0\sim13}$ for 16K, $A_{0\sim14}$ for 32K, $A_{0\sim15}$ for 64K, and $A_{0\sim16}$ for 128K devices

Device Descriptions

A Dual-port RAM is a static RAM with a dual-ported cell. There are separate address, data and control signals for each port to access a common SRAM array. A dual-port RAM is generally classified with FIFOs as a "specialty" memory. They are most commonly used in communications that include the exchange of data between processors, processes and systems.

Each port contains an internal counter for fast memory access applications. The initial address of the internal counter is loaded with the port's Address Strobe (/ADS). It also allows the Counter Enable (/CNTEN) to increment the internal counter on each Low to High transition of that port's clock signal. The counter can address the entire memory array and will loop back to start (address 0). The internal counter will be reset to zero while asserting Counter Reset (/CNTRST).

The AL5DS9xx9V is a high speed, 3.3V, synchronous, CMOS, dual-ported SRAM series. The AL5DS9349V/59V/69V/79V/89V are configured as 4K/8K/16K/32K/64K x 18-bit, AL5DS9269V/79V/89V as 16K/32K/64K x 16-bit, AL5DS9159V/69V/79V/89V/99V as 8K/16K/32K/64K/128K x 9-bit and AL5DS9069V/79V/89V/99V as 16K/32K/64K/128 x 8-bit. All these parts support both Pipelined and Flow-Through modes that are selected via the Pipe/FT pin. In the Pipelined mode, two cycles are required to reactivate the data outputs. The AL5DS9xx9V series features dual Chip Enables that allow simple depth and width expansion without external control logic.

All parts are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages. AL5DS9269V/79V/89V and AL5DS9379V/89V are also available in 128-pin TQFP packages.

For more information regarding AL5DS9xx9V synchronous Dual-Port RAM or other AverLogic products, please contact us at your local authorized representatives or visit our web site listed below.

Applications

- Cellular Base Stations
- Cellular Phones
- Multi-protocol Routers
- LAN/WAN Switches
- PBXs
- RAIDs (Storage Networks)
- Set-top Boxes
- Audio/Video Editing
- Graphics Accelerators
- Satellite Encoders
- Cable Modems
- Flight Simulators
- High-end Printing Servers
- Ultrasound Imaging

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