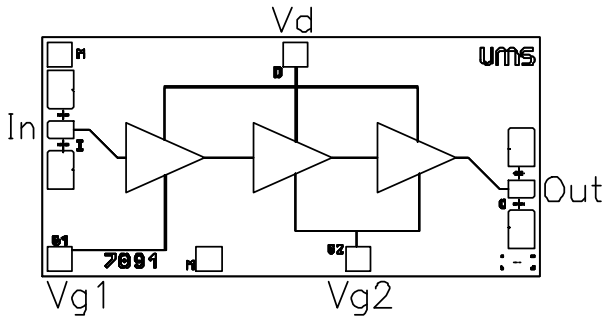
20-30GHz Low Noise Amplifier

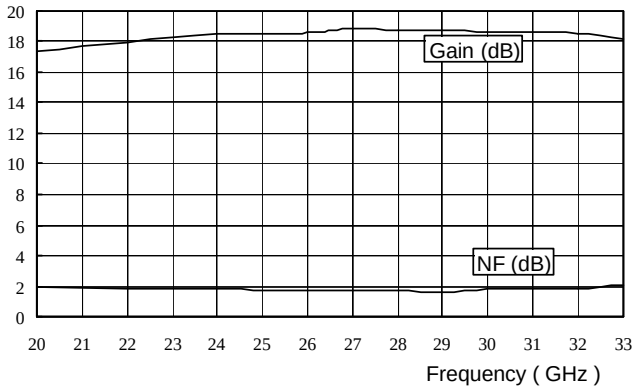
GaAs Monolithic Microwave IC

Description

The CHA2193 is a three stages low noise amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.





Typical on Wafer Measurements

Main Features

- 2.0 dB noise figure
- 18 dB ± 1dB gain
- 8 dBm output power (-1dB gain comp.)
- Very good broadband input matching
- DC power consumption, 60mA @ 3.5V
- Chip size : 2.07 x 1.03 x 0.10 mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	20		30	GHz
G	Small signal gain	16	18		dB
NF	Noise figure		2.0	2.5	dB
P1dB	Output power at 1dB gain compression	6	8		dBm
Id	Bias current		60	100	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Narrowband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	24		26	GHz
G	Small signal gain (1)	16	18		dB
ΔG	Small signal gain flatness (1)		±0.5		dB
Is	Reverse isolation (1)	25	30		dB
NF	Noise figure		2.0	2.5	dB
P1dB	CW output power at 1dB compression (1)	6	8		dBm
VSWRin	Input VSWR (1)		1.8:1	2.0:1	
VSWRout	Output VSWR (1)		1.8:1	2.0:1	
Vd	DC Voltage		3.5	4	V
Id	Bias current		60	100	mA

(1) These values are representative for CW on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	120	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) Duration < 1s.

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This low noise amplifier can also be used for broadband operation following the relaxed characteristics shown below.

Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	20		30	GHz
G	Small signal gain (1)	16	18		dB
ΔG	Small signal gain flatness (1)		±1		dB
Is	Reverse isolation (1)	25	30		dB
NF	Noise figure		2.0	2.5	dB
P1dB	CW output power at 1dB compression (1)	6	8		dBm
VSWRin	Input VSWR (1)		2.0:1	3.0:1	
VSWRout	Output VSWR (1)		2.0:1	3.0:1	
Vd	DC Voltage		3.5	4	V
Id	Bias current		60	100	mA

(1) These values are representative for CW on-wafer measurements that are made without bonding wires at the RF ports.

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Typical On Wafer Scattering Parameters and Noise Figure

Bias Conditions : Vd = +3.5V, Id = 60 mA

Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°	NF
1	-0,09	-14,32	-80,74	113,11	-40,30	169,78	-15,37	-135,30	
2	-0,12	-28,71	-81,92	-0,74	-40,82	119,08	-9,93	-131,21	
3	-0,14	-43,08	-77,35	25,09	-42,54	77,54	-6,93	-141,01	
4	-0,18	-57,94	-83,41	-166,09	-51,25	127,54	-5,91	-155,93	
5	-0,22	-72,91	-67,79	-40,02	-28,44	41,42	-5,58	-154,39	
6	-0,26	-88,98	-76,58	-160,06	-33,45	-69,76	-5,08	-162,37	
7	-0,34	-105,52	-79,08	-134,17	-21,80	-126,19	-4,76	-170,76	
8	-0,50	-123,88	-75,04	-97,32	-10,72	177,68	-4,83	-176,52	
9	-0,92	-143,90	-69,60	-106,78	-1,62	126,62	-5,16	179,09	
10	-1,82	-164,35	-66,24	173,75	5,69	71,35	-5,45	176,68	
11	-2,71	178,27	-65,98	101,28	10,50	13,83	-5,68	174,06	
12	-2,83	157,47	-62,37	32,22	13,30	-36,97	-5,92	171,52	
13	-3,00	128,18	-58,73	-15,96	15,32	-81,84	-6,28	168,03	
14	-3,85	90,80	-55,58	-61,72	16,80	-124,31	-6,59	164,79	2,75
15	-5,36	48,78	-53,10	-89,73	17,51	-164,61	-7,18	161,05	
16	-7,12	6,24	-50,87	-128,11	17,54	159,88	-7,81	158,07	2,39
17	-8,37	-33,74	-50,28	-153,61	17,30	130,36	-8,91	155,99	
18	-8,54	-68,42	-49,79	-174,52	17,28	104,28	-9,46	153,50	2,52
19	-8,48	-96,54	-49,80	165,50	17,39	80,17	-10,19	151,85	
20	-8,44	-120,79	-50,15	150,57	17,41	58,32	-10,77	148,38	1,96
21	-8,67	-140,98	-51,37	138,76	17,89	34,39	-11,68	142,69	
22	-9,07	-161,02	-50,08	131,82	18,09	10,95	-12,83	136,93	1,89
23	-10,37	-177,31	-49,49	119,58	18,30	-12,07	-14,17	132,50	
24	-12,87	172,65	-49,57	101,38	18,57	-33,78	-15,50	126,88	1,83
25	-14,41	172,94	-50,14	91,56	19,00	-57,79	-17,55	116,56	
26	-16,02	-179,78	-49,34	75,10	19,05	-80,79	-19,49	105,05	1,74
27	-15,80	-170,46	-50,03	60,07	19,19	-103,36	-21,66	82,30	1,72
28	-13,84	-161,36	-50,36	40,82	19,29	-126,71	-24,61	56,13	1,72
29	-11,86	-164,84	-51,41	23,31	19,21	-149,27	-23,32	16,43	1,66
30	-10,90	-170,62	-52,60	10,51	19,11	-171,38	-23,04	5,95	1,82
31	-9,43	-175,48	-51,86	-9,98	19,24	165,57	-20,98	-11,15	1,90
32	-8,16	176,47	-54,05	-26,91	19,20	141,50	-21,22	-10,65	1,86
33	-7,04	168,81	-52,64	-39,12	18,93	116,42	-20,33	-13,52	2,13
34	-6,00	159,28	-55,11	-64,75	18,67	91,00	-18,22	5,77	
35	-4,99	150,58	-53,15	-62,66	18,15	63,85	-15,72	6,40	
36	-4,01	139,72	-52,03	-79,29	17,22	35,89	-12,74	9,57	
37	-3,08	128,47	-51,22	-91,36	15,94	8,86	-9,98	8,08	
38	-2,41	115,71	-52,00	-110,30	14,33	-17,74	-8,05	4,67	
39	-2,00	104,97	-56,87	-132,32	12,28	-42,47	-6,44	-0,77	
40	-1,45	92,23	-49,81	-37,13	10,30	-66,02	-5,17	-7,26	

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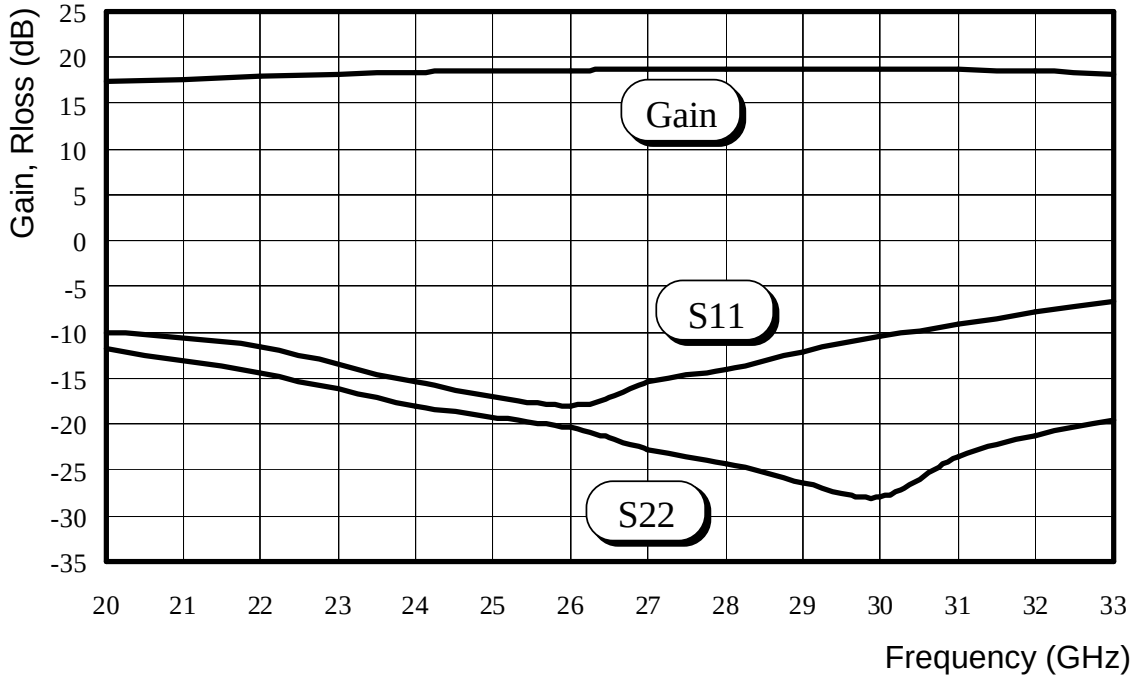
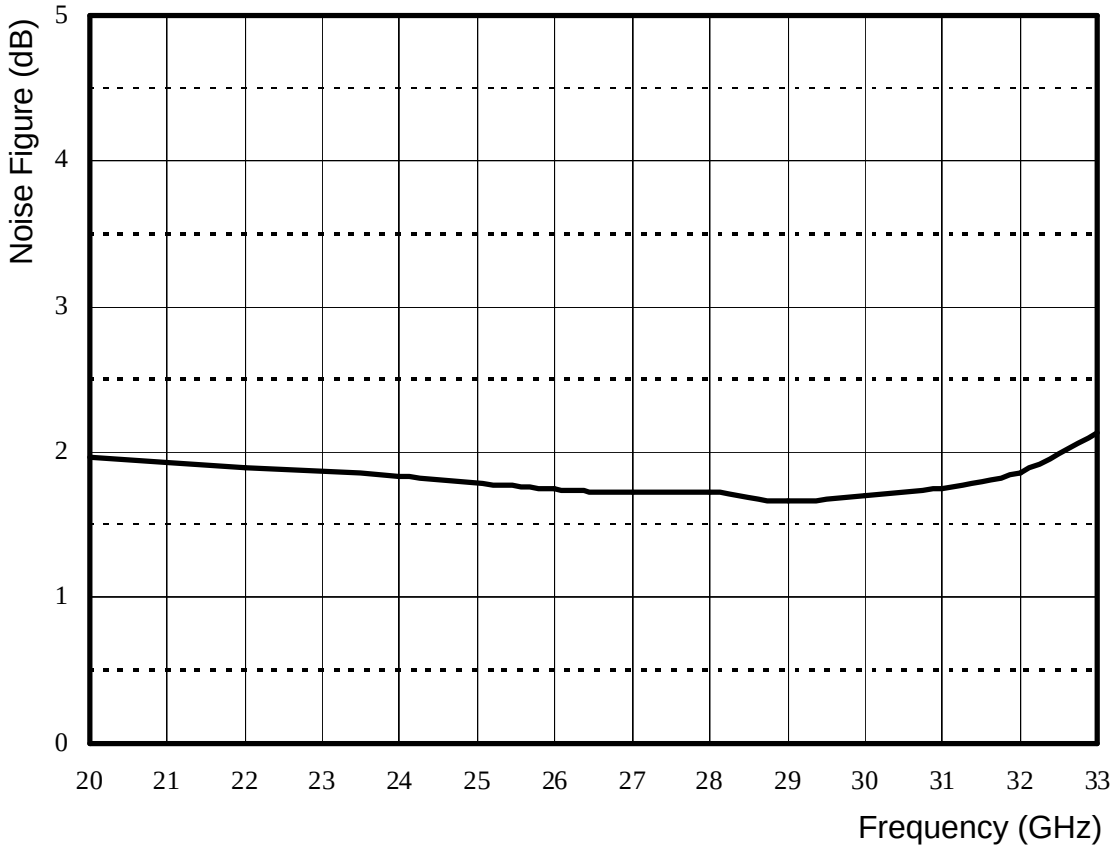
Typical on Wafer Measurements

Bias conditions: Tamb = +25°C, Vd = 3.5V, Vg1 = Vg2, Id = 60mA





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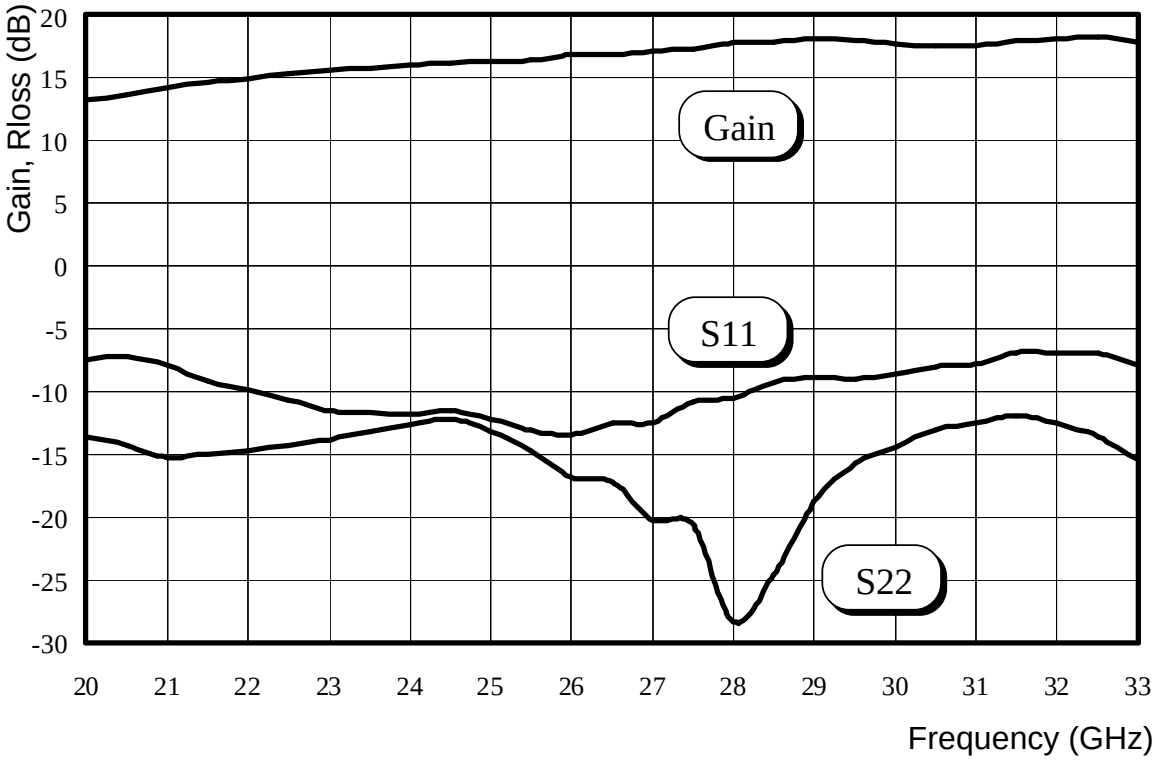

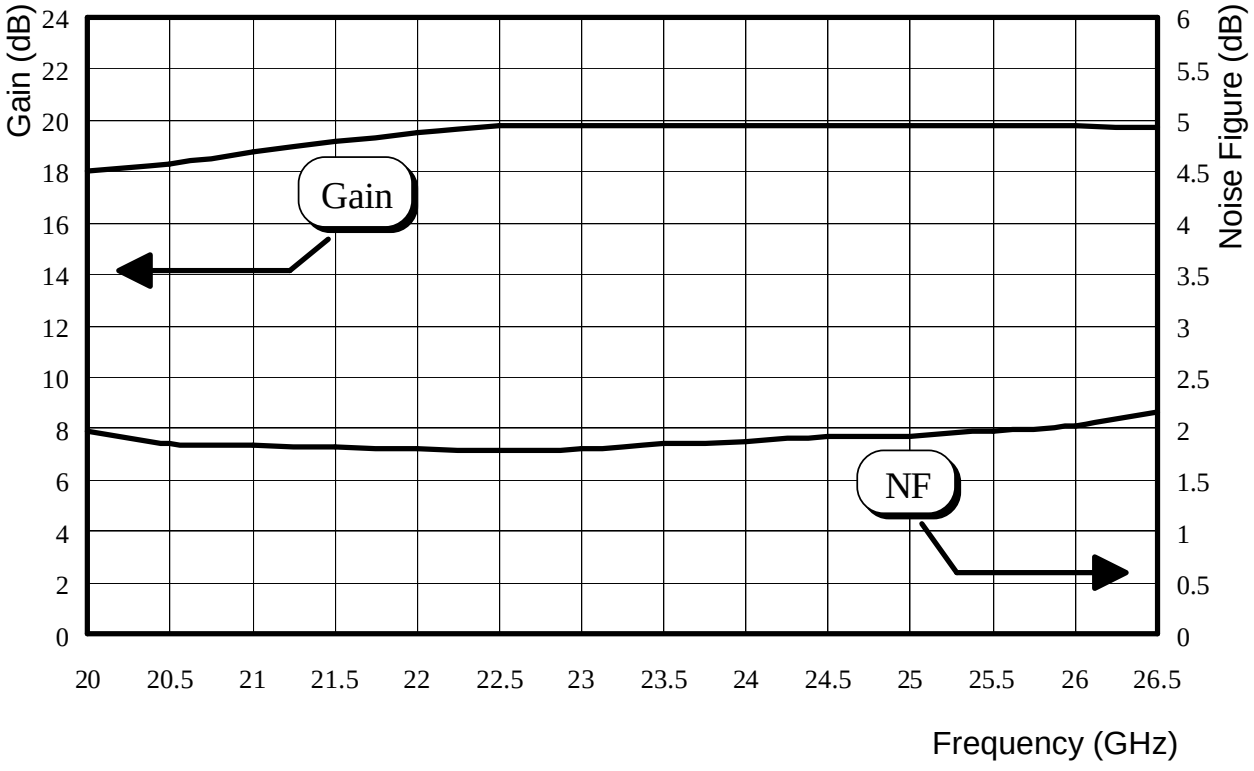

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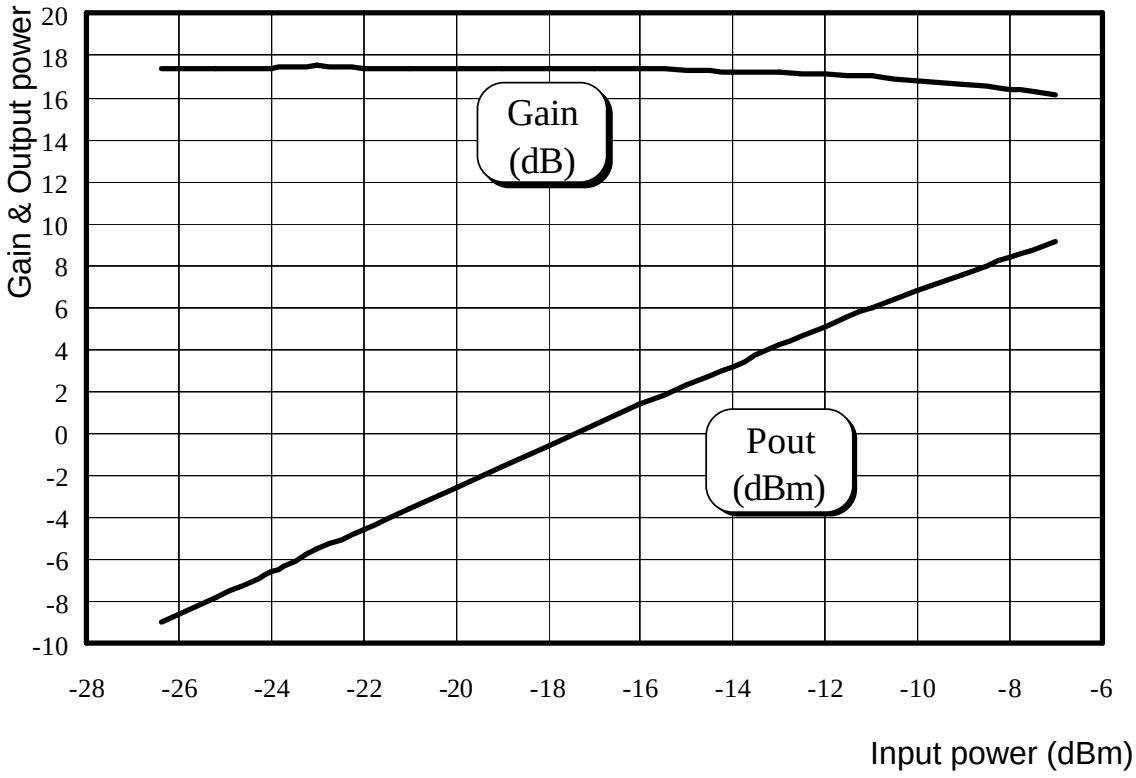

Typical Bias Tuning for Low Noise Operation

For low noise operation, a separate access to the gate voltages of the first stage (Vgs1), and of the second and third stages (Vgs2) is provided.
Nominal bias for low noise operation is obtained for a typical current of 20 mA for the second and third stages and 10 mA for the first stage (50 mA for the amplifier).
The first step to bias the amplifier is to tune the Vgs1 = -1V, and Vgs2 to drive 40 mA for the full amplifier. Then Vgs1 is reduced to obtain 50 mA of current through the amplifier.
A fine tuning of the noise figure may be obtained by modifying the Vgs1 bias voltage, but keeping the previous value for Vgs2.

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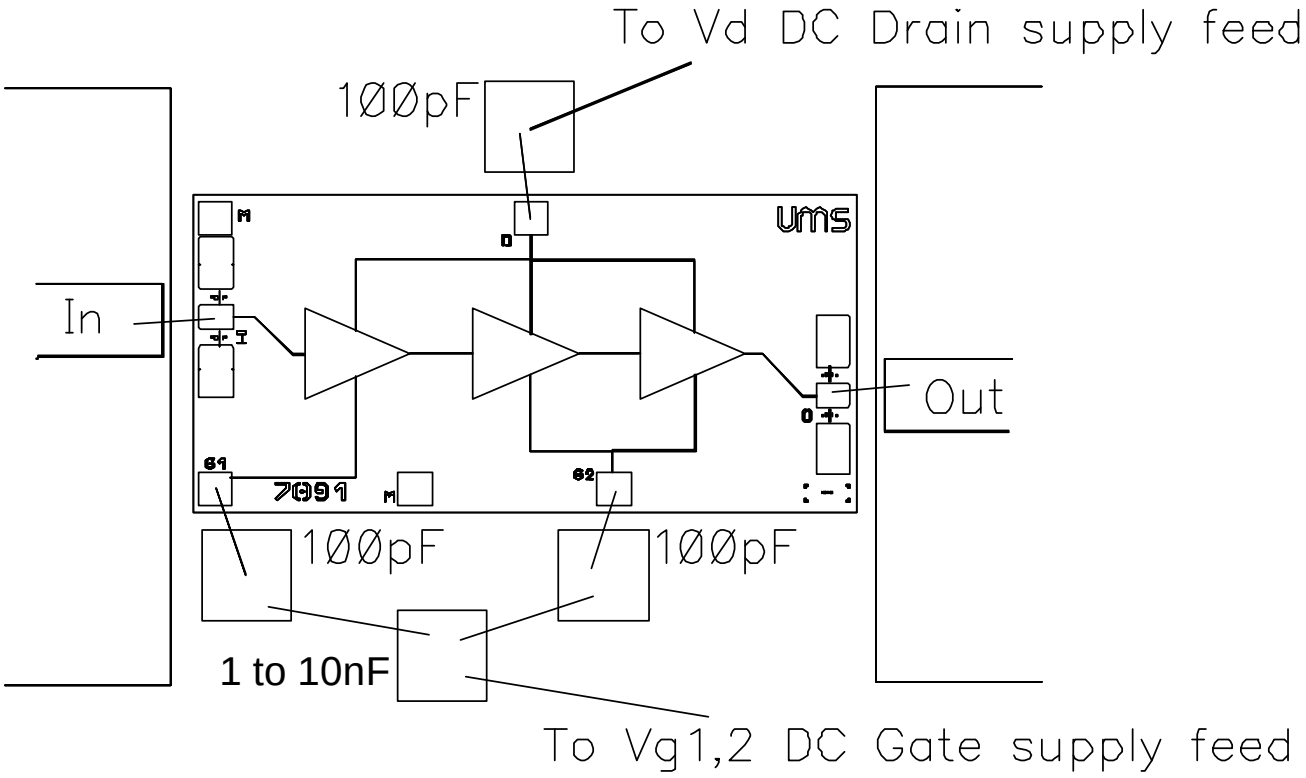
Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered.

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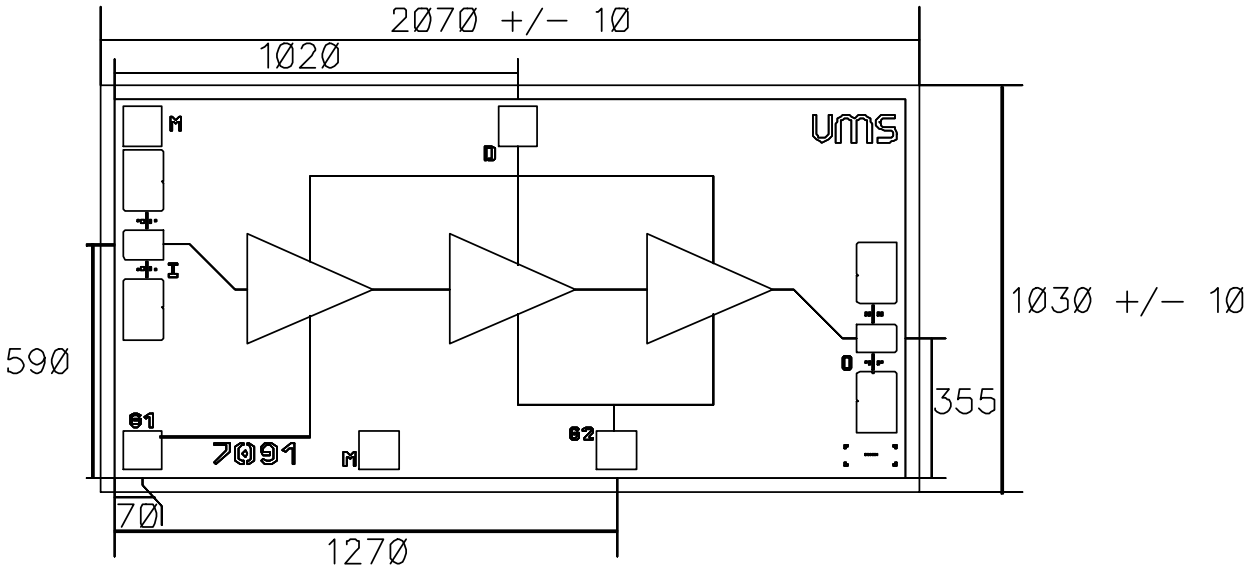

Bonding pad positions.

(Chip thickness : 100µm. All dimensions are in micrometers)

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Ordering Information

Chip form : CHA2193-99F/00

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