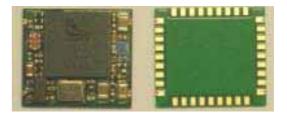
DFBM-CF320 BluetoothTM Module Class 2

A Class 2 Bluetooth module compliant with Bluetooth Specification V2.0+EDR for various application.



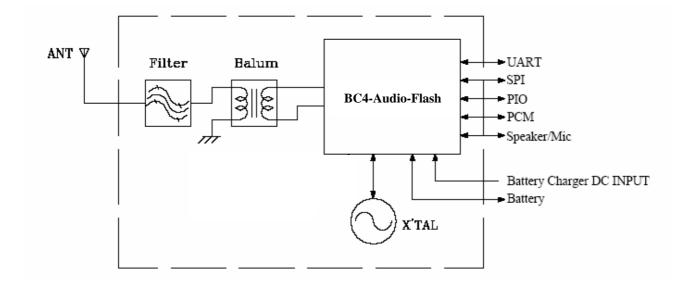
FEATURES:

- Suitable for Headset application with Build-in codec.
- Suitable for Automotive Hands-Free Kits.
- Suitable for General purpose Bluetooth systems requiring an on-chip audio CODEC.
- Small size and Low Profile using high-density packaging technology which compliant with RoHS.
- High sensitivity for better reception.
- Already embedded battery charger, LED driver and switch mode regulator.
- Need few external parts for headset design.
- Variable profiles with 6M Flash.
- Various interfaces: UART, SPI and PCM.
- Wide operating temperature range: -40~+80

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Device diagram



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General Specification

	1
Bluetooth Specification	Version 2.0+EDR
Frequency	2402~2480MHz
Modulation	GFSK/DQPSK/8DPSK
Transmission Rate	721K / 2M / 3M bps
Receive Sensitivity	Typ81.5dBm
Maximum Output Power	+4dBm (Class 2)
Operating Voltage	Refer to Recommend table
Power consumption	Up to 41 mA for SCO connection HV1 * Low to 0.1 mA for standby mode
Battery programmable charge current	25~100mA
Operating Temperature	-40~+80
Antenna Impedance	50Ω
Package Size	13.5*12*2.1 (mm)

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Interface				
Interface	Description			
Antenna	External Antenna 50			
UART Interface	TX, RX, RTS, CTS(9600bps~1.5Mbps)			
SPI Interface	Synchronous Serial Interface for firmware download			
PCM Codec	Qualcomm MSM 3000/5000 , Motorola MC145483/ MC145481 OKI MSM7705 , STW 5093/5094			
PIO Interface	8 terminals			

Rating

	Min	Мах	Unit
Storage Temperature	-40	+150	
VDD_1.8V	-0.4	+2.2	V
VBAT	-0.4	+4.25	V
VREG_EN	-0.4	+4.25	V
VDD_CHG	-0.4	+6.5	V

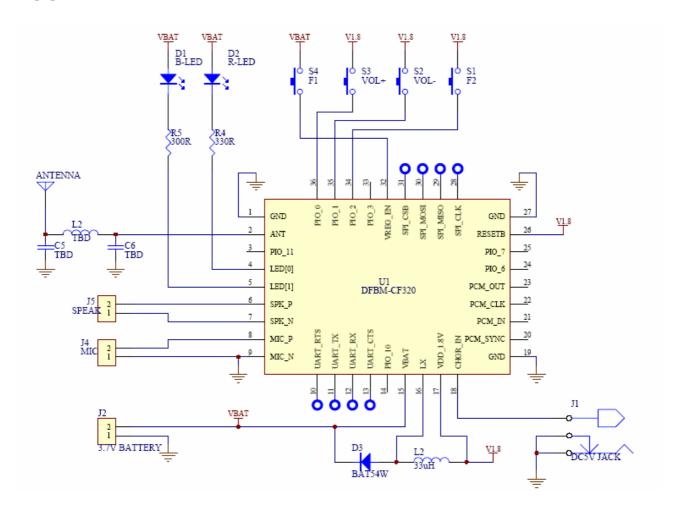
Recommend

	Min	Мах	Unit
VDD_1.8V	+1.7	+1.9	V
VBAT	+2.5	+4.2	V
VREG_EN	+2.5	+4.2	V
VDD_CHG	+4.35	+6.5	V
VDD_CHG current	25	100	mA

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Application circuit



Mono-Headset application circuit

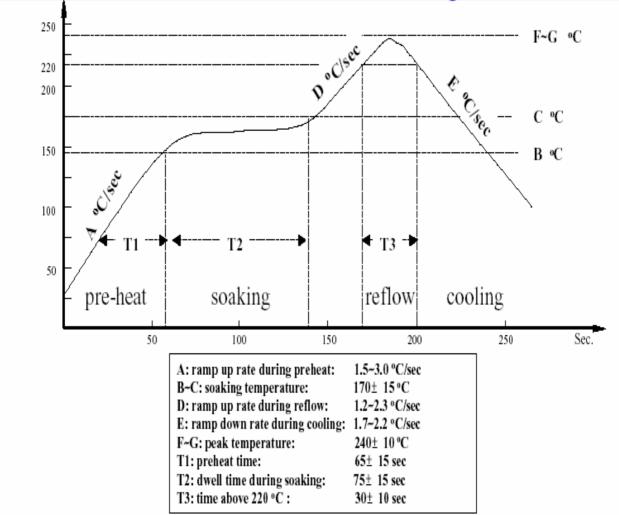
- Note : 1. Please left SPI & UART pins out for further test and evaluation.
 - 2. The circuits are offered without warranty and Delta is unable to accept any liability for direct or consequential loss associated with their use. It is therefore important for designers to ensure that their design is properly evaluated in a Design Verification Test.

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Recommended Reflow Profile

Reflow Profile Used at The Evaluation (Sn-3.0Ag-0.5Cu) – PF606-P



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Pin description				
Pin No.	Name	Description		
1	GND	Ground		
2	ANT	RF input/output		
3	PIO_11	Programmable input/output line		
4	LED_0	Current sink to drive LED		
5	LED_1	Current sink to drive LED		
6	SP+	Speaker output positive		
7	SP-	Speaker output negative		
8	MIC+	Microphone input positive		
9	MIC-	Microphone input negative		
10	UART_RTS	UART request to send active low		
11	UART_TX	UART data output active high		
12	UART_RX	UART data input active high		
13	UART_CTS	UART clear to send active low		
14	PIO_10	Programmable input/output line		
15	VBAT	Lithium Ion battery positive terminal		
16	LX	Switch-mode power regulator output		
17	VDD_1.8V	Supply Voltage (1.8V) input		
18	VDD_CHG	Lithium lon battery charger input		

Data Sheet

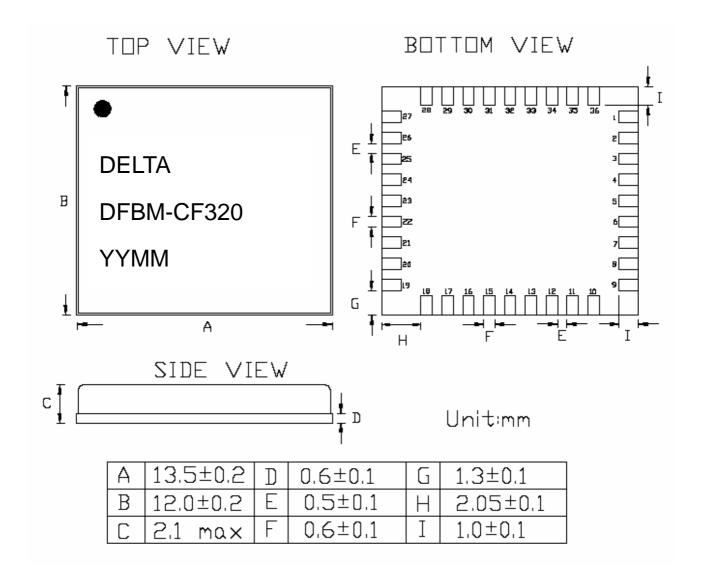
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19	GND	Ground	
20	PCM_SYNC	Synchronous data sync	
21	PCM_IN	Synchronous data input	
22	PCM_CLK	Synchronous data clock	
23	PCM_OUT	Synchronous data output	
24	PIO_6	Programmable input/output line	
25	PIO_7	Programmable input/output line	
26	RESETB	Reset if low	
27	GND	Ground	
28	SPI_CLK	Serial Peripheral Interface clock	
29	SPI_MISO	Serial Peripheral Interface data output	
30	SPI_MOSI	Serial Peripheral Interface data input	
31	SPI_CSB	Chip select for Serial Peripheral Interface, active low	
32	VREG_EN	Regulator control pin	
33	PIO_3	Programmable input/output line	
34	PIO_2	Programmable input/output line	
35	PIO_1	Programmable input/output line	
36	PIO_0	Programmable input/output line	

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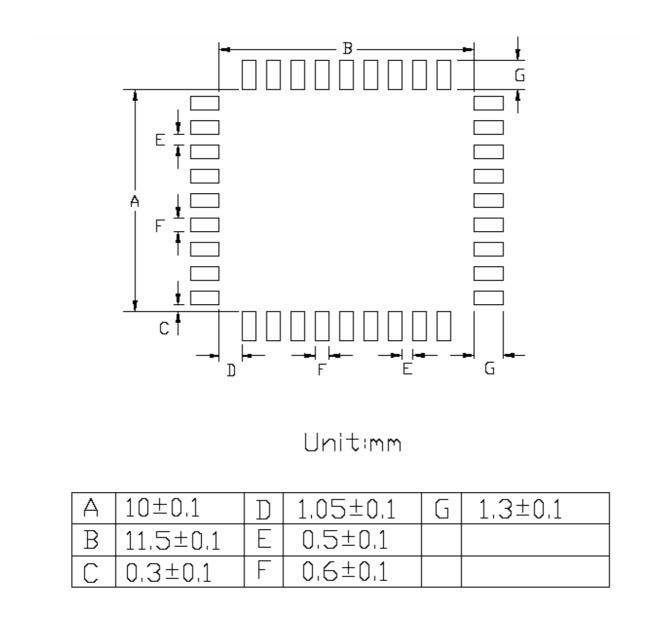
Dimensions (mm)



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Layout Guide



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Record of changes

Date	Content of change	Maker
Jan. 12,2007	Primarily release.	

Jan 12, 2007