

GENERAL DESCRIPTION

The EM6164K600V is a 1,048,576-bit low power CMOS static random access memory organized as 65,536 words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

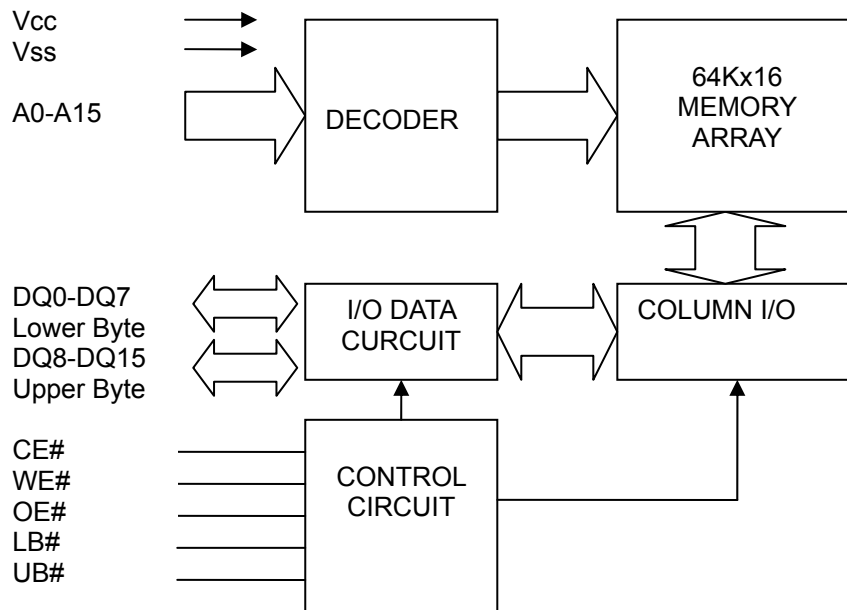
The EM6164K600V is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The EM6164K600V operates from a single power supply of 2.7V ~ 3.6V and all inputs and outputs are fully TTL compatible

FEATURES

- Fast access time: 45/55/70ns
- Low power consumption:
Operating current: 23/20/18mA (TYP.)
Standby current: -L/-LL version 10/1µA (TYP.)
- Single 2.7V ~ 3.6V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control :
LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage: 1.5V (MIN.)
- Package:
44-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM

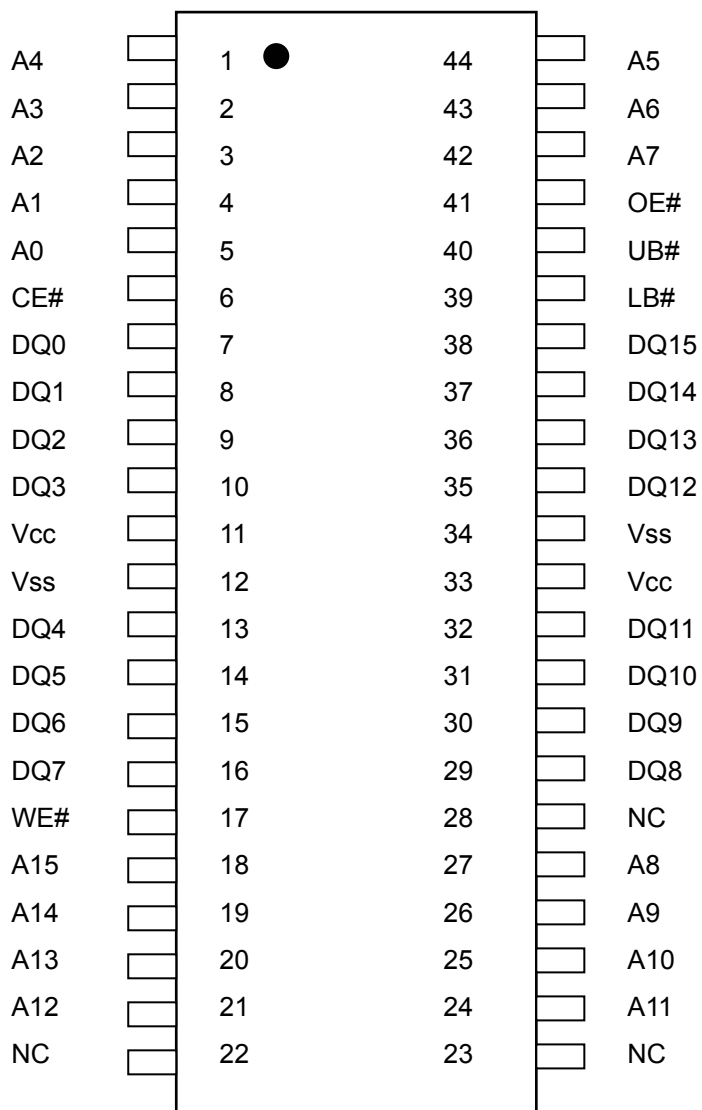


PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
LB#	Lower Byte Control
UB#	Upper Byte Control
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

TSOP-II



TFBGA

A	LB#	OE#	A0	A1	A2	NC
B	DQ8	UB#	A3	A4	CE#	DQ0
C	DQ9	DQ10	A5	A6	DQ1	DQ2
D	Vss	DQ11	NC	A7	DQ3	Vcc
E	Vcc	DQ12	NC	NC	DQ4	Vss
F	DQ14	DQ13	A14	A15	DQ5	DQ6
G	DQ15	NC	A12	A13	WE#	DQ7
H	NC	A8	A9	A10	A11	NC
	1	2	3	4	5	6

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to 4.6	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{SOLDER}	260	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	LB#	UB#	I/O OPERATION		SUPPLY CURRENT
						DQ0-DQ7	DQ8-DQ15	
Standby	H	X	X	X	X	High-Z	High-Z	I _{SB} , I _{SB1}
	X	X	X	H	H	High-Z	High-Z	
Output Disable	L	H	H	L	X	High-Z	High-Z	I _{CC} , I _{CC1}
	L	H	H	X	L	High-Z	High-Z	
Read	L	L	H	L	H	DOUT	High-Z	I _{CC} , I _{CC1}
	L	L	H	H	L	High-Z	DOUT	
	L	L	H	L	L	DOUT	DOUT	
Write	L	X	L	L	H	DIN	High-Z	I _{CC} , I _{CC1}
	L	X	L	H	L	High-Z	DIN	
	L	X	L	L	L	DIN	DIN	

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. *5	MAX.	UNIT	
Supply Voltage	V _{CC}		2.7	3.0	3.6	V	
Input High Voltage	V _{IH} *1		2.0	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL} *2		-0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	+1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.2	2.7	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA	-45	-	23	40	mA
			-55	-	20	35	mA
			-70	-	18	30	mA
	I _{CC1}	Cycle time = 1μs CE# ≤ 0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V	-	4	5	mA	
Standby Power	I _{SB}	CE# = V _{IH}	-	0.3	0.5	mA	

Supply Current	ISB1	CE# V ≥ VCC - 0.2V	-L	-	20	80	μA
			-LL		1	10	μA

Notes:

1. VIH(max) = VCC + 3.0V for pulse width less than 10ns.
2. VIL(min) = VSS - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. 10μA for special request
5. Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and TA = 25°C

CAPACITANCE (TA = 25°C , f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	CIN	-	6	pF
Input/Output Capacitance	CIO	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to VCC - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	CL = 30pF + 1TTL, IOH/IOL = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS

READ CYCLE

PARAMETER	SYM.	-45		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	tRC	45	-	55	-	70	-	ns
Address Access Time	tAA	-	45	-	55	-	70	ns
Chip Enable Access Time	tACE	-	45	-	55	-	70	ns
Output Enable Access Time	tOE	-	25	-	30	-	35	ns
Chip Enable to Output in Low-Z	tCLZ*	10	-	10	-	10	-	ns
Output Enable to Output in Low-Z	tOLZ*	5	-	5	-	5	-	ns
Chip Disable to Output in High-Z	tCHZ*	-	15	-	20	-	25	ns
Output Disable to Output in High-Z	tOHZ*	-	15	-	20	-	25	ns
Output Hold from Address Change	tOH	10	-	10	-	10	-	ns
LB#, UB# Access Time	tBA	-	45	-	55	-	70	ns
LB#, UB# to High-Z Output	tBHZ*	-	20	-	25	-	30	ns
LB#, UB# to Low-Z Output	tBLZ*	10	-	10	-	10	-	ns

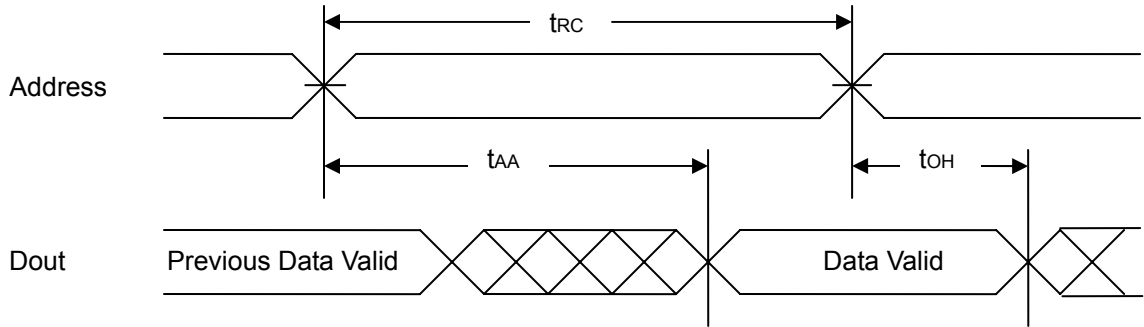
WRITE CYCLE

PARAMETER	SYM.	-45		-55		70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	tWC	45	-	55	-	70	-	ns
Address Valid to End of Write	tAW	40	-	50	-	60	-	ns
Chip Enable to End of Write	tCW	40	-	50	-	60	-	ns
Address Set-up Time	tAS	0	-	0	-	0	-	ns
Write Pulse Width	tWP	35	-	45	-	55	-	ns
Write Recovery Time	tWR	0	-	0	-	0	-	ns
Data to Write Time Overlap	tDW	20	-	25	-	30	-	ns
Data Hold from End of Write Time	tDH	0	-	0	-	0	-	ns
Output Active from End of Write	tOW*	5	-	5	-	5	-	ns
Write to Output in High-Z	tWHZ*	-	15	-	20	-	25	ns
LB#, UB# Valid to End of Write	tBW	35	-	45	-	60	-	ns

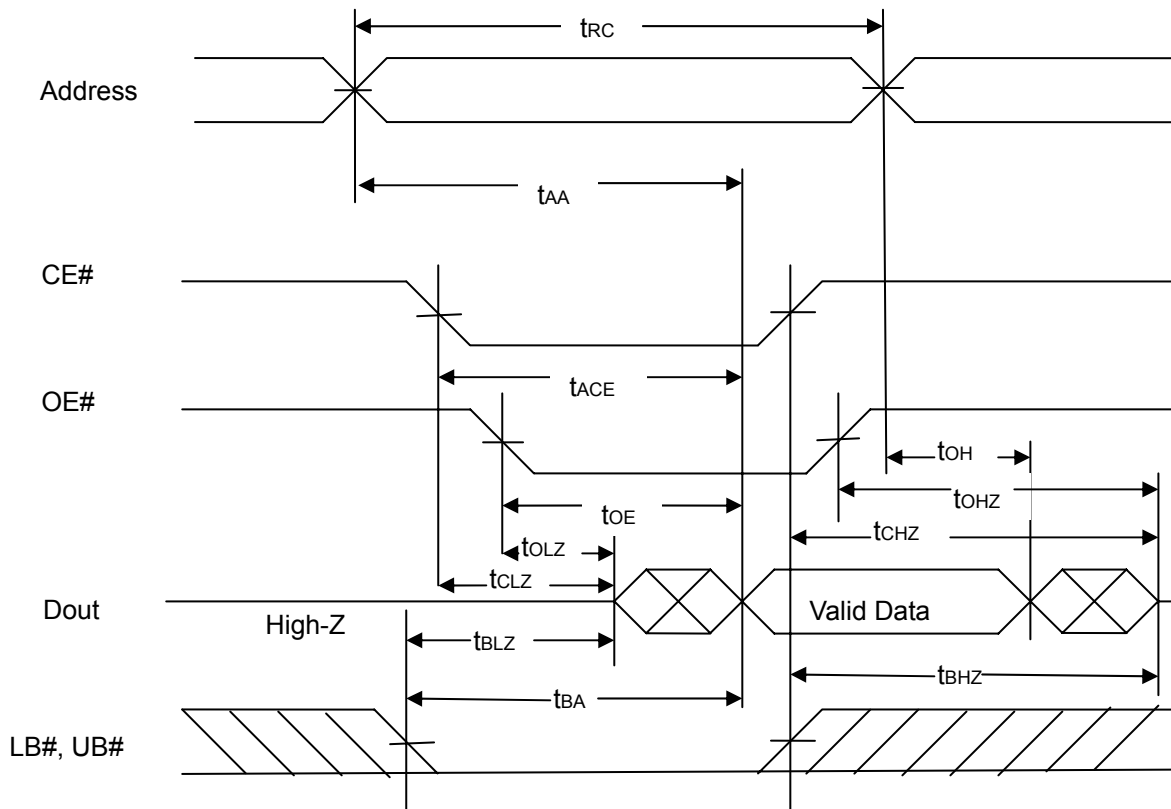
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



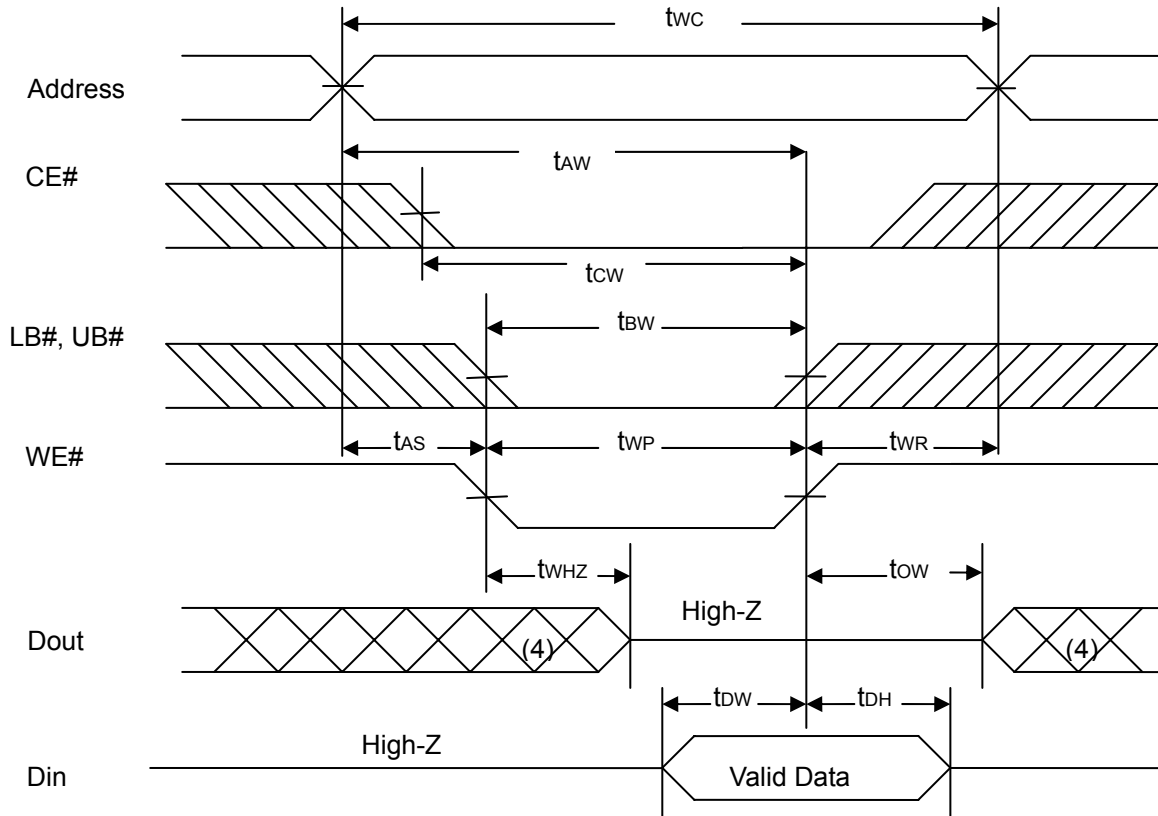
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



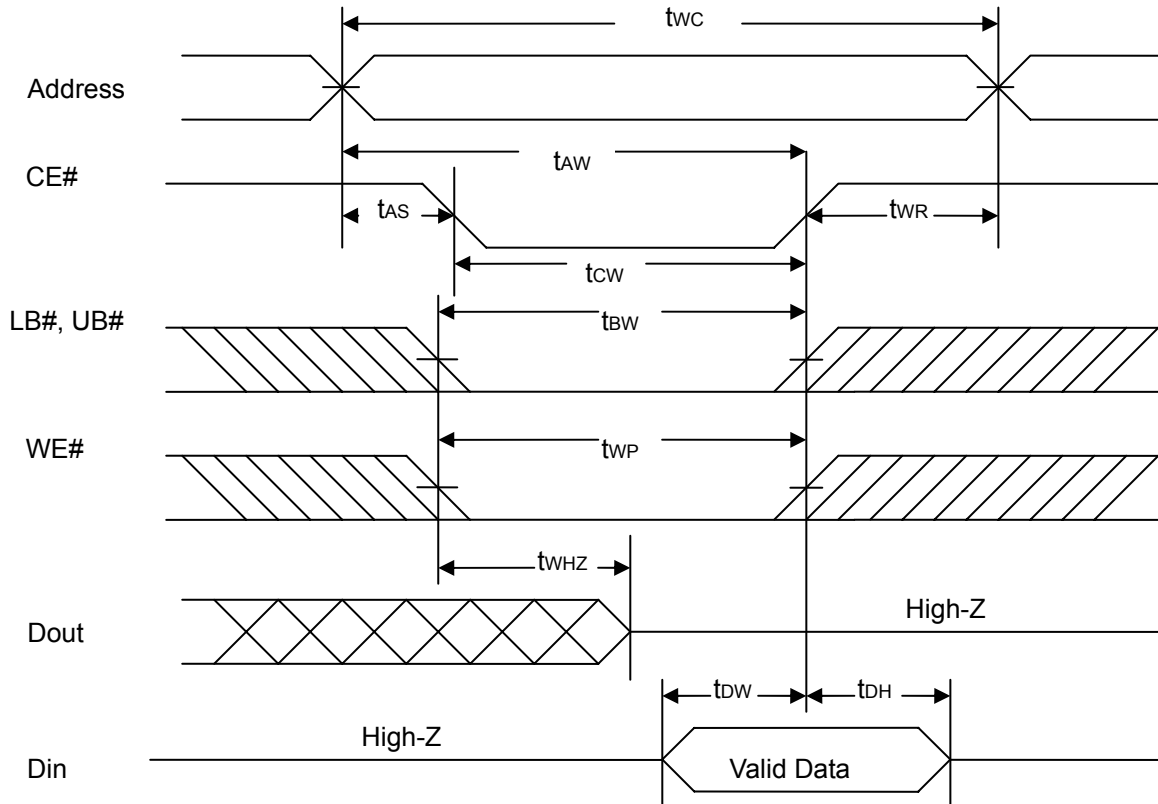
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low,; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $CL = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

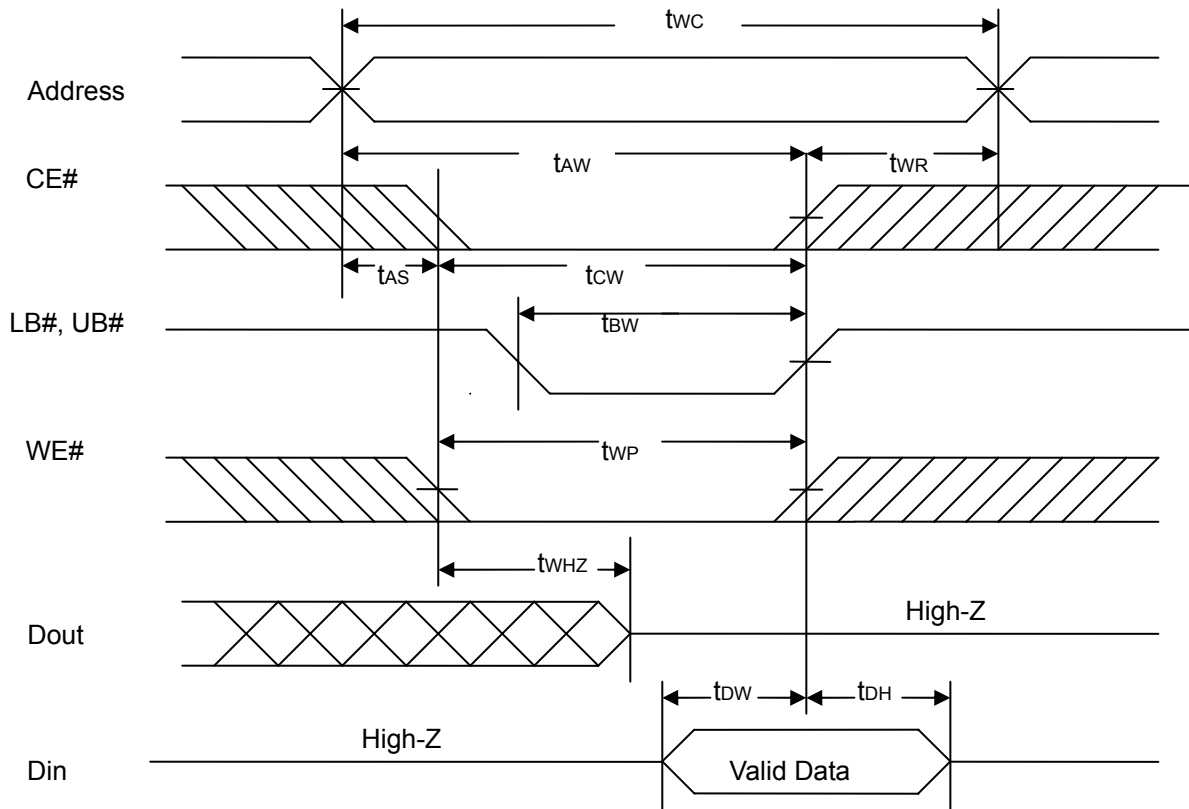
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



WRITE CYCLE 3 (LB#, UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, tWP must be greater than tWHZ + tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and tWHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.

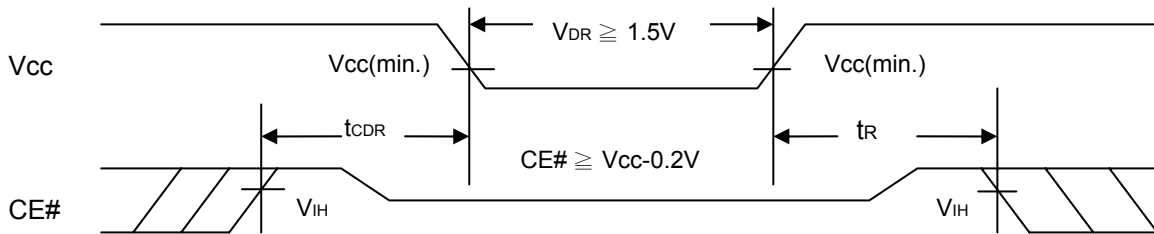
DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	CE# V ≥ V _{CC} - 0.2V	1.5	-	3.6	V	
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# V ≥ V _{CC} - 0.2V	-L	-	1	50	μA
			-LL	-	0.5	5	μA
			-LLE		0.5	10	μA
			-LLI				
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns	
Recovery Time	t _r		t _{RC} *			ns	

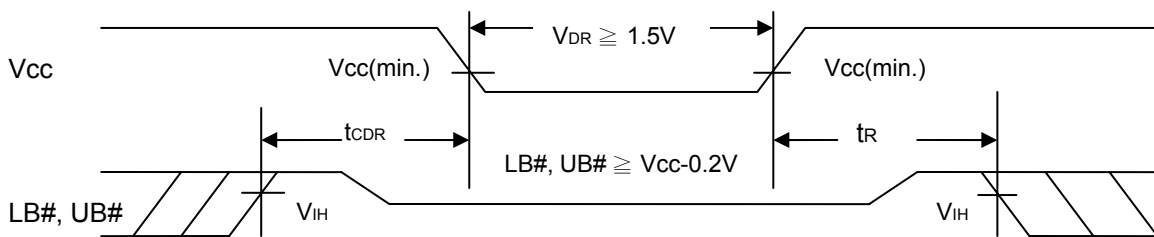
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low Vcc Data Retention Waveform (1) (CE# controlled)

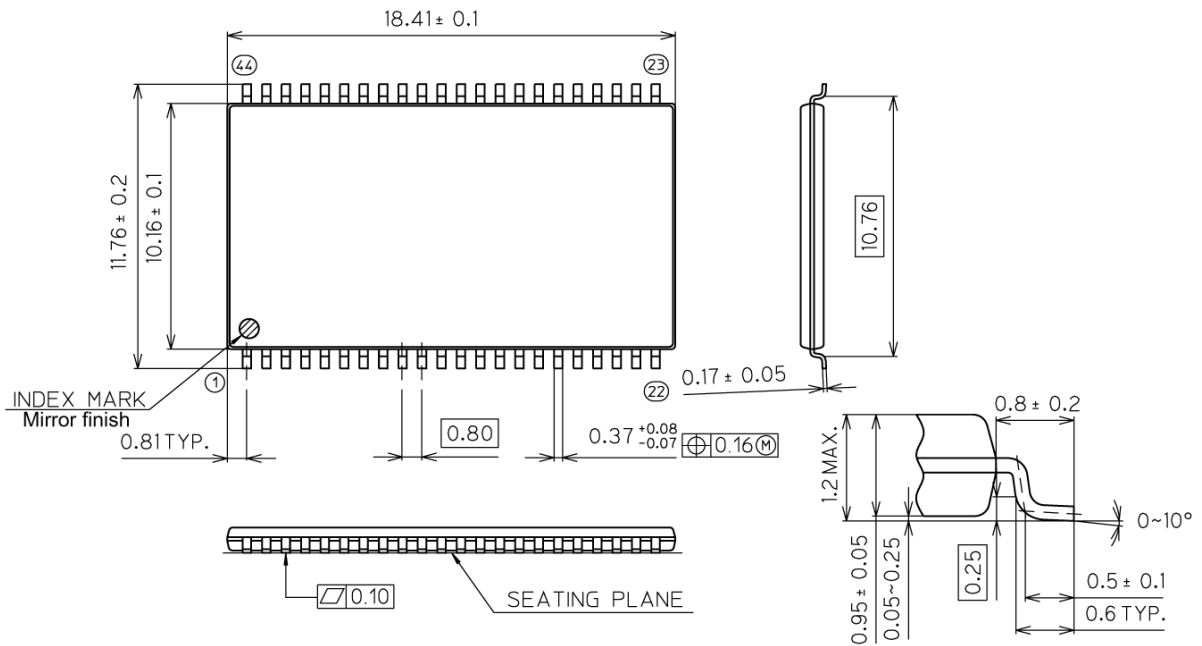


Low Vcc Data Retention Waveform (2) (LB#, UB# controlled)



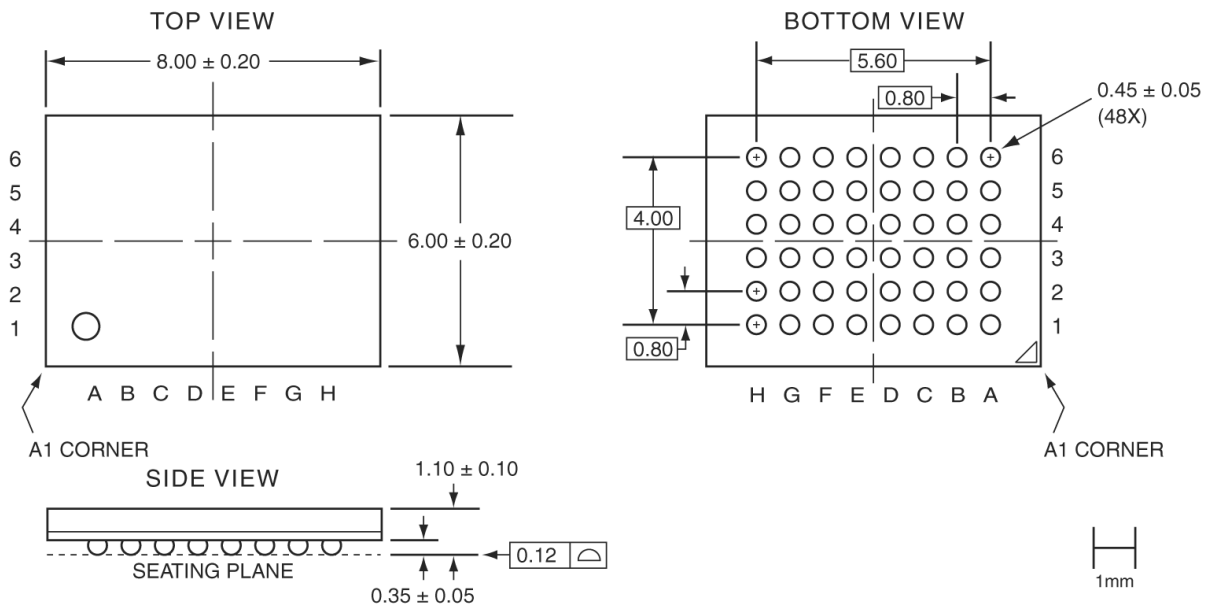
PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension

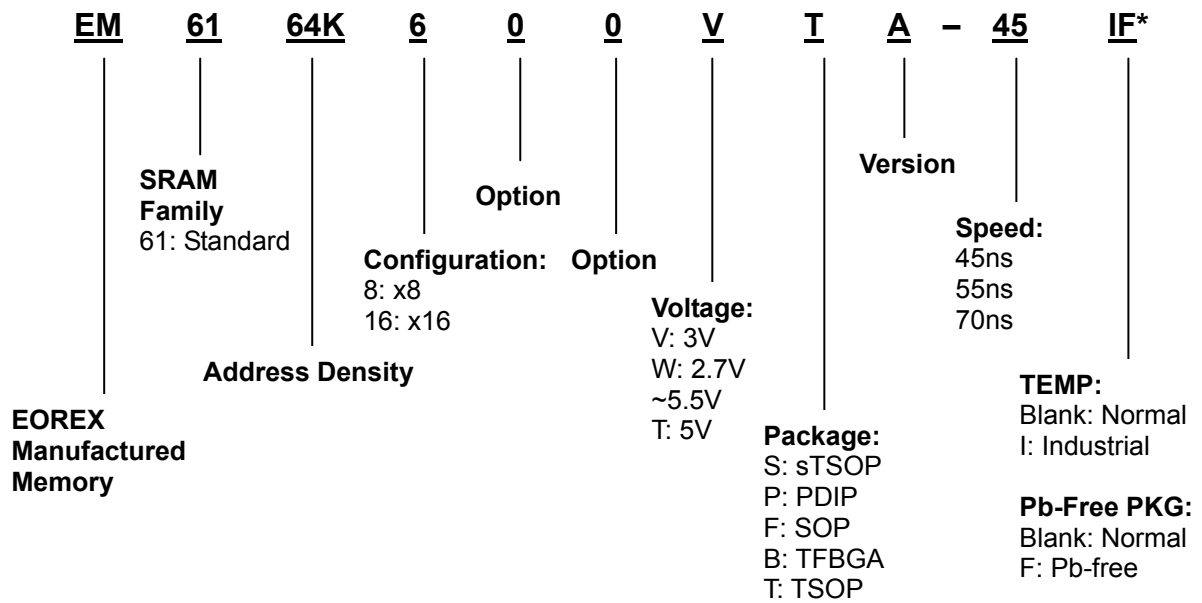


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	-	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.76	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.160	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
ZD	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0°	-	10°	0°	-	10°

48-ball 6mm × 8mm TFBGA Package Outline Dimension



Product ID Information



* Product ID example

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